WINSOURCE ELECTRONICS

THE DATASHEET OF

UCC2817D

UCC2817, UCC2818, UCC3817 and UCC3818 BiCMOS Power Factor Pregulator

1 Features

- Controls Boost Preregulator to Near-Unity Power Factor
- Limits Line Distortion
- World Wide Line Operation
- Over-Voltage Protection
- Accurate Power Limiting
- Average Current Mode Control
- Improved Noise Immunity
- Improved Feed-Forward Line Regulation
- Leading Edge Modulation
- 150-μA Typical Start-Up Current
- Low-Power BiCMOS Operation
- Up to 18-V Operation
- Frequency Range 6 kHz to 220 kHz

2 Applications

- PC Power
- Consumer Electronics
- Lighting
- Industrial Power Supplies
- IEC6100-3-2 Compliant Supplies Less Than 300 W

3 Description

The UCCx817 and UCCx818 family provides all the functions necessary for active power factor-corrected preregulators. The controller achieves near-unity power factor by shaping the AC input line current waveform to correspond to that of the AC input line voltage. Average current mode control maintains stable, low distortion sinusoidal line current.

Designed in Texas Instrument's BiCMOS process, the UCCx817 and UCCx818 offers new features such as lower start-up current, lower power dissipation, overvoltage protection, a shunt UVLO detect circuitry, a leading-edge modulation technique to reduce ripple current in the bulk capacitor, and an improved, low-offset (±2-mV) current amplifier to reduce distortion at light load conditions.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC2817, UCC2818, UCC3817, UCC3818	SOIC (16)	3.91 mm × 9.9 mm
		7.5 mm × 10.3 mm
	PDIP (16)	6.35 mm × 19.3 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram

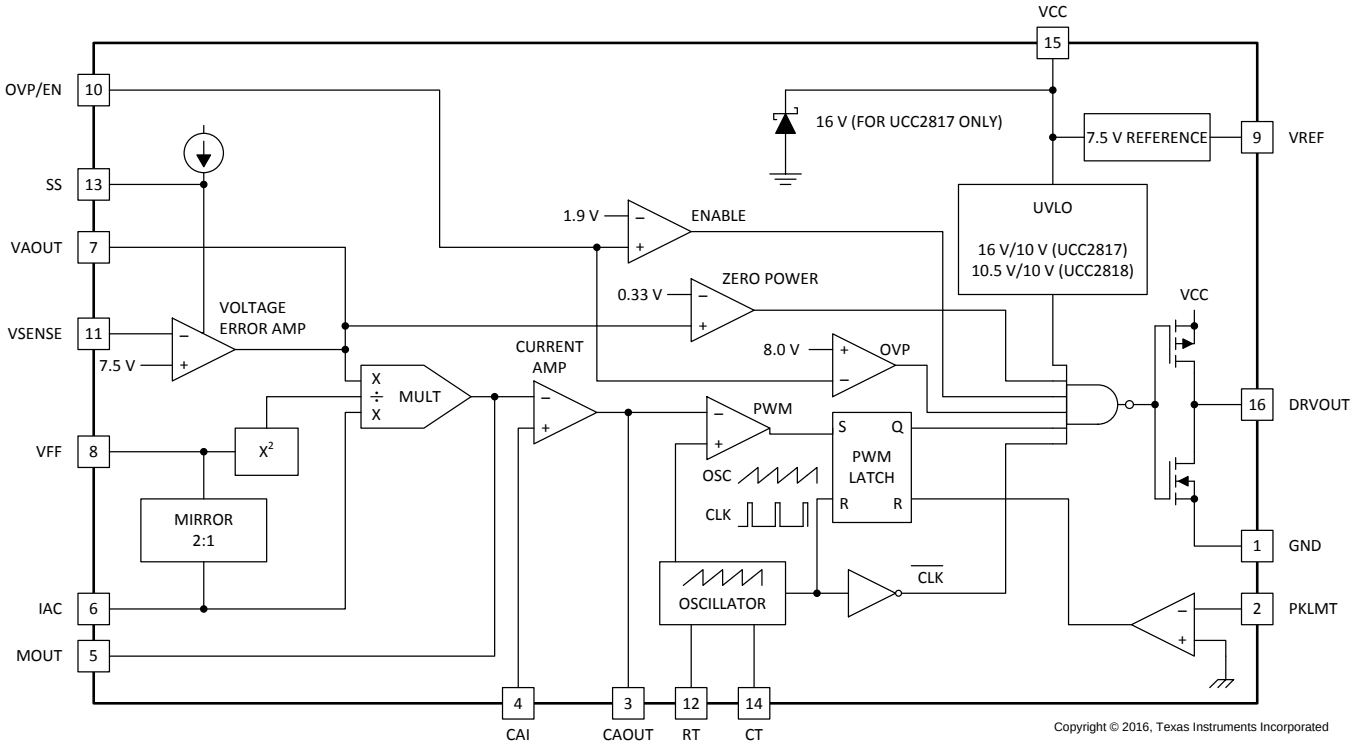

Table of Contents

1 Features ... 1
2 Applications ... 1
3 Description ... 1
4 Revision History ... 2
5 Pin Configuration and Functions ... 3
6 Specifications ... 4
6.1 Absolute Maximum Ratings ... 4
6.2 ESD Ratings ... 5
6.3 Recommended Operating Conditions ... 5
6.4 Thermal Information ... 5
6.5 Electrical Characteristics ... 5
6.6 Typical Characteristics ... 8
7 Detailed Description ... 9
7.1 Overview ... 9
7.2 Functional Block Diagram ... 9
7.3 Feature Description ... 10
7.4 Device Functional Modes ... 13
8 Application and Implementation ... 15
8.1 Application Information ... 15
8.2 Typical Application ... 16
9 Power Supply Recommendations ... 24
9.1 Power Switch Selection ... 24
10 Layout ... 25
10.1 Layout Guidelines ... 25
10.2 Layout Example ... 27
11 Device and Documentation Support ... 28
11.1 Documentation Support ... 28
11.2 Related Links ... 28
11.3 Receiving Notification of Documentation Updates 28
11.4 Community Resources ... 28
11.5 Trademarks ... 28
11.6 Electrostatic Discharge Caution ... 28
11.7 Glossary ... 28
12 Mechanical, Packaging, and Orderable Information ... 29

4 Revision History

Changes from Revision J (March 2009) to Revision K **Page**

- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

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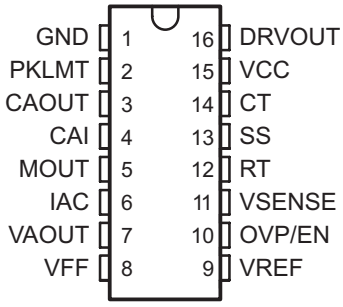
5 Pin Configuration and Functions

D, DW, N, and PW Packages
16 Pins
Top View



Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
GND	1	–	Ground. All voltages measured with respect to ground. VCC and REF should be bypassed directly to GND with a 0.1-μF or larger ceramic capacitor.
PKLMT	2	I	PFC peak current limit. The threshold for peak limit is 0 V. Use a resistor divider from the negative side of the current sense resistor to VREF to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0 V.
CAOUT	3	O	Current amplifier output. This is the output of a wide bandwidth operational amplifier that senses line current and commands the PFC pulse-width modulator (PWM) to force the correct duty cycle. Compensation components are placed between CAOUT and MOUT.
CAI	4	I	Current amplifier noninverting input. Place a resistor between this pin and the GND side of current sense resistor. This input and the inverting input (MOUT) remain functional down to and below GND.
MOUT	5	I/O	Multiplier output and current amplifier inverting input. The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high-impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier output current is limited to ($2 \times I_{IAC}$). The multiplier output current is given by the equation: $$I_{MOUT} = \frac{I_{IAC} \times (V_{VAOUT} - 1)}{V_{VFF}^2 \times K}$$ where • K = 1/V is the multiplier gain constant (1)
IAC	6	I	Current proportional to input voltage. This input to the analog multiplier is a current proportional to instantaneous line voltage. The multiplier is tailored for very low distortion from this current input (I_{IAC}) to multiplier output. The recommended maximum I_{IAC} is 500 μA.
VAOUT	7	O	Voltage amplifier output. This is the output of the operational amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5 V to prevent overshoot.
VFF	8	I	Feed-forward voltage. The RMS voltage signal generated at this pin by mirroring 1/2 of the I_{IAC} into a single pole external filter. At low line, the VFF voltage should be 1.4 V.
VREF	9	O	Voltage reference output. VREF is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 20 mA to peripheral circuitry, and is internally short-circuit current-limited. VREF is disabled and remains at 0 V when V_{VCC} is below the UVLO threshold. Bypass VREF to GND with a 0.1-μF or larger ceramic capacitor for best stability. Refer to Figure 1 and Figure 2 for VREF line and load regulation characteristics.
OVP/EN	10	I	Over-voltage/enable. A window comparator input that disables the output driver if the boost output voltage is a programmed level above the nominal ,or disables both the PFC output driver and resets SS if pulled below 1.9 V (typ).

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Pin Functions (continued)

PIN		I/O	DESCRIPTION
NAME	NO.		
VSENSE	11	I	Voltage amplifier inverting input. This is normally connected to a compensation network and to the boost converter output through a divider network.
RT	12	I	Oscillator charging current. A resistor from RT to GND is used to program oscillator charging current. A resistor between 10 kΩ and 100 kΩ is recommended. Nominal voltage on this pin is 3 V.
SS	13	I	Soft-start. V_{SS} is discharged for V_{VCC} low conditions. When enabled, SS charges an external capacitor with a current source. This voltage is used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a V_{VCC} dropout, the OVP/EN is forced below 1.9 V (typ), SS quickly discharges to disable the PWM. Note: In an open-loop test circuit, grounding the SS pin does not ensure 0% duty cycle. See the Application and Implementation for details.
CT	14	I	Oscillator timing capacitor. A capacitor from CT to GND sets the PWM oscillator frequency according to: $f \approx 0.6/(RT \times CT)$ (2) The lead from the oscillator timing capacitor to GND should be as short and direct as possible.
VCC	15	I	Positive supply voltage. Connect to a stable source of at least 20 mA between 10 V and 17 V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices are inhibited unless V_{VCC} exceeds the upper undervoltage lockout voltage threshold and remains above the lower threshold.
DRVOUT	16	O	Gate drive. The output drive for the boost switch is a totem-pole MOSFET gate driver on DRVOUT. Use a series gate resistor to prevent interaction between the gate impedance and the output driver that might cause the DRVOUT to overshoot excessively. See Figure 6 to determine minimum required gate resister value. Some overshoot of the DRVOUT output is always expected when driving a capacitive load.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) (1)

		MIN	MAX	UNIT
	Supply voltage VCC		18	V
	Supply current ICC		20	mA
	Gate drive current, continuous		0.2	A
	Gate drive current		1.2	A
	Input voltage, CAI, MOUT, SS		8	V
	Input voltage, PKLMT		5	V
	Input voltage, VSENSE, OVP/EN		10	V
	Input current, RT, IAC, PKLMT		10	mA
	Input current, VCC (no switching)		20	mA
	Maximum negative voltage, DRVOUT, PKLMT, MOUT		–0.5	V
	Power dissipation		1	W
T_J	Junction temperature	–55	150	°C
T_{stg}	Storage temperature	–65	150	°C
T_{sol}	Lead temperature (soldering, 10 seconds)		300	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

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6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001 (1)	±2000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101 (2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VCC	Input voltage		12		V
VSENSE	Input sense voltage		7.5	10	V
	Input current for oscillator		1.36	10	mA

6.4 Thermal Information

THERMAL METRIC (1)		UCC281x, UCC381x				UNIT
		SOIC (D)	SOIC (DW)	PDIP (N)	TSSOP (PW)	
		16 PINS	16 PINS	16 PINS	16 PINS	
$R_{\theta JA}$	Junction-to-ambient thermal resistance	73.9 (2)	74.1 (2)	49.3 (2)	98.9 (3)	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	33.5	35.5	38.9	30.2 (3)	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	31.4	38.9	29.4	44.8	°C/W
ψ_{JT}	Junction-to-top characterization parameter	5.8	9.9	18.9	1.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	31.1	38.3	29.2	44.1	°C/W

(1) For more information about traditional and new thermal metrics, For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report.
(2) Specified θ_{ja} (junction to ambient) is for devices mounted to 5-inch^2 FR4 PC board with one ounce copper, where noted. When resistance range is given, lower values are for 5 inch^2 aluminum PC board. Test PWB was 0.062-inch thick and typically used 0.635-mm trace widths for power packages and 1.3-mm trace widths for non-power packages with a 100-mil × 100-mil probe land area at the end of each trace.
(3) Modeled data. If value range given for θ_{ja}, lower value is for 3×3 inch. 1 oz internal copper ground plane, higher value is for 1×1-inch. ground plane. All model data assumes only one trace for each non-fused lead.

6.5 Electrical Characteristics

T_A = 0°C to 70°C for the UCC3817, and T_A = −40°C to 85°C for the UCC2817, $T_A = T_J$, VCC = 12 V, R_T = 22 kΩ, C_T = 270 pF, (unless otherwise noted)

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
SUPPLY CURRENT						
	Supply current, off	VCC = (VCC turn-on threshold −0.3 V)		150	300	µA
	Supply current, on	VCC = 12 V, No load on DRVOUT	2	4	6	mA
UVLO						
	VCC turn-on threshold (UCCx817)		15.4	16	16.6	V
	VCC turn-off threshold (UCCx817)		9.4	9.7		V
	UVLO hysteresis (UCCx817)		5.8	6.3		V
	Maximum shunt voltage (UCCx817)	I_{VCC} = 10 mA	15.4	17	17.5	V
	VCC turn-on threshold (UCCx818)		9.7	10.2	10.8	V
	VCC turn-off threshold (UCCx818)		9.4	9.7		V
	UVLO hysteresis (UCCx818)		0.3	0.5		V
VOLTAGE AMPLIFIER						

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Electrical Characteristics (continued)

T_A = 0°C to 70°C for the UCC3817, and T_A = −40°C to 85°C for the UCC2817, $T_A = T_J$, VCC = 12 V, R_T = 22 kΩ, C_T = 270 pF, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Input voltage	T_A = 0°C to 70°C	7.387	7.5	7.613	V
	T_A = −40°C to 85°C	7.369	7.5	7.631	
V_{SENSE} bias current	$V_{SENSE} = V_{REF}$, VAOUT = 2.5 V		50	200	nA
Open loop gain	VAOUT = 2 V to 5 V	50	90		dB
High-level output voltage	I_L = −150 μA	5.3	5.5	5.6	V
Low-level output voltage	I_L = 150 μA	0	50	150	mV
OVERVOLTAGE PROTECTION AND ENABLE					
Over voltage reference		VREF +0.48	VREF +0.50	VREF +0.52	V
Hysteresis		300	500	600	mV
Enable threshold		1.7	1.9	2.1	V
Enable hysteresis		0.1	0.2	0.3	V
CURRENT AMPLIFIER					
Input offset voltage	V_{CM} = 0 V, V_{CAOUT} = 3 V	–3.5	0	2.5	mV
Input bias current	V_{CM} = 0 V, V_{CAOUT} = 3 V		–50	–100	nA
Input offset current	V_{CM} = 0 V, V_{CAOUT} = 3 V		25	100	nA
Open loop gain	V_{CM} = 0 V, V_{CAOUT} = 2 V to 5 V	90			dB
Common-mode rejection ratio	V_{CM} = 0 V to 1.5 V, V_{CAOUT} = 3 V	60	80		dB
High-level output voltage	I_L = −120 μA	5.6	6.5	6.8	V
Low-level output voltage	I_L = 1 mA	0.1	0.2	0.5	V
Gain bandwidth product			(1)2.5		MHz
VOLTAGE REFERENCE					
Input voltage	T_A = 0°C to 70°C	7.387	7.5	7.613	V
	T_A = −40°C to 85°C	7.369	7.5	7.631	
Load regulation	I_{REF} = 1 mA to 2 mA	0		10	mV
Line regulation	VCC = 10.8 V to 15 V, (2)	0		10	mV
Short-circuit current	V_{REF} = 0 V	–20	–25	–50	mA
OSCILLATOR					
Initial accuracy	T_A = 25°C	85	100	115	kHz
Voltage stability	VCC = 10.8 V to 15 V	–1%		1%	
Total variation	Line, temp	80		120	kHz
Ramp peak voltage		4.5	5	5.5	V
Ramp amplitude voltage (peak to peak)		3.5	4	4.5	V
PEAK CURRENT LIMIT					
PKLMT reference voltage		–15		15	mV
PKLMT propagation delay		150	350	500	ns
MULTIPLIER					
I_{MOUT}, high line, low power output current, (0°C to 85°C)	I_{AC} = 500 μA, V_{FF} = 4.7 V, VAOUT = 1.25 V	0	–6	–20	μA
I_{MOUT}, high line, low power output current, (–40°C to 85°C)	I_{AC} = 500 μA, V_{FF} = 4.7 V, VAOUT = 1.25 V	0	–6	–23	μA
I_{MOUT}, high line, high power output current	I_{AC} = 500 μA, V_{FF} = 4.7 V, VAOUT = 5 V	–70	–90	–105	μA

(1) Ensured by design, not production tested.
(2) Reference variation for V_{CC} < V is shown in Figure 1.

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Electrical Characteristics (continued)

T_A = 0°C to 70°C for the UCC3817, and T_A = −40°C to 85°C for the UCC2817, $T_A = T_J$, VCC = 12 V, R_T = 22 kΩ, C_T = 270 pF, (unless otherwise noted)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
I_{MOUT}, low line, low power output current	I_{AC} = 150 µA, V_{FF} = 1.4 V, VAOUT = 1.25 V	–10	–19	–50	µA
I_{MOUT}, low line, high power output current	I_{AC} = 150 µA, V_{FF} = 1.4 V, VAOUT = 5 V	–268	–300	–345	µA
I_{MOUT}, IAC limited output current	I_{AC} = 150 µA, V_{FF} = 1.3 V, VAOUT = 5 V	–250	–300	–400	µA
Gain constant (K)	I_{AC} = 300 µA, V_{FF} = 3 V, VAOUT = 2.5 V	0.5	1	1.5	1/V
I_{MOUT}, zero current	I_{AC} = 150 µA, V_{FF} = 1.4 V, VAOUT = 0.25 V		0	–2	µA
	I_{AC} = 500 µA, V_{FF} = 4.7 V, VAOUT = 0.25 V		0	–2	
I_{MOUT}, zero current, (0°C to 85°C)	I_{AC} = 500 µA, V_{FF} = 4.7 V, VAOUT = 0.5 V		0	–3	µA
I_{MOUT}, zero current, (–40°C to 85°C)	I_{AC} = 500 µA, V_{FF} = 4.7 V, VAOUT = 0.5 V		0	–3.5	µA
Power limit (I_{MOUT} x V_{FF})	I_{AC} = 150 µA, V_{FF} = 1.4 V, VAOUT = 5 V	–375	–420	–485	µW
FEED-FORWARD					
VFF output current	I_{AC} = 300 µA	–140	–150	–160	µA
SOFT START					
SS charge current		–6	–10	–16	µA
GATE DRIVER					
Pullup resistance	I_O = –100 mA to −200 mA		5	12	Ω
Pulldown resistance	I_O = 100 mA		2	10	Ω
Output rise time	C_L = 1 nF, R_L = 10 Ω, V_{DRVOUT} = 0.7 V to 9.0 V		25	50	ns
Output fall time	C_L = 1 nF, R_L = 10 Ω, V_{DRVOUT} = 9.0 V to 0.7 V		10	50	ns
Maximum duty cycle		93%	95%	99%	
Minimum controlled duty cycle	At 100 kHz			2%	
ZERO POWER					
Zero power comparator threshold	Measured on VAOUT	0.20	0.33	0.50	V

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6.6 Typical Characteristics

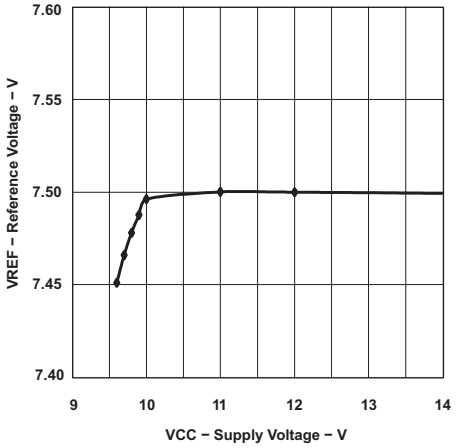

Figure 1. Reference Voltage vs Supply Voltage

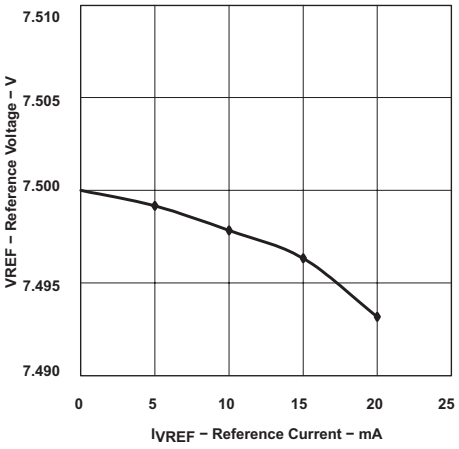

Figure 2. Reference Voltage vs Reference Current

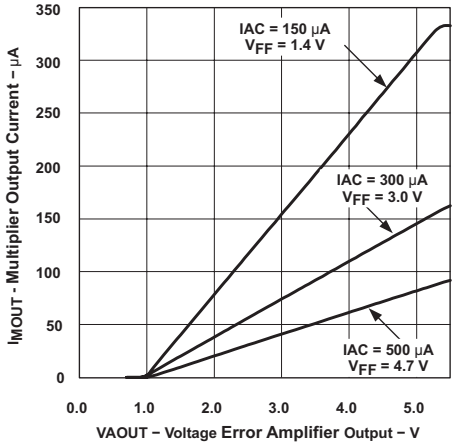

Figure 3. Multiplier Output Current vs Voltage Error Amplifier Output

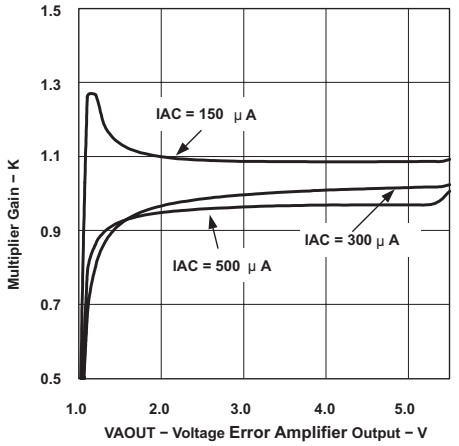

Figure 4. Multiplier Gain vs Voltage Error Amplifier Output

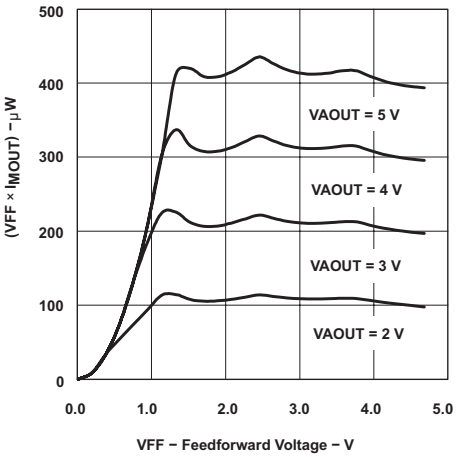

Figure 5. Multiplier Constant Power Performance

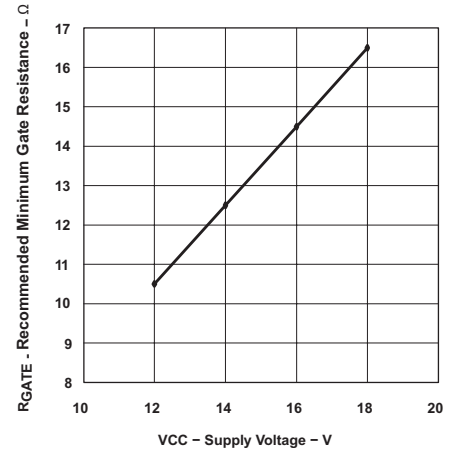

Figure 6. Recommended Minimum Gate Resistance vs Supply Voltage

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7 Detailed Description

7.1 Overview

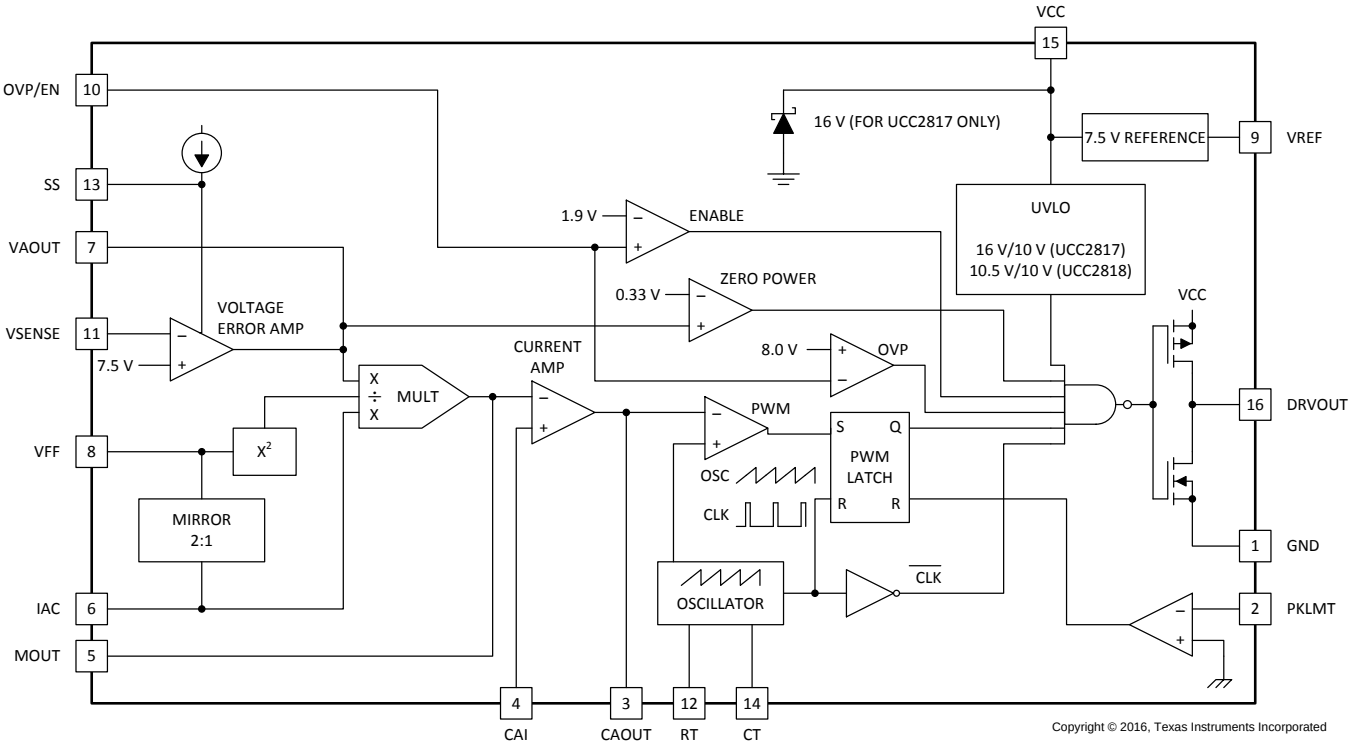
The UCC3817 and the UCC3818 family of products provides PFC controllers all the necessary functions for achieving near unity PFC.

The UCC3817 and UCC3818, while being pin-compatible with other industry controllers providing similar functionality, offer many feature enhancements and tighter specifications, leading to an overall reduction in system implementation cost.

The system performance is enhanced by incorporating many innovative features such as average current-mode control which maintains stable noise immune low distortion sinusoidal current. Also, the device features a leading edge modulation which when synchronized properly with a second stage DC-DC converter can reduce the ripple current on the output capacitor thereby increasing the overall lifetime of the power supply.

In addition to these features, the key difference between the UCC281x and the UCC381x is that the UCC2817 can work over the extended temperature range of –40 to +85°C as opposed to 0 to +70°C in the case of the UCC3817.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Reference Section and Error Amplifier

The reference is a highly accurate 7-V reference with an accuracy of the reference is 1.5%.

The error amplifier is a classic voltage error amplifier and has a short circuit current capability of 20 mA.

7.3.2 Zero Power Block

When the output of the zero power comparator goes below 2.3 V, the zero power comparator latches the gate drive signal low.

7.3.3 Multiplier

The multiplier has 3 inputs. The inputs to the multiplier are VAOUT, the voltage amplifier error signal, IIAC, a representation of the input rectified AC line voltage, and an input voltage feedforward signal, VVFF.

The multiplier performs the calculation in Equation 3.

$$IMOUNT = IAC \times (VVAOUT - 1) / (K \times VVff^2)$$

where

- $K = 1/V$ (3)

As the multiplier output is a current, this is a high-impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation.

7.3.4 Output Overvoltage Protection

When the output voltage exceeds the OVP threshold, the IC stops switching. The OVP reference is at 1.07%. There is also a 500 mV of hysteresis at the pin.

7.3.5 Pin Descriptions

7.3.5.1 CAI

Place a resistor between this pin and the GND side of current sense resistor. This input and the inverting input (MOUT) remain functional down to and below GND.

7.3.5.2 CAOUT

This is the output of a wide bandwidth operational amplifier that senses line current and commands the PFC pulse-width modulator (PWM) to force the correct duty cycle. Compensation components are placed between CAOUT and MOUT.

7.3.5.3 CT

A capacitor from CT to GND sets the PWM oscillator frequency according to Equation 4:

$$f \approx \left(\frac{0.6}{RT \times CT} \right) \quad (4)$$

The lead from the oscillator timing capacitor to GND should be as short and direct as possible.

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Feature Description (continued)

7.3.5.4 DRVOUT

The output drive for the boost switch is a totem-pole MOSFET gate driver on DRVOUT. To avoid the excessive overshoot of the DRVOUT while driving a capacitive load, a series gate current-limiting/damping resistor is recommended to prevent interaction between the gate impedance and the output driver. The value of the series gate resistor is based on the pulldown resistance ($R_{pulldown}$ which is 4 Ω typical), the maximum VCC voltage (VCC), and the required maximum gate drive current (I_{MAX}). Using Equation 5, a series gate resistance of resistance 11 Ω would be required for a maximum VCC voltage of 18 V and for 1.2 A of maximum sink current. The source current will be limited to approximately 900 mA (based on the Rpullup of 9-Ω typical).

$$R_{GATE} = \frac{VCC - (I_{MAX} \times R_{pulldown})}{I_{MAX}} \quad (5)$$

7.3.5.5 GND

All voltages measured with respect to ground. VCC and REF should be bypassed directly to GND with a 0.1-µF or larger ceramic capacitor.

7.3.5.6 IAC

This input to the analog multiplier is a current proportional to instantaneous line voltage. The multiplier is tailored for very low distortion from this current input (I_{IAC}) to multiplier output. The recommended maximum I_{IAC} is 500 µA.

7.3.5.7 MOUT

The output of the analog multiplier and the inverting input of the current amplifier are connected together at MOUT. As the multiplier output is a current, this is a high-impedance input so the amplifier can be configured as a differential amplifier. This configuration improves noise immunity and allows for the leading-edge modulation operation. The multiplier output current is limited to ($2 \times I_{IAC}$). The multiplier output current is given by Equation 6:

$$I_{MOUT} = \frac{I_{IAC} \times (V_{VAOUT} - 1)}{V_{VFF}^2 \times K} \quad (6)$$

where $K = \frac{1}{V}$ is the multiplier gain constant.

7.3.5.8 OVP/EN

A window comparator input that disables the output driver if the boost output voltage is a programmed level above the nominal or disables both the PFC output driver and resets SS if pulled below 1.9 V (typical).

7.3.5.9 PKLMT

The threshold for peak limit is 0 V. Use a resistor divider from the negative side of the current sense resistor to VREF to level shift this signal to a voltage level defined by the value of the sense resistor and the peak current limit. Peak current limit is reached when PKLMT voltage falls below 0 V.

7.3.5.10 RT

A resistor from RT to GND is used to program oscillator charging current. TI recommends a resistor between 10 kΩ and 100 kΩ. Nominal voltage on this pin is 3 V.

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Feature Description (continued)

7.3.5.11 SS

VSS is discharged for VVCC low conditions. When enabled, SS charges an external capacitor with a current source. This voltage is used as the voltage error signal during start-up, enabling the PWM duty cycle to increase slowly. In the event of a V_{VCC} dropout, the OVP/EN is forced below 1.9 V (typ), SS quickly discharges to disable the PWM.

NOTE

In an open-loop test circuit, grounding the SS pin does not ensure 0% duty cycle. See the application section for details.

7.3.5.12 VAOUT

This is the output of the operational amplifier that regulates output voltage. The voltage amplifier output is internally limited to approximately 5.5 V to prevent overshoot.

7.3.5.13 VCC

Connect to a stable source of at least 20 mA from 10 V to 17 V for normal operation. Bypass VCC directly to GND to absorb supply current spikes required to charge external MOSFET gate capacitances. To prevent inadequate gate drive signals, the output devices are inhibited unless V_{VCC} exceeds the upper undervoltage lockout voltage threshold and remains above the lower threshold.

7.3.5.14 VFF

The RMS voltage signal generated at this pin by mirroring 1/2 of the I_{IAC} into a single pole external filter. At low line, the VFF voltage should be 1.4 V.

7.3.5.15 VSENSE

This is normally connected to a compensation network and to the boost converter output through a divider network.

7.3.5.16 VREF

VREF is the output of an accurate 7.5-V voltage reference. This output is capable of delivering 20 mA to peripheral circuitry and is internally short-circuit current limited. VREF is disabled and remains at 0 V when V_{VCC} is below the UVLO threshold. Bypass VREF to GND with a 0.1-µF or larger ceramic capacitor for best stability. See Figure 13 and Figure 14 for VREF line and load regulation characteristics.

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7.4 Device Functional Modes

7.4.1 Transition Mode Control

The boost converter, the most common topology used for power factor correction, can operate in two modes: continuous conduction code (CCM) and discontinuous conduction mode (DCM). Transition mode control, also referred to as critical conduction mode (CRM) or boundary conduction mode, maintains the converter at the boundary between CCM and DCM by adjusting the switching frequency.

The CRM converter typically uses a variation of hysteretic control, with the lower boundary equal to zero current. It is a variable frequency control technique that has inherently stable input current control while eliminating reverse recovery rectifier losses. As shown in Figure 7, the switch current is compared to the reference signal (output of the multiplier) directly. This control method has the advantage of simple implementation and good power factor correction.

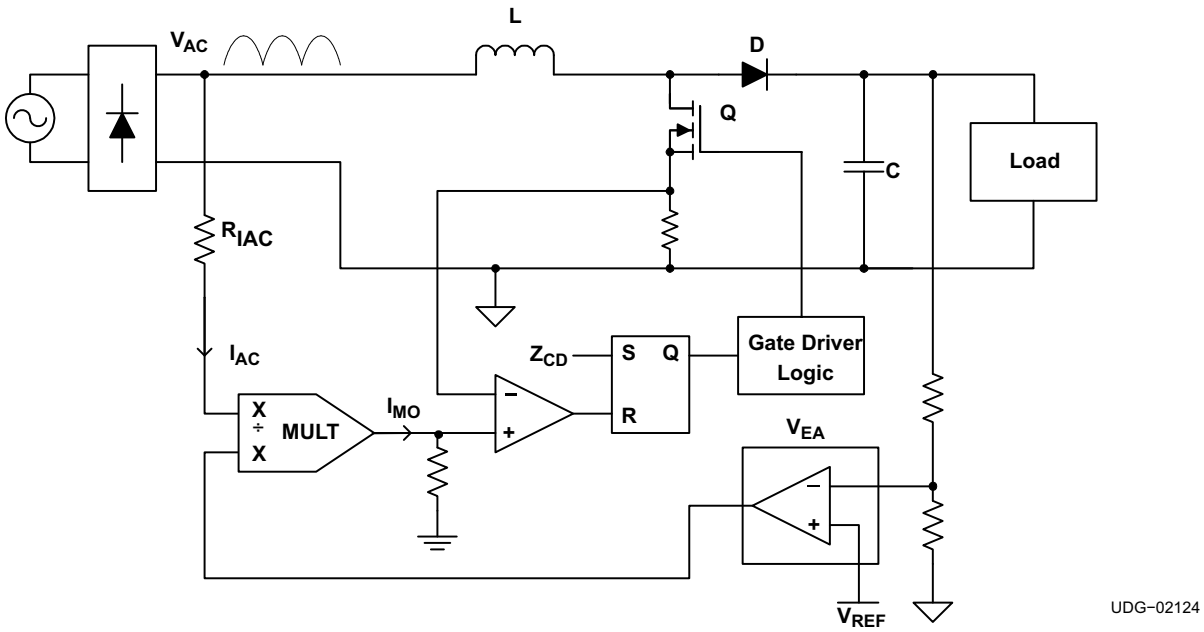

Figure 7. Basic Block Diagram of CRM Boost PFC

Device Functional Modes (continued)

The power stage equations and the transfer functions of the CRM are the same as the CCM. However, implementations of the control functions are different. Transition mode forces the inductor current to operate just at the border of CCM and DCM. The current profile is also different, and affects the component power loss and filtering requirements. The peak current in the CRM boost is twice the amplitude of CCM, leading to higher conduction losses. The peak-to-peak ripple is twice the average current, which affects MOSFET switching losses and magnetics AC losses.

For low to medium power applications up to approximately 300 W, the CRM boost has an advantage in losses. The filtering requirement is not severe, and therefore is not a disadvantage. For medium to higher power applications, where the input filter requirements dominate the size of the magnetics, the CCM boost is a good choice due to lower peak currents (which reduces conduction losses) and lower ripple current (which reduces filter requirements). The main tradeoff in using CRM boost is lower losses due to no reverse recovery in the boost diode vs higher ripple and peak currents.

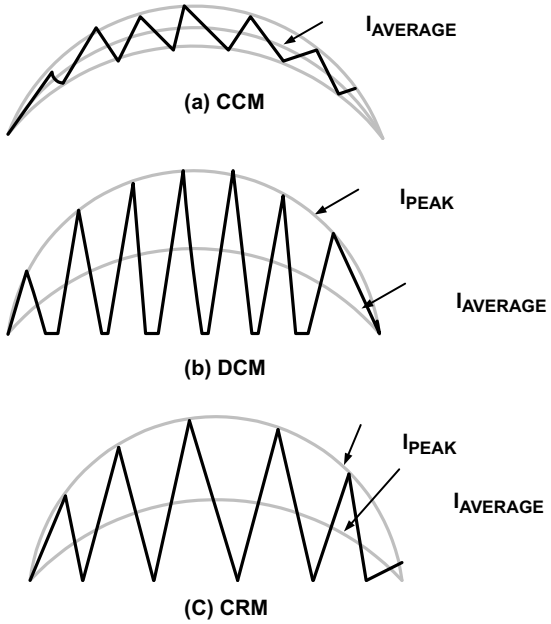

Figure 8. PFC Inductor Current Profiles

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8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCC3817 is a BiCMOS average current mode boost controller for high power factor, high efficiency preregulator power supplies. Figure 9 shows the UCC3817 in a 250-W PFC preregulator circuit. Off-line switching power converters normally have an input current that is not sinusoidal. The input current waveform has a high harmonic content because current is drawn in pulses at the peaks of the input voltage waveform. An active power-factor correction circuit programs the input current to follow the line voltage, forcing the converter to look like a resistive load to the line. A resistive load has 0° phase displacement between the current and voltage waveforms. Power factor can be defined in terms of the phase angle between two sinusoidal waveforms of the same frequency:

$PF = \cos \theta$

Therefore, a purely resistive load would have a power factor of 1. In practice, power factors of 0.999 with THD (total harmonic distortion) of less than 3% are possible with a well-designed circuit. The following guidelines are provided to design PFC boost converters using the UCC3817.

NOTE

Schottky diodes, D5 and D6, are required to protect the PFC controller from electrical over stress during system power up.

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8.2 Typical Application

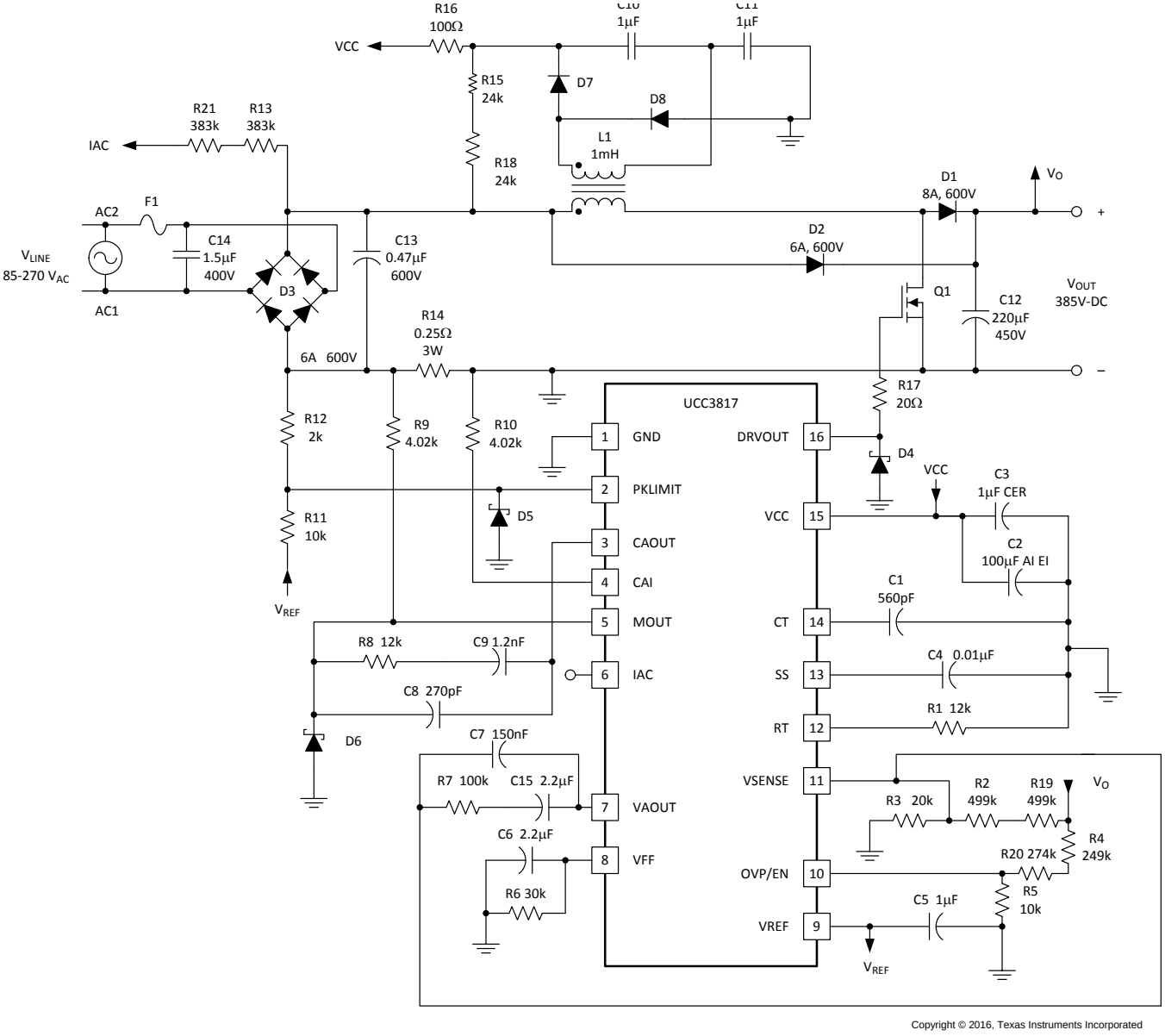

Figure 9. Typical Application Circuit

8.2.1 Design Requirements

Table 1 lists the parameters for this application.

Table 1. Design Parameters

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
VIN	Input RMS voltage		85		270	V
	Input frequency			50/60		Hz
VOUT	Output Voltage			385	420	V
POUT	Output Power			250		W
	Holdup Time	All line and load conditions		16		ms
	Efficiency	Efficiency at 85 Vrms, 100% Load		91%		

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Typical Application (continued)

Table 1. Design Parameters (continued)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
THD at Low Line	85 Vrms = 100% Load		5%		
THD at High Line	265 Vrms, 100% Load		15%		

8.2.2 Detailed Design Procedure

8.2.2.1 Power Stage

8.2.2.1.1 L_{BOOST}

The boost inductor value is determined by:

$$L_{BOOST} = \frac{\left(V_{IN(min)} \times D\right)}{(\Delta I \times fs)} \quad (7)$$

where

- D is the duty cycle
- ΔI is the inductor ripple current
- f_S is the switching frequency

For the example circuit in Figure 9, a switching frequency of 100 kHz, a ripple current of 875 mA, a maximum duty cycle of 0.688, and a minimum input voltage of 85 V_{RMS} give a boost inductor value of approximately 1 mH. The values used in this equation are at the peak of low line, where the inductor current and its ripple are at a maximum.

8.2.2.1.2 C_{OUT}

Two main criteria, the capacitance and the voltage rating, dictate the selection of the output capacitor. The value of capacitance is determined by the holdup time required for supporting the load after input ac voltage is removed. Holdup is the amount of time that the output stays in regulation after the input has been removed. For the circuit in Figure 9, the desired holdup time is approximately 16 ms. Expressing the capacitor value in terms of output power, output voltage, and holdup time gives the equation:

$$C_{OUT} = \frac{\left(2 \times P_{OUT} \times \Delta t\right)}{\left(V_{OUT}^{2} - V_{OUT(min)}^{2}\right)} \quad (8)$$

In practice, the calculated minimum capacitor value may be inadequate, because output ripple voltage specifications limit the amount of allowable output capacitor ESR. Attaining a sufficiently low value of ESR often requires the use of a much larger capacitor value than calculated. The amount of output capacitor ESR allowed is determined by dividing the maximum specified output ripple voltage by the inductor ripple current. In the design in Figure 9, holdup time is the dominant determining factor, and a 220-µF, 450-V capacitor was chosen for the output voltage level of 385 VDC at 250 W.

8.2.2.2 Softstart

The softstart circuitry prevents overshoot of the output voltage during start up by bringing up the voltage amplifier output (V_{VAOUT}) slowly, which allows for the PWM duty cycle to increase slowly. Use the following equation to select a capacitor for the softstart pin.

In this example, t_{DELAY} is equal to 7.5 ms, which would yield a C_{SS} of 10 nF.

$$C_{SS} = \frac{10\ \mu A \times t_{DELAY}}{7.5\ V} \quad (9)$$

In an open-loop test circuit, shorting the softstart pin to ground does not ensure 0% duty cycle. This is due to the input offset voltage of the current amplifier, which could force the current amplifier output high or low depending on the polarity of the offset voltage. However, in the typical application there is sufficient amount of inrush and bias current to overcome the offset voltage of the current amplifier.

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8.2.2.3 Multiplier

The output of the multiplier of the UCC3817 is a signal representing the desired input line current. The multiplier is an input to the current amplifier, which programs the current loop to control the input current to give high power factor operation. As such, the proper functioning of the multiplier is key to the success of the design. The inputs to the multiplier are VAOUT, the voltage amplifier error signal, I_{IAC}, a representation of the input rectified ac line voltage, and an input voltage feedforward signal, V_{VFF}. The output of the multiplier, I_{MOUT}, can be expressed as:

$$I_{MOUT} = I_{IAC} \times \frac{\left(V_{VAOUT} - 1\right)}{K \times V_{VFF}^{2}} \quad (10)$$

where

- K is a constant typically equal to 1/V

Electrical Characteristics covers all the required operating conditions for designing with the multiplier. Additionally, Figure 3, Figure 4, and Figure 5 provide typical multiplier characteristics over its entire operating range.

The I_{IAC} signal is obtained through a high-value resistor connected between the rectified ac line and the IAC pin of the UCC381x. This resistor (R_{IAC}) is sized to give the maximum I_{IAC} current at high line. For the UCC381x, the maximum I_{IAC} current is approximately 500 μA. A higher current than this can drive the multiplier out of its linear range. A smaller current level is functional, but noise can become an issue, especially at low input line. Assuming a universal line operation of 85 V_{RMS} to 265 V_{RMS} gives an R_{IAC} value of 750 kΩ. Because of voltage rating constraints of standard 1/4-W resistor, use a combination of lower value resistors connected in series to give the required resistance and distribute the high voltage amongst the resistors. For the design example in Figure 9, two 383-kΩ resistors are used in series.

The current into the IAC pin is mirrored internally to the VFF pin, where it is filtered to produce a voltage feed forward signal proportional to line voltage. The VFF voltage keeps the power stage gain constant, and to provide input power limiting. Refer to Texas Instruments application note DN-66 UC3854A/B and UC3855A/B Provide Power Limiting with Sinusoidal Input (SLUA196) for detailed explanation on how the VFF pin provides power limiting. The following equation can be used to size the VFF resistor (R_{VFF}) to provide power limiting where $V_{IN(min)}$ is the minimum RMS input voltage, and R_{IAC} is the total resistance connected between the IAC pin and the rectified line voltage.

$$R_{VFF} = \frac{1.4\ V}{\frac{V_{IN(min)} \times 0.9}{2 \times R_{IAC}}} \approx 30\ k\Omega \quad (11)$$

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Because the VFF voltage is generated from line voltage, it must be adequately filtered to reduce total harmonic distortion caused by the 120-Hz rectified line voltage. Refer to Unitrode Power Supply Design Seminar, SEM−700 Topic 7, [Optimizing the Design of a High Power Factor Preregulator.] A single pole filter is adequate for the design in Figure 9. Assuming that an allocation of 1.5% total harmonic distortion from this input is allowed, and that the second harmonic ripple is 66% of the input AC line voltage, the amount of attenuation required by this filter is:

1.5%/66% = 0.022

With a ripple frequency (f_R) of 120 Hz and an attenuation of 0.022, the pole of the filter (f_P) must be placed at:

$$f_P = 120\ \text{Hz} \times 0.022 \approx 2.6\ \text{Hz} \quad (12)$$

The following equation can be used to select the filter capacitor (C_{VFF}) required to produce the desired low pass filter.

$$C_{VFF} = 1/(2 \times \pi \times R_{VFF} \times f_P) \approx 2.2\ \mu\text{F} \quad (13)$$

The R_{MOUT} resistor is sized to match the maximum current through the sense resistor to the maximum multiplier current. The maximum multiplier current, or $I_{MOUT(max)}$, is determined by the equation:

$$I_{MOUT(max)} = \frac{I_{IAC@V_{IN(min)}} \times \left(V_{VAOUT(max)} - 1V\right)}{K \times V_{VFF(min)}^2} \quad (14)$$

$I_{MOUT(max)}$ for the design in Figure 9 is approximately 315 μA. The R_{MOUT} resistor is then determined by:

$$R_{MOUT} = V_{RSENSE}/I_{MOUT(max)} \quad (15)$$

In this example, V_{RSENSE} is selected to give a dynamic operating range of 1.25 V, which gives an R_{MOUT} of approximately 3.91 kΩ.

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8.2.2.4 Voltage Loop

The second major source of harmonic distortion is the ripple on the output capacitor at the second harmonic of the line frequency. This ripple is fed back through the error amplifier, and appears as a 3rd-harmonic ripple at the input to the multiplier. The voltage loop must be compensated, not just for stability, but also to attenuate the contribution of this ripple to the total harmonic distortion of the system (refer to Figure 10).

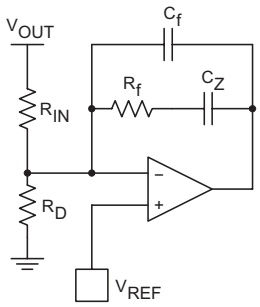

Figure 10. Voltage Amplifier Configuration

The gain of the voltage amplifier, G_{VA}, is determined by first calculating the amount of ripple present on the output capacitor. The peak value of the second harmonic voltage is given by the equation:

$$V_{OPK} = P_{IN} / (2\pi \times f_R \times C_{OUT} \times V_{OUT}) \quad (16)$$

In this example, V_{OPK} is equal to 3.91 V. Assuming an allowable contribution of 0.75% (1.5% peak to peak) from the voltage loop to the total harmonic distortion budget, set the gain equal to:

$$G_{VA} = (\Delta V_{VAOUT})(0.015) / (2 \times V_{OPK}) \quad (17)$$

where

- ΔV_{VAOUT} is the effective output voltage range of the error amplifier (5 V for the UCC3817)

The network must realize this filter is comprised of an input resistor, R_{IN}, and feedback components C_f, C_Z, and R_f. The value of R_{IN} is already determined, because of its function as one half of a resistor divider from V_{OUT} feeding back to the voltage amplifier for output voltage regulation. In this case, the value was chosen to be 1 MΩ. This high value was chosen to reduce power dissipation in the resistor. In practice, the resistor value would be realized by the use of two 500-kΩ resistors in series, because of the voltage rating constraints of most standard 1/4-W resistors. The value of C_f is determined by the equation:

$$C_f = 1 / (2\pi \times f_R \times G_{VA} \times R_{IN}) \quad (18)$$

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In this example, C_f equals 150 nF. Resistor R_f sets the dc gain of the error amplifier and thus determines the frequency of the pole of the error amplifier. The location of the pole can be found by setting the gain of the loop equation to one, and solving for the crossover frequency. The frequency, expressed in terms of input power, can be calculated by the equation:

$$f_{VI}^2 = P_{IN} / (2\pi^2 \times \Delta V_{VAOUT} \times V_{OUT} \times R_{IN} \times C_{OUT} \times C_f) \quad (19)$$

f_{VI} for this converter is 10 Hz. A derivation of this equation can be found in the Unitrode Power Supply Design Seminar SEM1000, Topic 1, [A 250-kHz, 500-W Power Factor Correction Circuit Employing Zero Voltage Transitions].

Solving for R_f becomes:

$$R_f = 1 / (2\pi \times f_{VI} \times C_f) \quad (20)$$

or R_f equals 100 kΩ.

Due to the low output impedance of the voltage amplifier, capacitor C_Z was added in series with R_F to reduce loading on the voltage divider. To ensure the voltage loop crossed over at f_{VI}, C_Z was selected to add a zero at a 10th of f_{VI}. For the design in Figure 9, a 2.2-µF capacitor was chosen for C_Z. The following equation can calculate C_Z.

$$C_Z = \frac{1}{2 \times \pi \times \frac{f_{VI}}{10} \times R_f} \quad (21)$$

8.2.2.5 Current Loop

The gain of the power stage is:

$$G_{ID}(s) = (V_{OUT} \times R_{SENSE}) / (s \times L_{BOOST} \times V_P) \quad (22)$$

R_{SENSE} has been chosen to give the desired differential voltage for the current sense amplifier at the desired current limit point. In this example, a current limit of 4 A and a reasonable differential voltage to the current amp of 1 V gives a R_{SENSE} value of 0.25 Ω. V_P in this equation is the voltage swing of the oscillator ramp, 4 V for the UCC3817. Setting the crossover frequency of the system to 1/10th of the switching frequency, or 10 kHz, requires a power stage gain at that frequency of 0.383. For the system to have a gain of 1 at the crossover frequency, the current amplifier must have a gain of $1/G_{ID}$ at that frequency. G_{EA}, the current amplifier gain is then:

$$G_{EA} = (1/G_{ID}) = (1/0.383) = 2.611 \quad (23)$$

R_I is the R_{MOUT} resistor, previously calculated to be 3.9 kΩ. (refer to Figure 11). The gain of the current amplifier is R_f/R_I, so multiplying R_I by G_{EA} gives the value of R_f,which in this case is approximately 12 kΩ. Setting a zero at the crossover frequency and a pole at half the switching frequency completes the current loop compensation.

$$C_Z = 1 / (2 \times \pi \times R_f \times f_C) \quad (24)$$

$$C_P = 1 / (2 \times \pi \times R_f \times f_S/2) \quad (25)$$

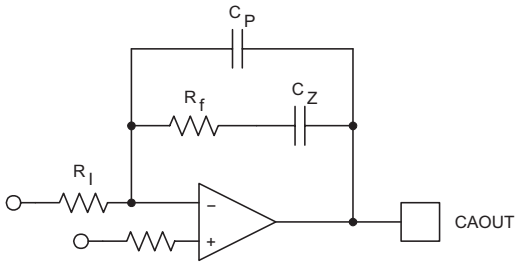

Figure 11. Current Loop Compensation

The UCC3817 current amplifier has the input from the multiplier applied to the inverting input. This change in architecture from previous Texas Instruments PFC controllers improves noise immunity in the current amplifier and adds a phase inversion into the control loop. The UCC3817 takes advantage of this phase inversion to implement leading-edge duty cycle modulation. Synchronizing a boost PFC controller to a downstream dc-to-dc controller reduces the ripple current seen by the bulk capacitor between stages, reducing capacitor size and cost and reducing EMI. This is explained in greater detail in *Capacitor Ripple Reduction*. The UCC3817 current amplifier configuration is shown in Figure 12.

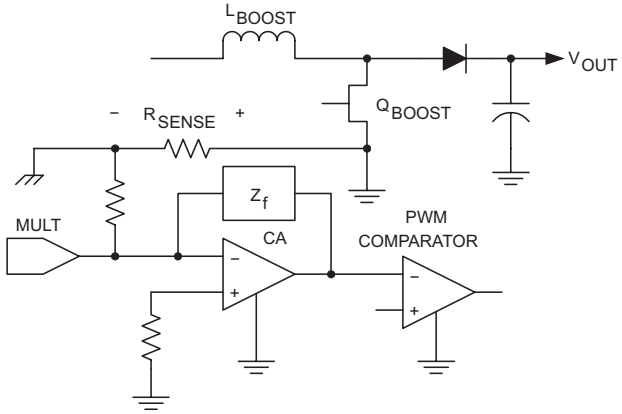

Figure 12. UCC3817 Current Amplifier Configuration

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8.2.2.6 Start Up

The UCC3818 version of the device is intended to have VCC connected to a 12-V supply voltage. The UCC3817 has an internal shunt regulator, enabling the device to be powered from bootstrap circuitry as shown in Figure 9. The current drawn by the UCC3817 during undervoltage lockout, or start-up current, is typically 150 μA. Once VCC is above the UVLO threshold, the device is enabled and draws 4 mA typically. A resistor connected between the rectified ac line voltage and the VCC pin provides current to the shunt regulator during power up. Once the circuit is operational, the bootstrap winding of the inductor provides the VCC voltage. Sizing of the start-up resistor is determined by the start-up time requirement of the system design.

$$I_C = C(\Delta V/\Delta t) \quad (26)$$

$$R = (V_{RMS} \times 0.9) / I_C$$

where

- I_C is the charge current
- C is the total capacitance at the VCC pin
- ΔV is the UVLO threshold
- Δt is the allowed start-up time (27)

Assuming a 1 second allowed start-up time, a 16-V VCC turn-on threshold, and a total VCC capacitance of 100 μF, a resistor value of 51 kΩ is required at a low line input voltage of 85 V_{RMS}. The IC start-up current is sufficiently small as to be ignored in sizing the start-up resistor.

8.2.3 Application Curves

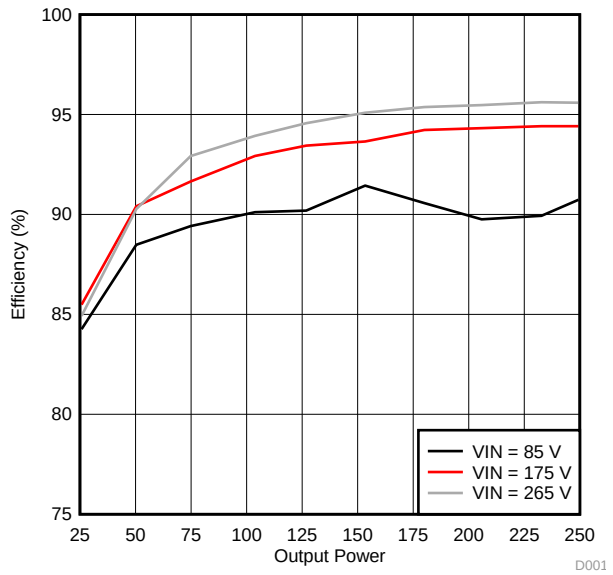

Figure 13. Efficiency vs Output Power

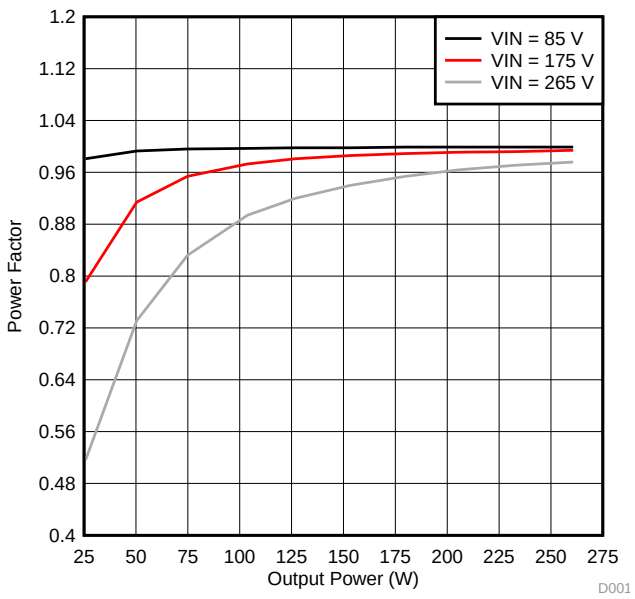

Figure 14. Power Factor vs Output Power

9 Power Supply Recommendations

9.1 Power Switch Selection

As in any power supply design, tradeoffs between performance, cost, and size must be made. When selecting a power switch, calculate the total power dissipation in the switch for several different devices at the switching frequencies being considered for the converter. Total power dissipation in the switch is the sum of switching loss and conduction loss. Switching losses are the combination of the gate charge loss, C_{OSS} loss and turnon and turnoff losses:

$$P_{GATE} = Q_{GATE} \times V_{GATE} \times f_S \quad (28)$$

$$P_{COSS} = 1/2 \times C_{OSS} \times V^2_{OFF} \times f_S \quad (29)$$

$$P_{ON} + P_{OFF} = 1/2 \times V_{OFF} \times I_L \times (t_{ON} + t_{OFF}) \times f_S$$

where

- Q_{GATE} is the total gate charge
- V_{GATE} is the gate drive voltage
- f_S is the clock frequency
- C_{OSS} is the drain source capacitance of the MOSFET
- I_L is the peak inductor current
- t_{ON} and t_{OFF} are the switching times (estimated using device parameters R_{GATE}, Q_{GD} and V_{TH})
- V_{OFF} is the voltage across the switch during the off time; in this case $V_{OFF} = V_{OUT}$ (30)

Conduction loss is calculated as the product of the $R_{DS(on)}$ of the switch (at the worst case junction temperature) and the square of RMS current:

$$P_{COND} = R_{DS(on)} \times K \times I^2_{RMS}$$

where

- K is the temperature factor found in the manufacturer's $R_{DS(on)}$ vs. junction temperature curves (31)

Calculating these losses and plotting against frequency gives a curve that enables the designer to determine either which device has the best performance at the desired switching frequency, or which switching frequency has the least total loss for a particular power switch. For the design example in Figure 9, an IRFP450 HEXFET from International Rectifier was chosen because of its low $R_{DS(on)}$ and its V_{DSS} rating. The IRFP450 $R_{DS(on)}$ of 0.4 Ω and the maximum V_{DSS} of 500 V made it an ideal choice. An excellent review of this procedure can be found in the Unitrode Power Supply Design Seminar SEM1200, Topic 6, Design Review: 140 W, [Multiple Output High Density DC/DC Converter].

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10 Layout

10.1 Layout Guidelines

10.1.1 Capacitor Ripple Reduction

For a power system where the PFC boost converter is followed by a dc-to-dc converter stage, it can be beneficial to synchronize the two converters. In addition to the usual advantages such as noise reduction and stability, proper synchronization can significantly reduce the ripple currents in the output capacitor of the boost circuit. Figure 15 helps illustrate the impact of proper synchronization, by showing a PFC boost converter together with the simplified input stage of a forward converter.

The capacitor current during a single switching cycle depends on the status of the switches Q1 and Q2, and is shown in Figure 16. With a synchronization scheme that maintains conventional trailing-edge modulation on both converters, the capacitor current ripple is highest. The greatest ripple current cancellation is attained when the overlap of Q1 offtime and Q2 ontime is maximized. One method of achieving this is to synchronize the turnon of the boost diode (D1) with the turnon of Q2. This approach implies that the leading edge of the boost converter is pulse-width modulated, while the forward converter is modulated with traditional trailing-edge PWM. The UCC3817 is designed as a leading-edge modulator with easy synchronization to the downstream converter to facilitate this advantage. Table 2 compares the $I_{CB(rms)}$ for D1/Q2 synchronization as offered by UCC3817 versus the $I_{CB(rms)}$ for the other extreme of synchronizing the turnon of Q1 and Q2 for a 200-W power system with a V_{BST} of 385 V.

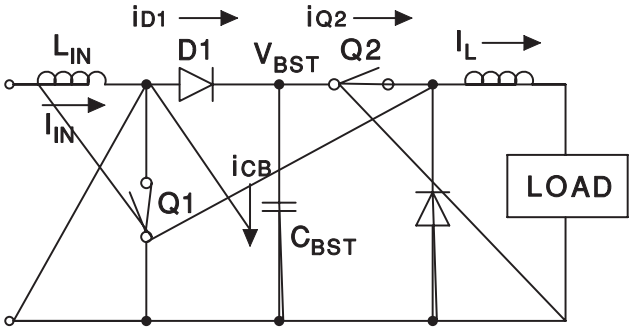

Figure 15. Simplified Representation of a 2-Stage PFC Power Supply

Layout Guidelines (continued)

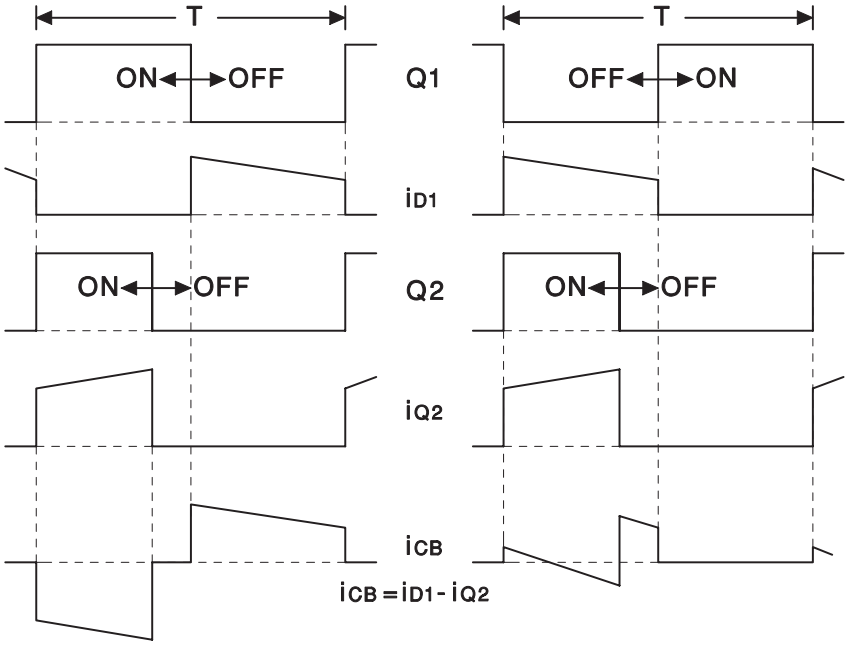

Figure 16. Timing Waveforms for Synchronization Scheme

Table 2. Effects of Synchronization on Boost Capacitor Current

	V_{IN} = 85 V		V_{IN} = 120 V		V_{IN} = 240 V	
D(Q2)	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2	Q1/Q2	D1/Q2
0.35	1.491 A	0.835 A	1.341 A	0.663 A	1.024 A	0.731 A
0.45	1.432 A	0.93 A	1.276 A	0.664 A	0.897 A	0.614 A

Table 2 illustrates that the boost capacitor ripple current can be reduced by approximately 50% at nominal line, and about 30% at high line with the synchronization scheme facilitated by the UCC3817. Figure 17 shows the suggested technique for synchronizing the UCC3817 to the downstream converter. With this technique, maximum ripple reduction as shown in Figure 16 is achievable. The output capacitance value can be significantly reduced if its choice is dictated by ripple current, or the capacitor life can be increased as a result. In cost-sensitive designs where holdup time is not critical, this is a significant advantage.

An alternative method of synchronization makes it possible to achieve the same ripple reduction. In this method, the turnon of Q1 is synchronized to the turnoff of Q2. While this method yields almost identical ripple reduction and maintains trailing edge modulation on both converters, the synchronization is more difficult to achieve, and the circuit can become susceptible to noise as the synchronizing edge itself is being modulated.

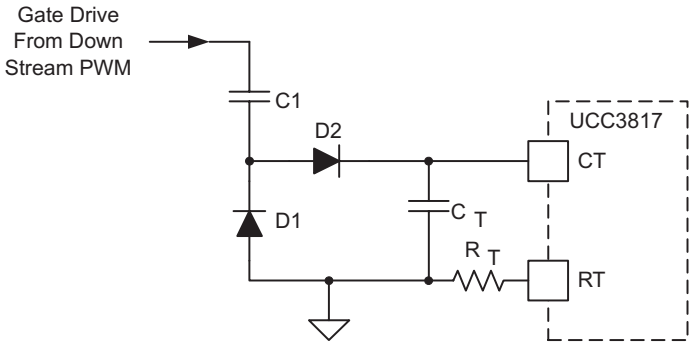

Figure 17. Synchronizing the UCC3817 to a Down-Stream Converter

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10.2 Layout Example

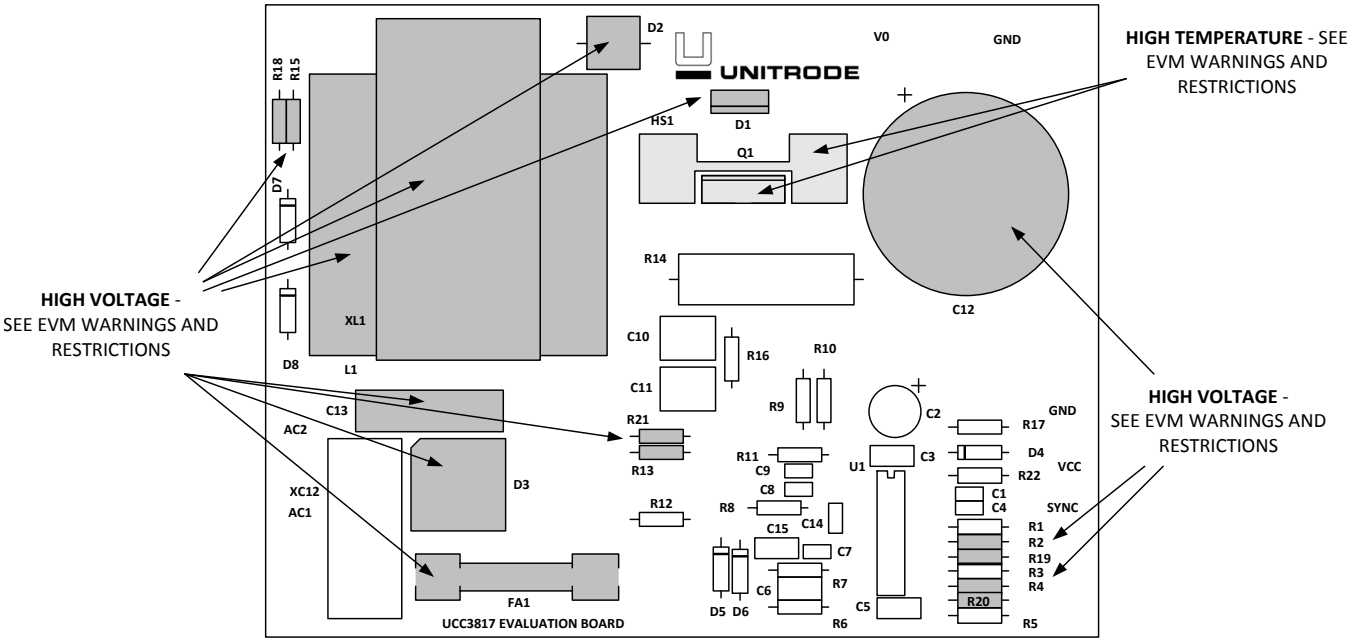

Figure 18. UCC3817EVM Evaluation Board Layout Assembly

11 Device and Documentation Support

11.1 Documentation Support

11.1.1 Related Documentation

For related documentation see the following:

1. *Differences Between UCC3817A/18A/19A and UCC3817/18/19* (SLUA294)
2. *UCC3817 BiCMOS Power Factor Preregulator Evaluation Board* (SLUU077)
3. *Synchronizing a PFC Controller from a Down Stream Controller Gate Drive* (SLUA245)
4. Seminar topic, *High Power Factor Switching Preregulator Design Optimization*, L.H. Dixon, SEM-700,1990.
5. Seminar topic, *High Power Factor Preregulator for Off-line Supplies*, L.H. Dixon, SEM-600, 1988.

11.2 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 3. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC2817	Click here	Click here	Click here	Click here	Click here
UCC2818	Click here	Click here	Click here	Click here	Click here
UC3817	Click here	Click here	Click here	Click here	Click here
UC3818	Click here	Click here	Click here	Click here	Click here

11.3 Receiving Notification of Documentation Updates

To receive notification of documentation updates, navigate to the device product folder on ti.com. In the upper right corner, click on *Alert me* to register and receive a weekly digest of any product information that has changed. For change details, review the revision history included in any revised document.

11.4 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.5 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.6 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.7 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

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12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

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PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2817D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2817D	Samples
UCC2817DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2817D	Samples
UCC2817DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2817DW	Samples
UCC2817N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2817N	Samples
UCC2818D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2818D	Samples
UCC2818DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	UCC2818D	Samples
UCC2818DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2818DW	Samples
UCC2818DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	UCC2818DW	Samples
UCC2818N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	-40 to 85	UCC2818N	Samples
UCC2818PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	-40 to 85	2818PW	Samples
UCC3817D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3817D	Samples
UCC3817DG4	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3817D	Samples
UCC3817DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3817D	Samples
UCC3817DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3817DW	Samples
UCC3817DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3817DW	Samples
UCC3817N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3817N	Samples
UCC3817NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3817N	Samples

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC3818D	ACTIVE	SOIC	D	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3818D	Samples
UCC3818DTR	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3818D	Samples
UCC3818DTRG4	ACTIVE	SOIC	D	16	2500	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	UCC3818D	Samples
UCC3818DW	ACTIVE	SOIC	DW	16	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3818DW	Samples
UCC3818DWTR	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3818DW	Samples
UCC3818DWTRG4	ACTIVE	SOIC	DW	16	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	UCC3818DW	Samples
UCC3818N	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3818N	Samples
UCC3818NG4	ACTIVE	PDIP	N	16	25	Green (RoHS & no Sb/Br)	CU NIPDAU	N / A for Pkg Type	0 to 70	UCC3818N	Samples
UCC3818PW	ACTIVE	TSSOP	PW	16	90	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR	0 to 70	3818PW	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

OTHER QUALIFIED VERSIONS OF UCC2818 :

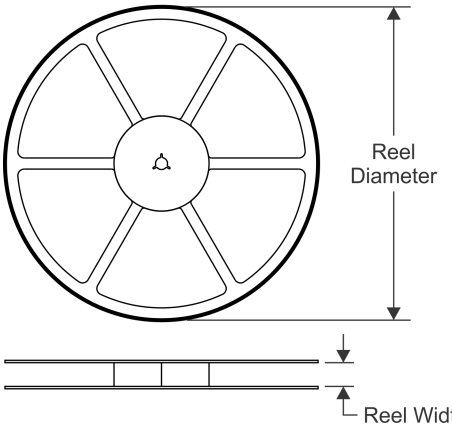
- Enhanced Product: UCC2818-EP

NOTE: Qualified Version Definitions:

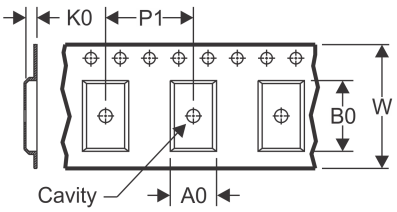
- Enhanced Product - Supports Defense, Aerospace and Medical Applications

TAPE AND REEL INFORMATION

REEL DIMENSIONS

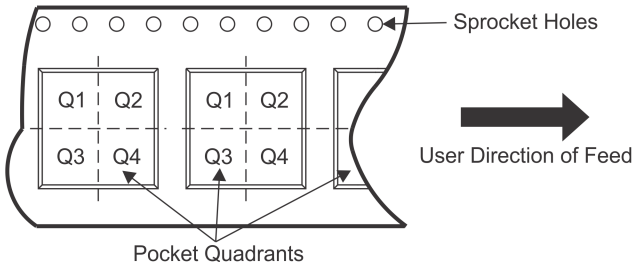


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

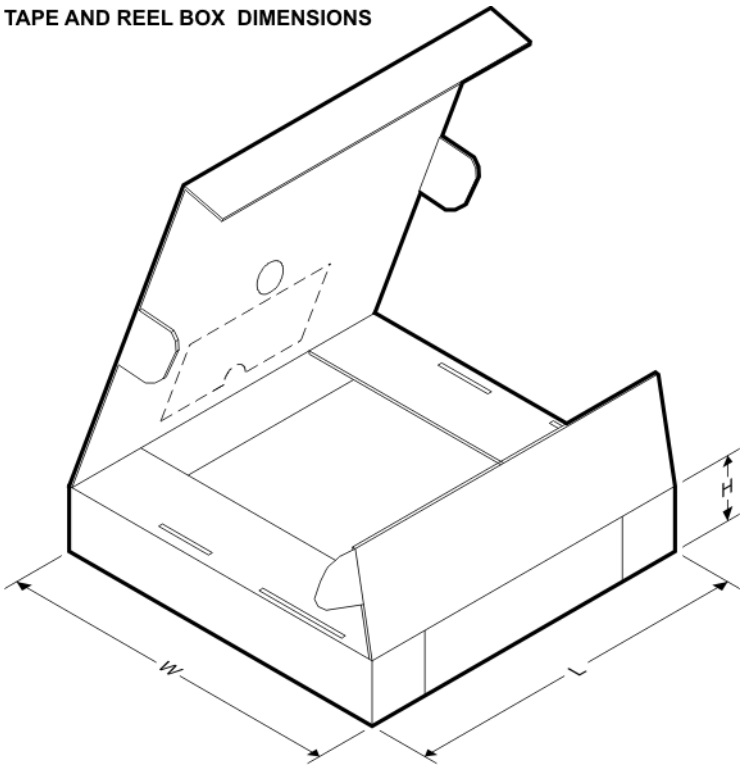
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2817DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC2818DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC2818DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UCC3817DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC3817DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1
UCC3818DTR	SOIC	D	16	2500	330.0	16.4	6.5	10.3	2.1	8.0	16.0	Q1
UCC3818DWTR	SOIC	DW	16	2000	330.0	16.4	10.75	10.7	2.7	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2817DTR	SOIC	D	16	2500	333.2	345.9	28.6
UCC2818DTR	SOIC	D	16	2500	333.2	345.9	28.6
UCC2818DWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UCC3817DTR	SOIC	D	16	2500	333.2	345.9	28.6
UCC3817DWTR	SOIC	DW	16	2000	367.0	367.0	38.0
UCC3818DTR	SOIC	D	16	2500	333.2	345.9	28.6
UCC3818DWTR	SOIC	DW	16	2000	367.0	367.0	38.0

GENERIC PACKAGE VIEW

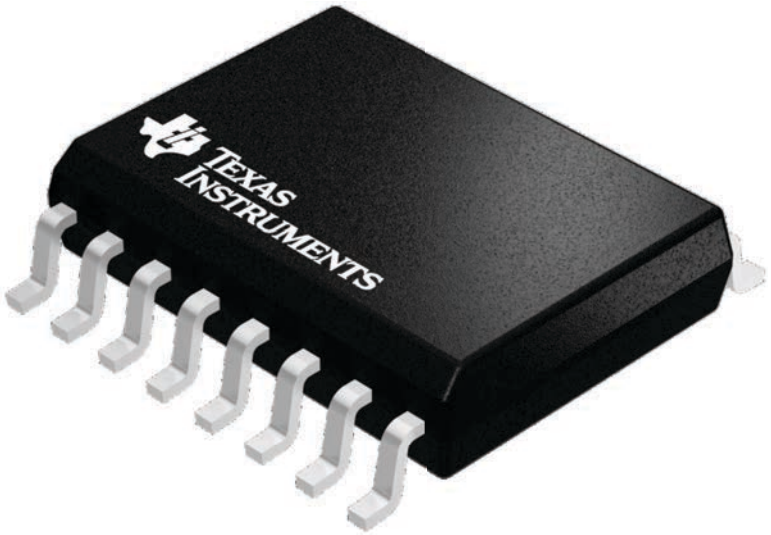
DW 16

SOIC - 2.65 mm max height

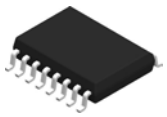
7.5 x 10.3, 1.27 mm pitch

SMALL OUTLINE INTEGRATED CIRCUIT

This image is a representation of the package family, actual package may vary.
Refer to the product data sheet for package details.



4224780/A

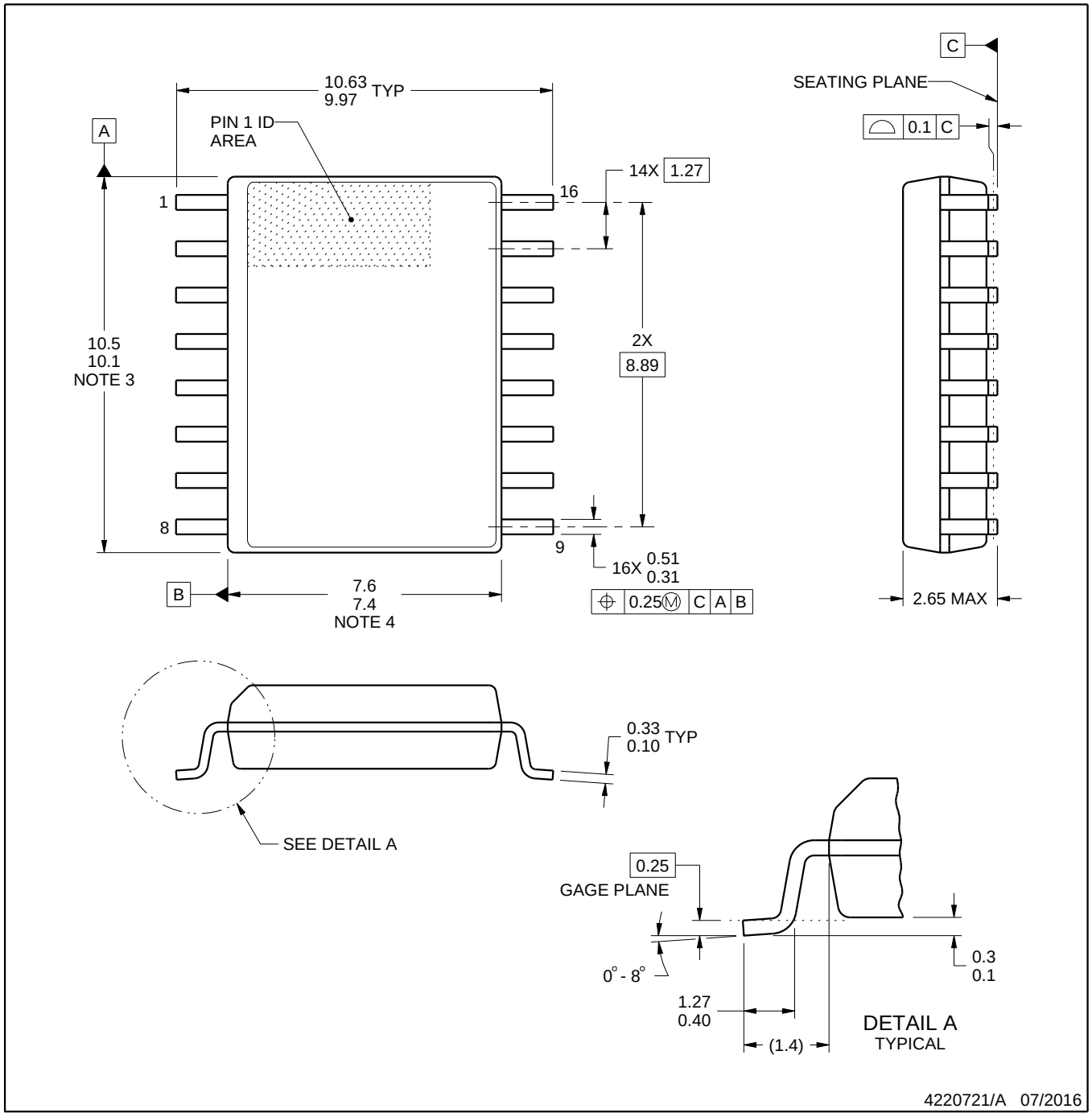


PACKAGE OUTLINE

DW0016A

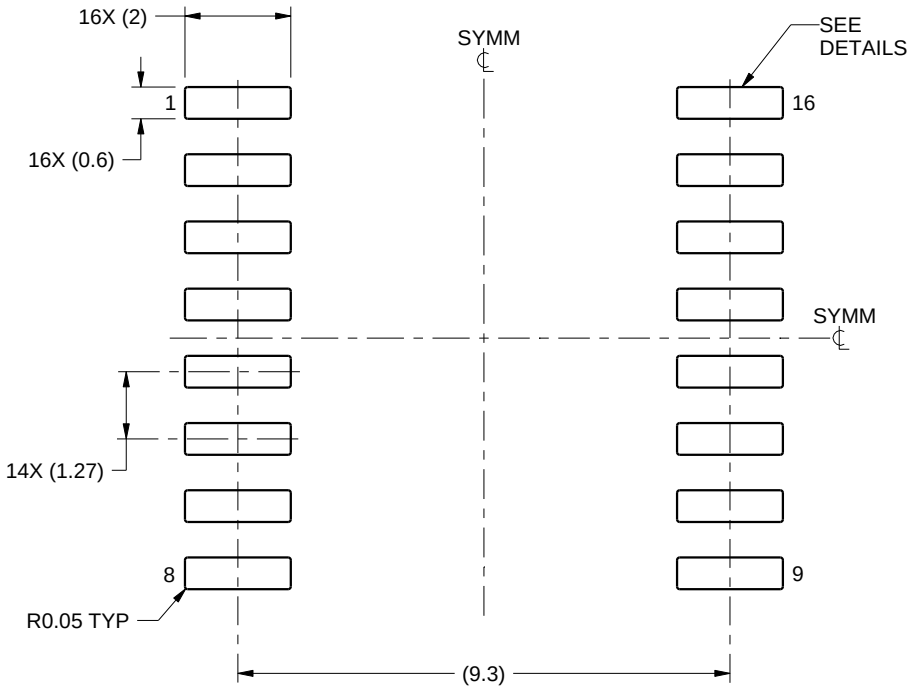
SOIC - 2.65 mm max height

SOIC

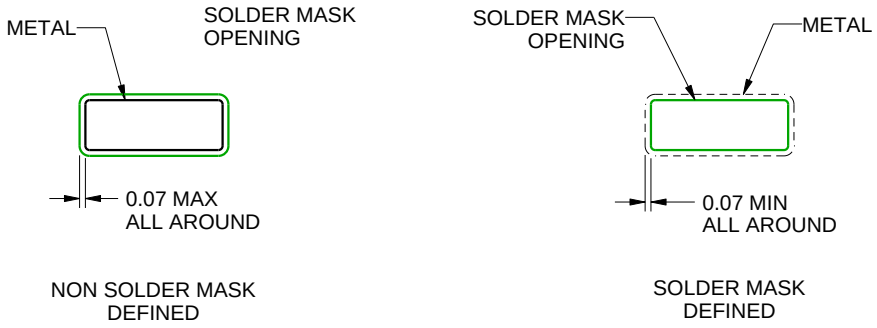


NOTES:

1. All linear dimensions are in millimeters. Dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm, per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm, per side.
5. Reference JEDEC registration MS-013.



LAND PATTERN EXAMPLE
SCALE:7X

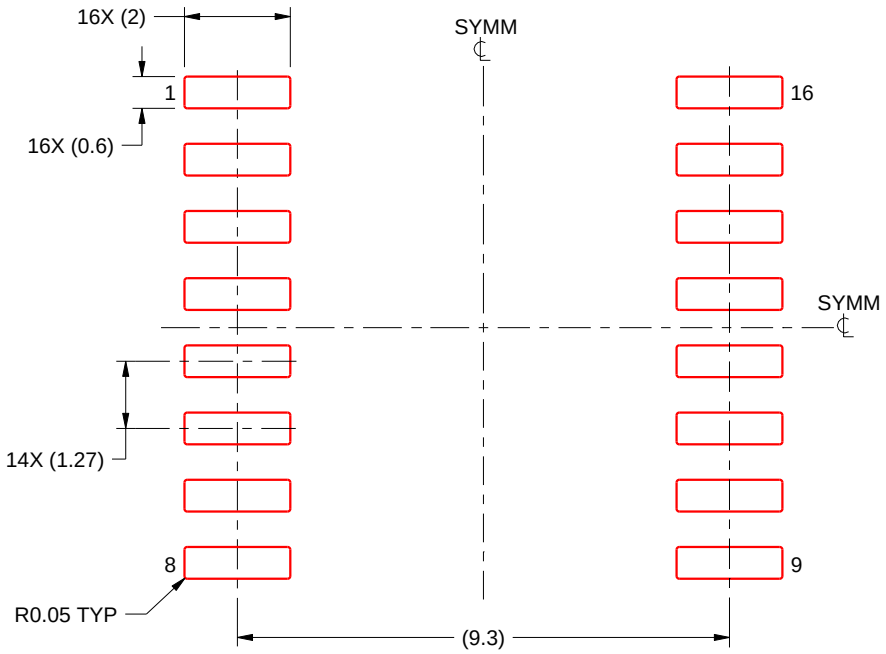


SOLDER MASK DETAILS

4220721/A 07/2016

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:7X

4220721/A 07/2016

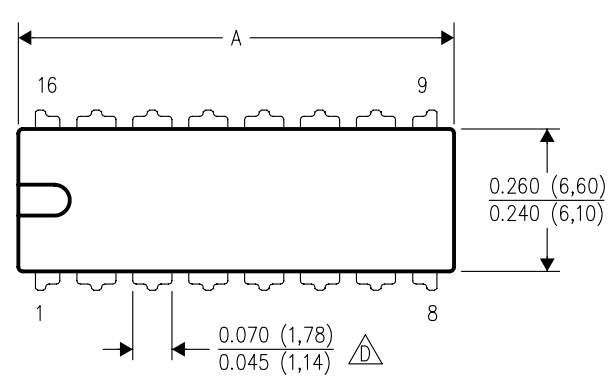
NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

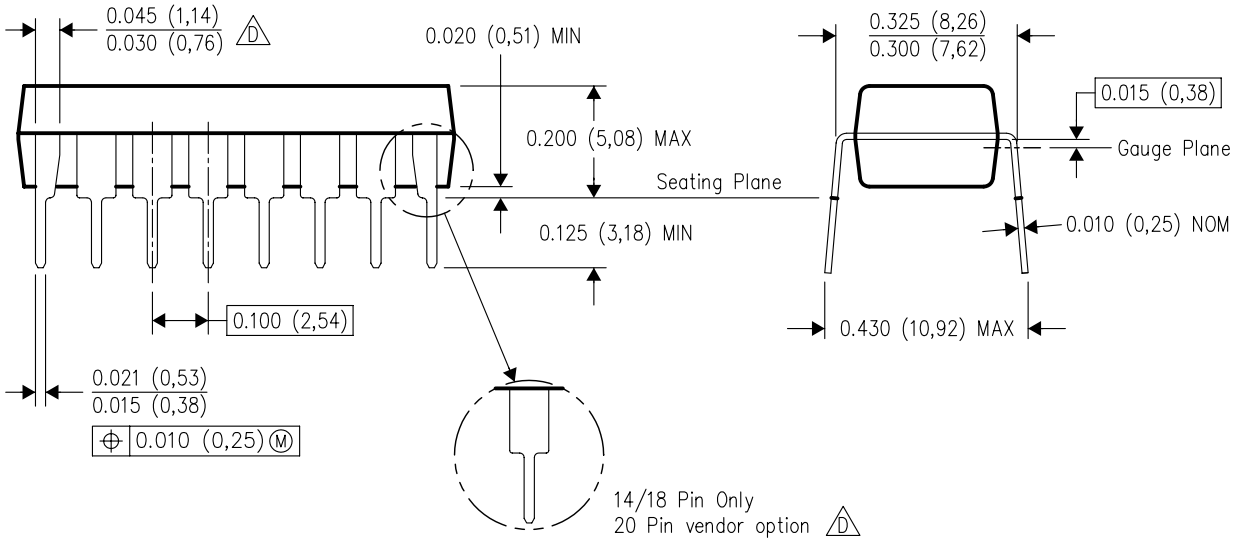
N (R–PDIP–T**)

PLASTIC DUAL–IN–LINE PACKAGE

16 PINS SHOWN



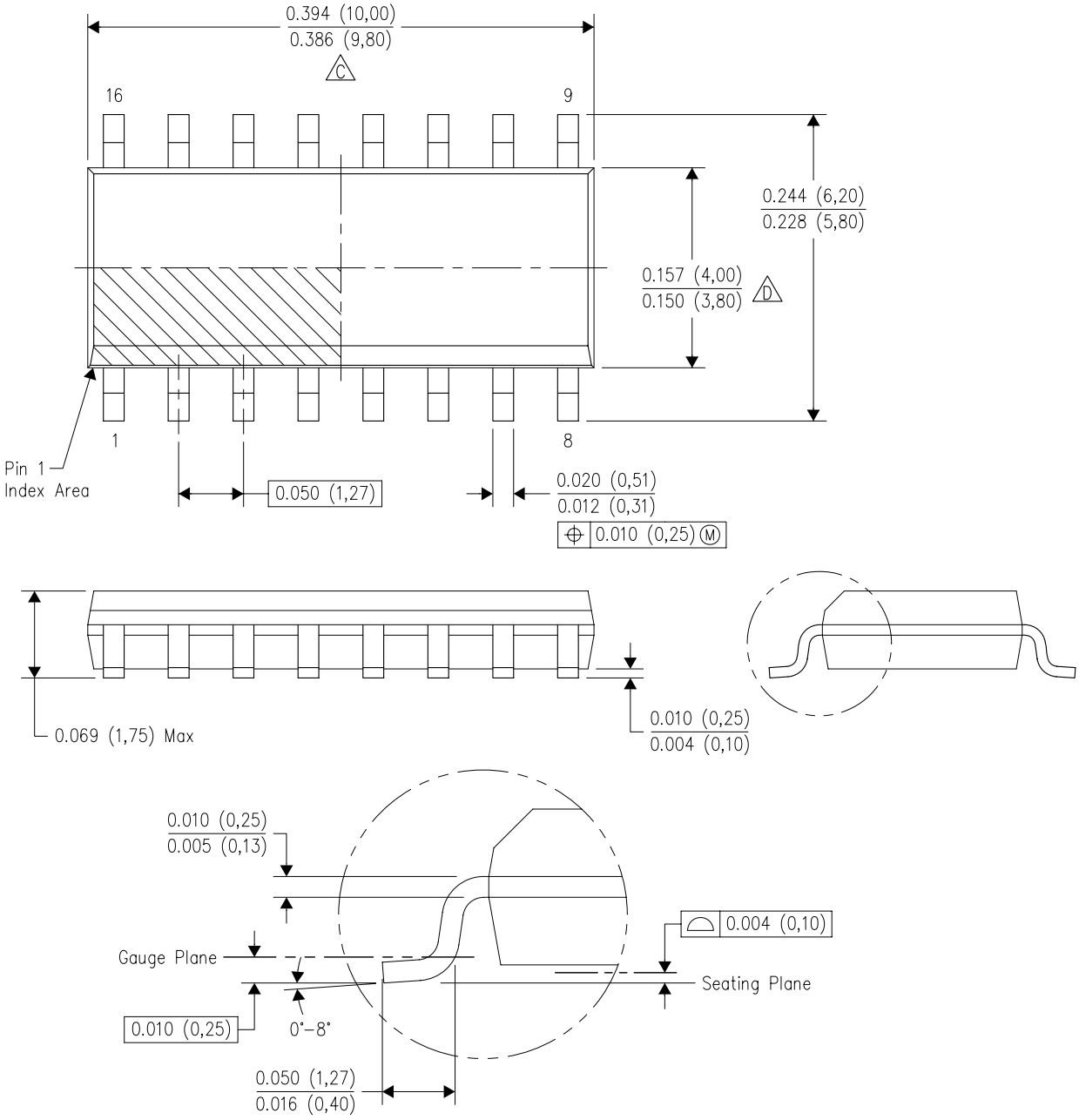
DIM \ PINS **	14	16	18	20
A MAX	0.775 (19,69)	0.775 (19,69)	0.920 (23,37)	1.060 (26,92)
A MIN	0.745 (18,92)	0.745 (18,92)	0.850 (21,59)	0.940 (23,88)
MS–001 VARIATION (C)	AA	BB	AC	AD



4040049/E 12/2002

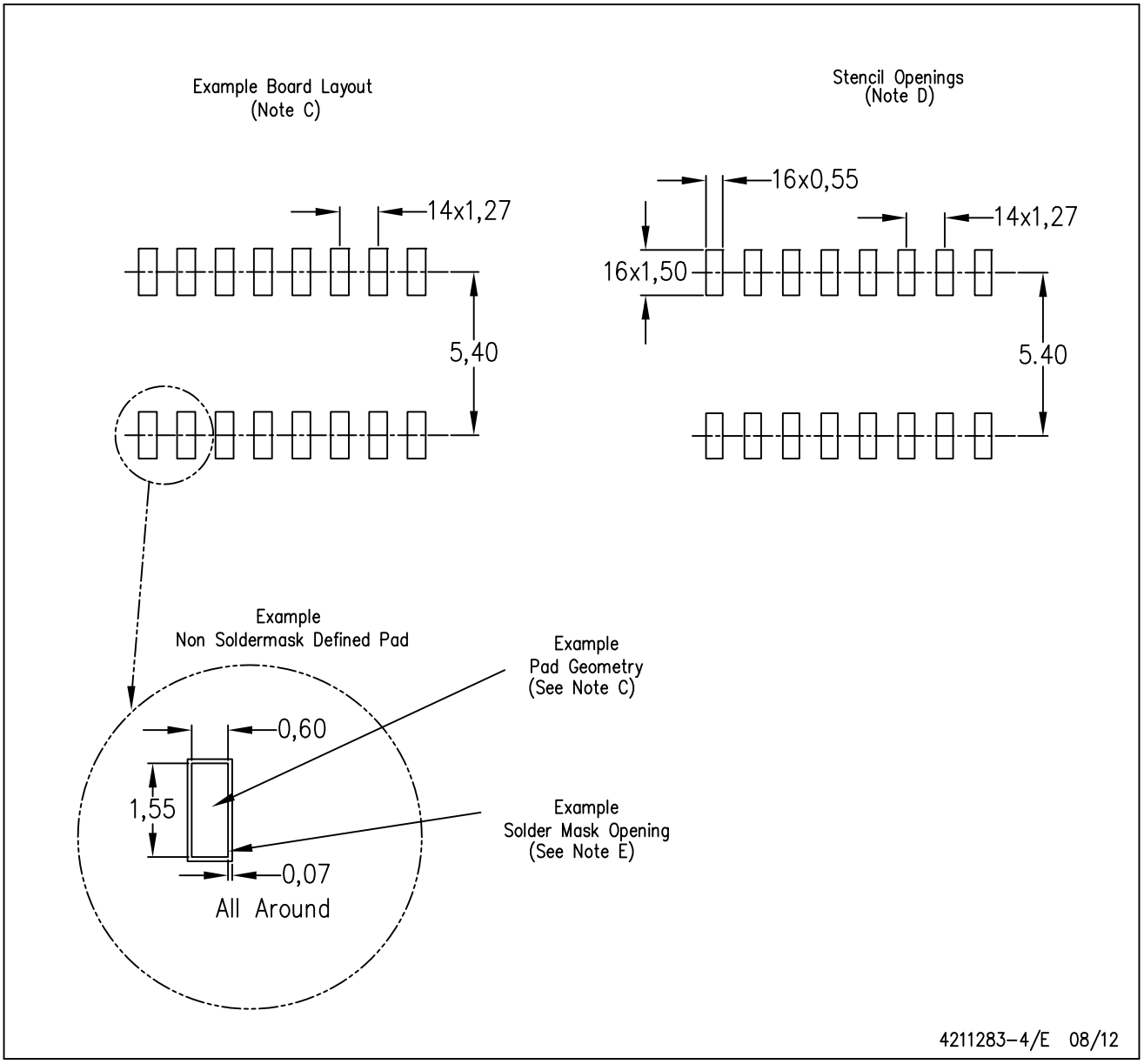
NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Falls within JEDEC MS–001, except 18 and 20 pin minimum body length (Dim A).
D. The 20 pin end lead shoulder width is a vendor option, either half or full width.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



NOTES:
A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.006 (0,15) each side.
D. Body width does not include interlead flash. Interlead flash shall not exceed 0.017 (0,43) each side.
E. Reference JEDEC MS–012 variation AC.

D (R–PDSO–G16) PLASTIC SMALL OUTLINE



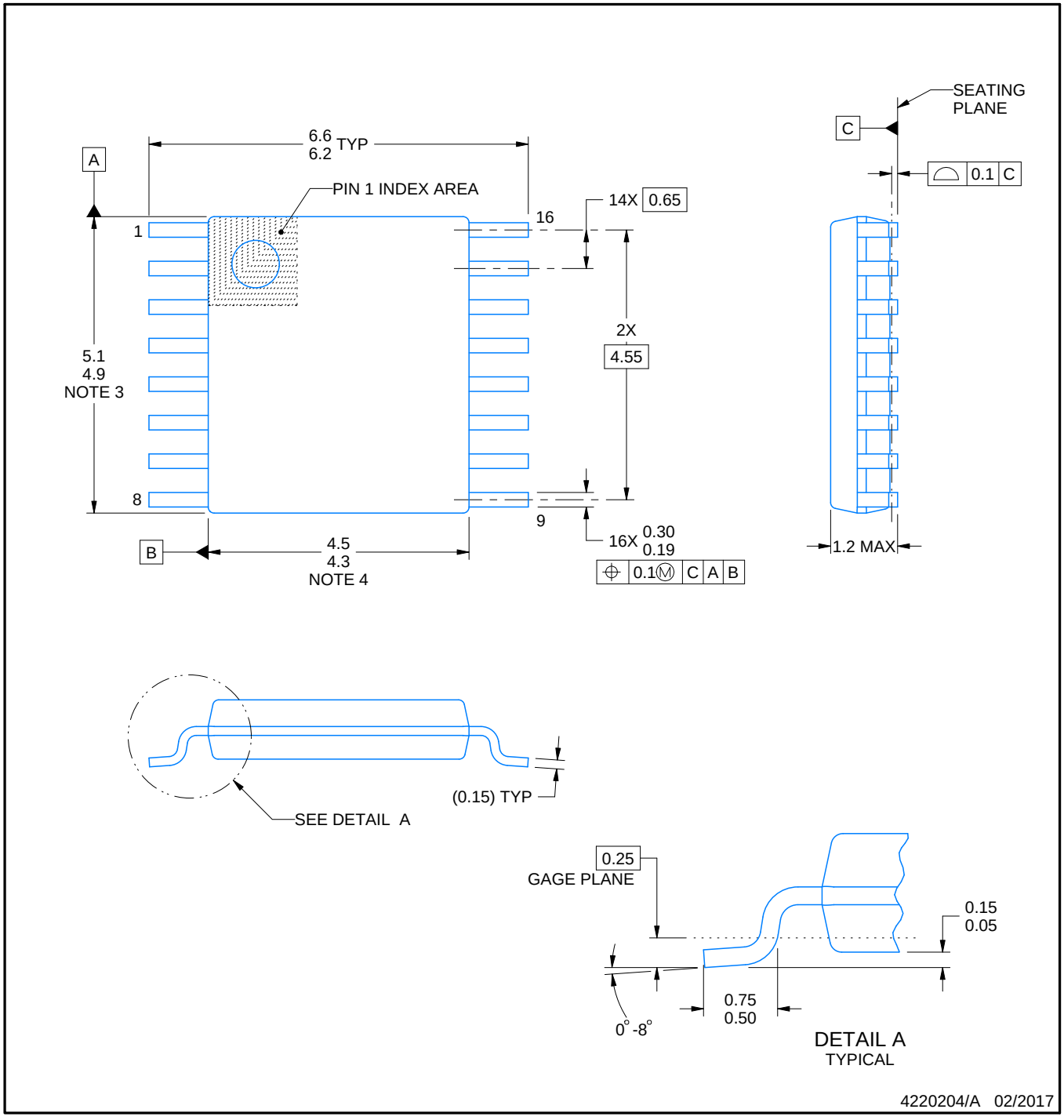
NOTES:
A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Publication IPC–7351 is recommended for alternate designs.
D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525 for other stencil recommendations.
E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

PACKAGE OUTLINE

PW0016A

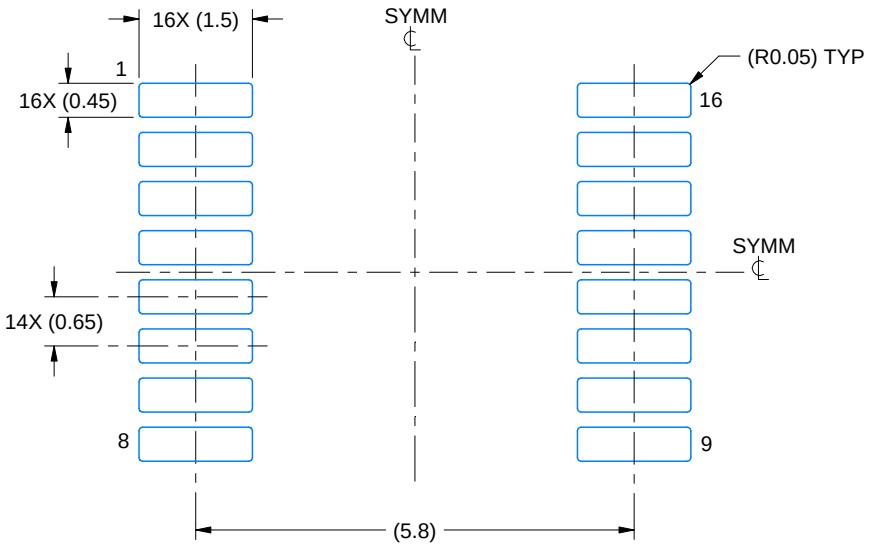
TSSOP - 1.2 mm max height

SMALL OUTLINE PACKAGE



NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
4. This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
5. Reference JEDEC registration MO-153.



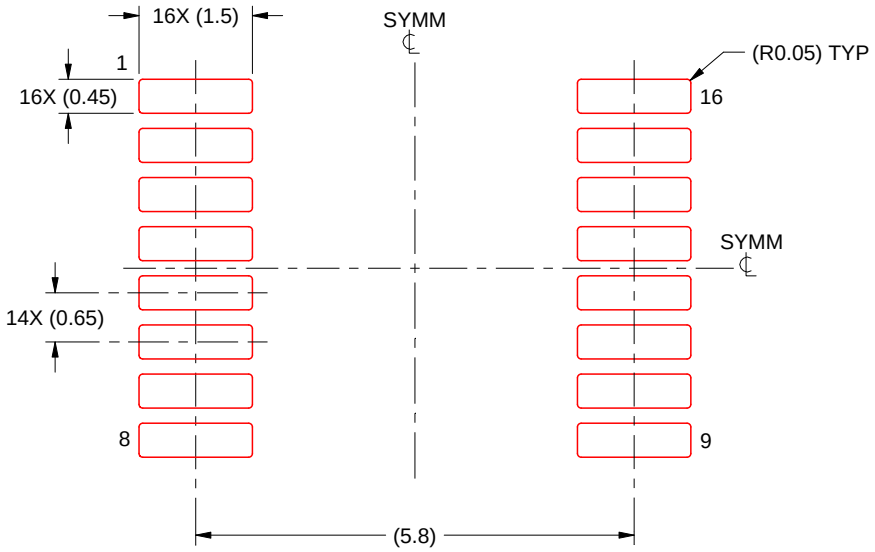
LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X

SOLDER MASK DETAILS

4220204/A 02/2017

NOTES: (continued)

6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE: 10X

4220204/A 02/2017

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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