THE DATASHEET OF

UCC3808DTR-2

UCCx808-x Low Power Current Mode Push-Pull PWM

1 Features

- Dual Output Drive Stages in Push-Pull Configuration
- 130-µA Typical Starting Current
- 1-mA Typical Run Current
- Operation to 1-MHz
- Internal Soft-Start
- On-Chip Error Amplifier With 2-MHz Gain Bandwidth Product
- On-Chip VDD Clamping
- Output Drive Stages Capable Of 500-mA Peak Source Current, 1-A Peak Sink Current

2 Applications

- Server and Desktop Power Supplies
- Telecom Power Supplies
- DC-DC Converters
- Switched-Mode Power Supplies

3 Description

The UCCx808-x is a family of BiCMOS push-pull, high-speed, low-power, pulse-width modulators. The UCCx808 contains all of the control and drive circuitry required for offline or DC-to-DC fixed frequency current-mode switching power supplies with minimal external parts count.

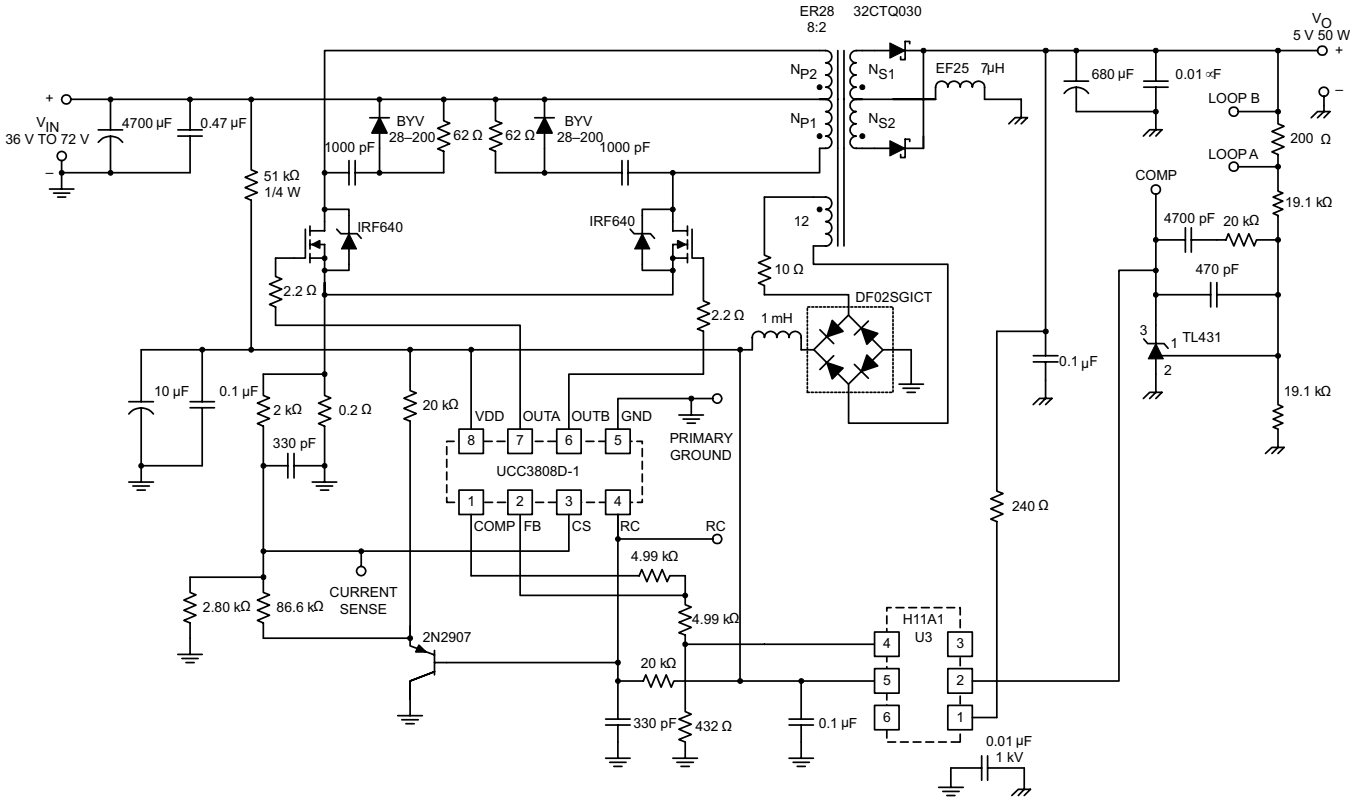
The UCCx808-x dual output drive stages are arranged in a push-pull configuration. Both outputs switch at half the oscillator frequency using a toggle flip-flop. The dead time between the two outputs is typically 60 ns to 200 ns depending on the values of the timing capacitor and resistors, thus limiting each output stage duty cycle to less than 50%.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
UCC2808-1 UCC2808-2 UCC3808-1 UCC3808-2	SOIC (8)	4.90 mm × 3.91 mm
	PDIP (8)	9.81 mm × 6.35 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic



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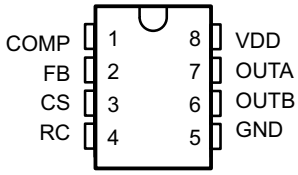
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision D (August 2002) to Revision E	Page
• Removed references to the TSSOP packaging	1
• Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section.	1

5 Pin Configuration and Functions

D Package
8-Pin SOIC
Top View



P Package
8-Pin PDIP
Top View

Pin Functions

PIN		I/O	DESCRIPTION
NAME	NO.		
COMP	1	I/O	Output of the error amplifier and the input of the PWM comparator.
CS	3	I	Input to the PWM, peak current, and overcurrent comparators.
FB	2	I	Inverting input to the error amplifier.
GND	5	—	Reference ground and power ground for all functions.
OUTA	7	O	Alternating high current output stage.
OUTB	6	O	Alternating high current output stage.
RC	4	I	Oscillator programming pin.
VDD	8	—	Power input connection for this device.

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

		MIN	MAX	UNIT
	Supply voltage (IDD ≤ 10 mA)		15	V
	Supply current		20	mA
	OUTA/OUTB source current (peak)(2)	–0.5		A
	OUTA/OUTB sink current (peak)(2)		1.0	A
	Analog inputs (FB, CS) – 0.3 V to VDD+0.3 V		6	V
	Power dissipation at T_A = 25 ° C (N Package)		1	W
	Power dissipation at T A = 25 ° C (D Package)		650	mW
	Power dissipation at T A = 25 ° C (PW Package)		400	mW
T_J	Junction temperature	–55	150	°C
	Lead temperature (soldering, 10 sec.)		300	°C
T_{stg}	Storage temperature	–65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Currents are positive into, negative out of the specified terminal. Consult Packaging Section of the Power Supply Control Data Book (SLUD003) for thermal limitations and considerations of packages.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±2500	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

			MIN	MAX	UNIT
V_{DD}	Supply Voltage	UCCx808-1	13	14	V
		UCCx808-2	5	14	
T_J	Junction Temperature	UCC2808-x	–40	85	°C
		UCC3808-x	0	70	

6.4 Electrical Characteristics

T_A = 0°C to 70°C for the UCC3808-x, –40°C to 85°C for the UCC2808-x and –55°C to 125°C for the UCC1808-x, VDD = 10 V(1), 1-µF capacitor from VDD to GND, R = 22 kΩ , C = 330 pF, $T_A = T_J$, (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
OSCILLATOR SECTION					
Oscillator frequency		175	194	213	kHz
Oscillator amplitude/VDD(2)		0.44	0.5	0.56	V/V
ERROR AMPLIFIER SECTION					
Input voltage	COMP = 2 V	1.95	2	2.05	V
Input bias current		–1		1	µ A
Open-loop voltage gain		60	80		dB
COMP sink current	FB = 2.2 V, COMP = 1 V	0.3	2.5		mA

(1) Does not include current in the external oscillator network.
(2) Measured at RC. Signal amplitude tracks VDD.

Electrical Characteristics (continued)

T_A = 0°C to 70°C for the UCC3808-x, –40°C to 85°C for the UCC2808-x and –55°C to 125°C for the UCC1808-x, VDD = 10 V(1), 1-µF capacitor from VDD to GND, R = 22 kΩ , C = 330 pF, $T_A = T_J$, (unless otherwise specified)

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
COMP source current	FB = 1.3 V, COMP = 3.5 V	–0.25	–0.5		mA
PWM SECTION					
Maximum duty cycle	Measured at OUTA or OUTB	48%	49%	50%	
Minimum duty cycle	COMP = 0 V			0%	
CURRENT SENSE SECTION					
Gain(3)		1.9	2.2	2.5	V/V
Maximum input signal	COMP = 5 V (4)	0.45	0.5	0.55	V
CS to output delay	COMP = 3.5 V, CS from 0 to 600 mV		100	200	ns
CS source current		–200			nA
Over current threshold		0.7	0.75	0.8	V
COMP to CS offset	CS = 0 V	0.35	0.8	1.2	V
OUTPUT SECTION					
OUT low level	I = 100 mA		0.5	1	V
OUT high level	I = – 50 mA, VDD – OUT		0.5	1	V
Rise time	C_L = 1 nF		25	60	ns
Fall time	C_L = 1 nF		25	60	ns
UNDERVOLTAGE LOCKOUT SECTION					
Start threshold	UCCx808-1 (1)	11.5	12.5	13.5	V
	UCCx808-2	4.1	4.3	4.5	
Minimum operating voltage after start	UCCx808-1	7.6	8.3	9	V
	UCCx808-2	3.9	4.1	4.3	
Hysteresis	UCCx808-1	3.5	4.2	5.1	V
	UCCx808-2	0.1	0.2	0.3	
SOFT-START SECTION					
COMP rise time	FB = 1.8 V, rise from 0.5 V to 4 V		3.5	20	ms
OVERALL SECTION					
Start-up current	VDD < start threshold		130	260	µA
Operating supply current	FB = 0 V, CS = 0 V (5) (1)		1	2	mA
VDD zener shunt voltage	IDD = 10 mA (6)	13	14	15	V

$$A = \frac{\Delta V_{COMP}}{\Delta V_{CS}}, 0 \le V_{CS} \le 0.4V$$

(3) Gain is defined by: 0 v V_{CS} v 0.4 V
(4) Parameter measured at trip point of latch with FB at 0 V.
(5) For UCCx808 – 1, set VDD above the start threshold before setting at 10 V
(6) Start threshold and Zener shunt threshold track one another.

6.5 Typical Characteristics

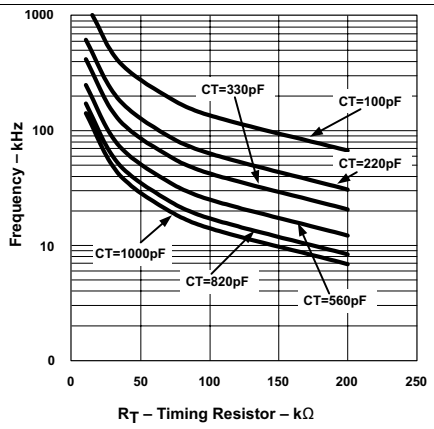


Figure 1. Frequency vs Timing Resistor

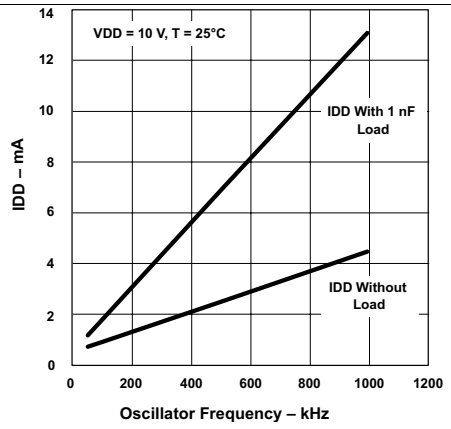


Figure 2. IDD vs Oscillator Frequency

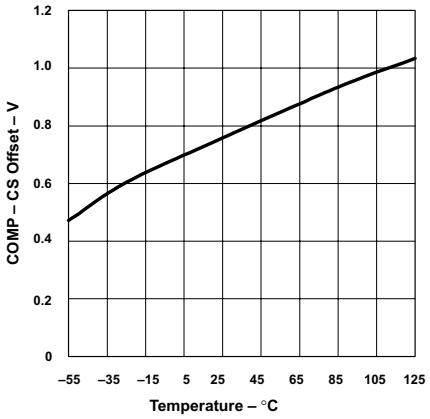


Figure 3. CS Offset vs Temperature

7 Detailed Description

7.1 Overview

The UCCx808-x device is a highly-integrated, low power current mode push-pull PWM controller. The controller employs low starting current, and employs an internal control algorithm that offers accurate static output voltage regulation against line and load. The UCCx808-x family offers a variety of package temperature range options, and choice of undervoltage lockout levels. The family has UVLO thresholds and hysteresis options for offline and battery-powered system.

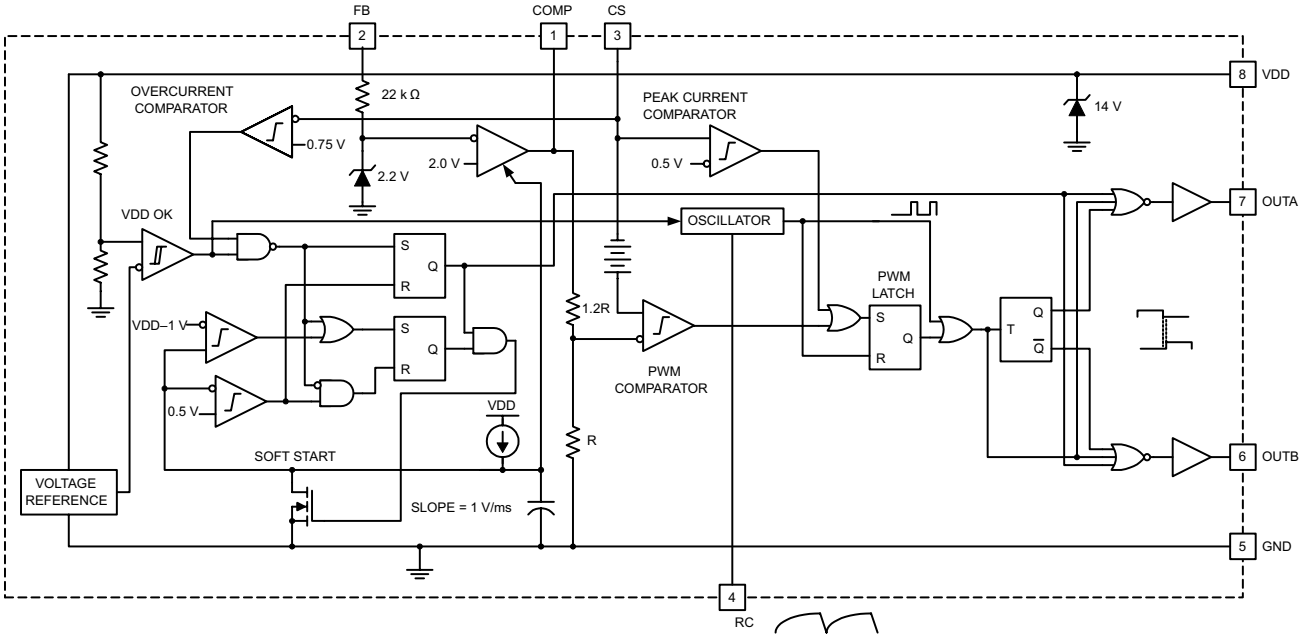
Table 1. Undervoltage Lockout Levels

PART NUMBER	TURN ON THRESHOLD	TURN OFF THRESHOLD
UCCx808-1	12.5 V	8.3 V
UCCx808-2	4.3 V	4.1 V

Table 2. Undervoltage Lockout Options

$T_A = T_J$	PACKAGED DEVICES		
	UVLO OPTION	SOIC (D)	PDIP (N)
–40°C to 85°C	12.5 V/8.3 V	UCC2808D-1	UCC2808N-1
	4.3 V/4.1 V	UCC2808D-2	UCC2808N-2
0°C to 70°C	12.5 V/8.3 V	UCC3808D-1	UCC3808N-1
	4.3 V/4.1 V	UCC3808D-2	UCC3808N-2

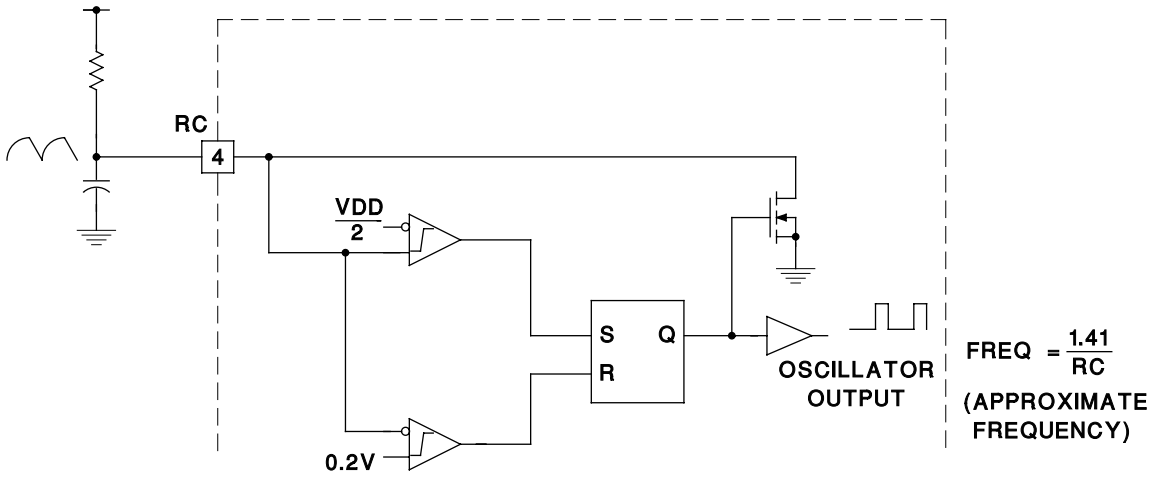
7.2 Functional Block Diagram



Pinout shown is for SOIC and PDIP packages.

Figure 4. Functional Block Diagram

Functional Block Diagram (continued)



The oscillator generates a sawtooth waveform on RC. During the RC rise time, the output stages alternate on time, but both stages are off during the RC fall time. The output stages switch at ½ the oscillator frequency, with guaranteed duty cycle of <50% for both outputs.

Figure 5. Block Diagram for Oscillator

7.3 Feature Description

7.3.1 Pin Descriptions

COMP: COMP is the output of the error amplifier and the input of the PWM comparator. The error amplifier in the UCC3808 is a true low-output impedance, 2-MHz operational amplifier. As such, the COMP pin can both source and sink current. However, the error amplifier is internally current limited, so that zero duty cycle can be externally forced by pulling COMP to GND.

The UCC3808 family features built-in full cycle soft-start. Soft-start is implemented as a clamp on the maximum COMP voltage.

CS: The input to the PWM, peak current, and overcurrent comparators. The overcurrent comparator is only intended for fault sensing. Exceeding the overcurrent threshold will cause a soft-start cycle.

FB: The inverting input to the error amplifier. For best stability, keep FB lead length as short as possible and FB stray capacitance as small as possible.

GND: Reference ground and power ground for all functions. Due to high currents, and high frequency operation of the UCC3808, a low impedance circuit board ground plane is highly recommended.

OUTA and OUTB: Alternating high current output stages. Both stages are capable of driving the gate of a power MOSFET. Each stage is capable of 500-mA peak source current, and 1-A peak sink current.

The output stages switch at half the oscillator frequency, in a push/pull configuration. When the voltage on the RC pin is rising, one of the two outputs is high, but during fall time, both outputs are off. This dead time between the two outputs, along with a slower output rise time than fall time, insures that the two outputs can not be on at the same time. This dead time is typically 60 ns to 200 ns and depends upon the values of the timing capacitor and resistor.

The high-current output drivers consist of MOSFET output devices, which switch from VDD to GND. Each output stage also provides a very low impedance to overshoot and undershoot. This means that in many cases, external schottky clamp diodes are not required.

RC: The oscillator programming pin. The oscillator of the UCC3808-x tracks VDD and GND internally, so that variations in power supply rails minimally affect frequency stability. Figure 5 shows the oscillator block diagram.

Only two components are required to program the oscillator: a resistor (tied to the VDD and RC), and a capacitor (tied to the RC and GND). The approximate oscillator frequency is determined by the simple formula:

Feature Description (continued)

$$f_{OSCILLATOR} = \frac{1.41}{RC}$$

where

- frequency is in hertz, resistance in ohms, and capacitance in farads. (1)

The recommended range of timing resistors is between 10 kΩ and 200 kΩ and range of timing capacitors is between 100 pF and 1000 pF. Timing resistors less than 10 kΩ must be avoided.

For best performance, keep the timing capacitor lead to GND as short as possible, the timing resistor lead from VDD as short as possible, and the leads between timing components and RC as short as possible. Separate ground and VDD traces to the external timing network are encouraged.

VDD: The power input connection for this device. Although quiescent VDD current is very low, total supply current will be higher, depending on OUTA and OUTB current, and the programmed oscillator frequency. Total VDD current is the sum of quiescent VDD current and the average OUT current. Knowing the operating frequency and the MOSFET gate charge (Qg), average OUT current can be calculated from:

$$I_{OUT} = Q_g F$$

where

- F is frequency To prevent noise problems, bypass VDD to GND with a ceramic capacitor as close to the chip as possible along with an electrolytic capacitor. (2)

A 1-µF decoupling capacitor is recommended.

7.4 Device Functional Modes

7.4.1 VCC

When VCC becomes above 12.5 V (for UCCx808-1) or 4.3 V (for UCCx808-2), the device is enable, and after all fault conditions are cleared, the gate driver starts with soft-start. When VCC drops below 8.3 V (for UCCx808-1) or 4.1 V (for UCCx808-2), the device enters the UVLO protection mode and both gate drivers are actively pulled low.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The UCCx808-x PWM controller contains all of the features needed to implement push-pull topology, using current-mode control in a small 8-pin package. The UCCx808-x is designed for current-mode control push-pull topology. UCCx808-x employs advantages of current-mode control, peak current sense, overcurrent protection.

8.2 Typical Application

A 200-kHz push-pull application circuit with a full wave rectifier is shown in Figure 6.

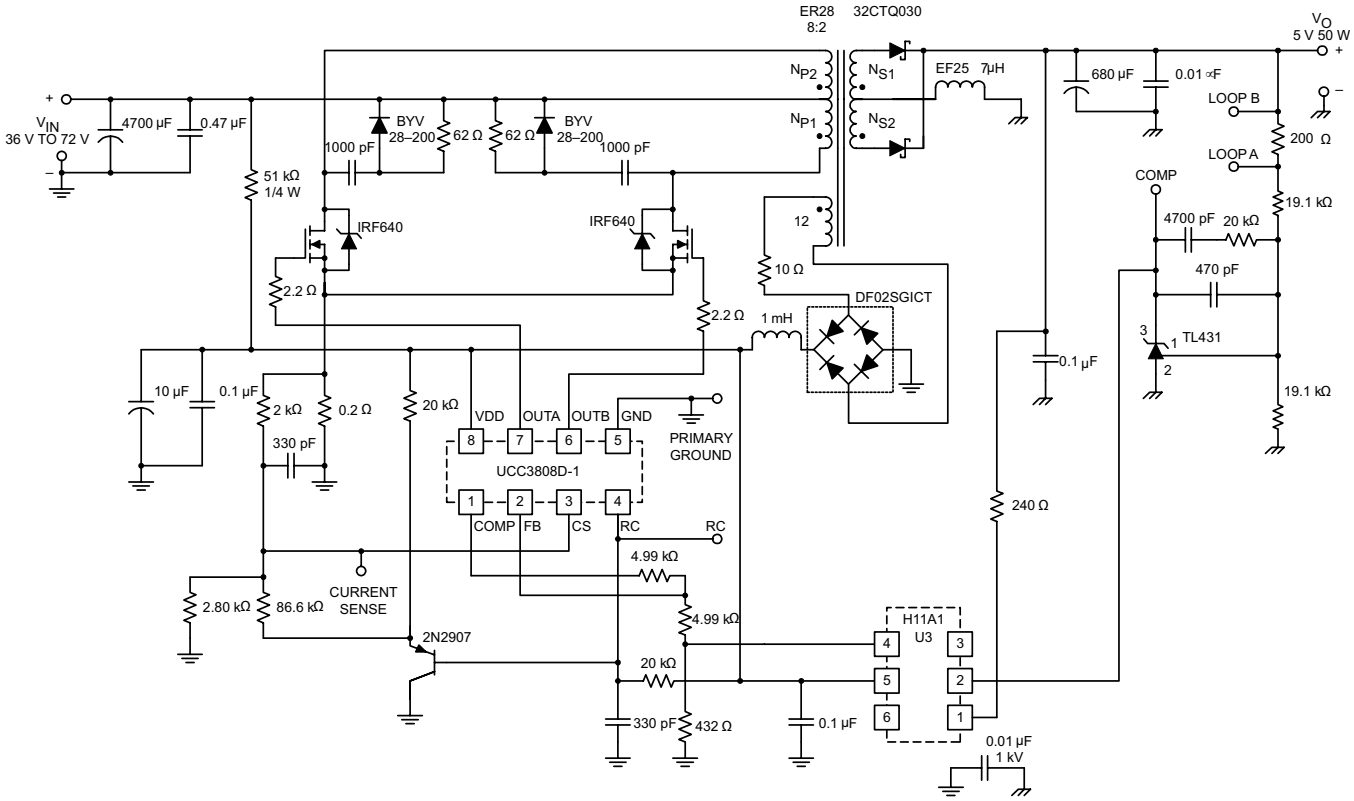


Figure 6. Typical Application Diagram: 48-V In, 5-V, 50-W Output

8.2.1 Design Requirements

Table 3 lists the design parameters of the UCC3808-x.

Table 3. Design Parameters

DESIGN PARAMETER	TARGET VALUE
Output voltage	5 V
Rated output power	50 W
Input DC voltage range	36 V to 72 V
Switching frequency	210 kHz

8.2.2 Detailed Design Procedure

The output, VO, provides 5 V at 75 W maximum and is electrically isolated from the input. Since the UCC3808 is a peak current mode controller the 2N2222A emitter following amplifier (buffers the CT waveform) provides slope compensation which is necessary for duty ratios greater than 50%. Capacitor decoupling is very important with a single ground IC controller, and a 1 µF is suggested as close to the IC as possible. The controller supply is a series RC for start-up, paralleled with a bias winding on the output inductor used in steadystate operation.

Isolation is provided by an optocoupler with regulation done on the secondary side using the UC3965 Precision Reference with Low Offset Error Amplifier. Small signal compensation with tight voltage regulation is achieved using this part on the secondary side. Many choices exist for the output inductor depending on cost, volume, and mechanical strength. Several design options are iron powder, molypermalloy (MPP), or a ferrite core with an air gap as shown here. The main power transformer is a low profile design, EFD size 25, using Magnetics Inc. P material which is a good choice at this frequency and temperature. The input voltage may range from 36 V DC to 72 V DC.

8.2.3 Application Curves

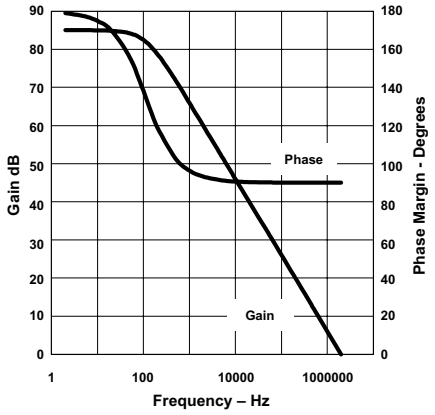


Figure 7. Error Amplifier Gain and Phase Response vs Frequency

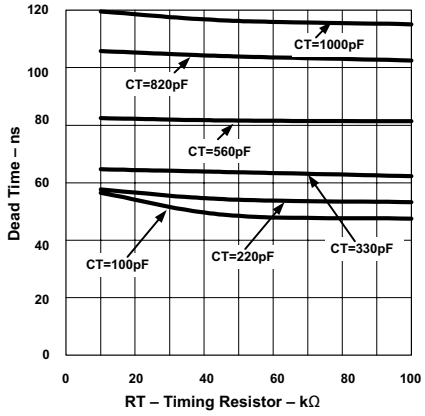


Figure 8. Dead Time vs Timing Resistor

9 Power Supply Recommendations

The VDD power terminal for the device requires the placement of electrolytic capacitor as energy storage capacitor, because of UCCx808-x is controller with 1-A driver capability. And requires the placement of low-ESR noise-decoupling capacitance as directly as possible from the VDD terminal to the GND terminal, ceramic capacitors with stable dielectric characteristics over temperature are recommended, such as X7R or better. The recommended electrolytic capacitor is a 10-µF or 25-V capacitor.

The recommended decoupling capacitors are a 0.1-µF 0603-sized 25-V X7R capacitor.

10 Layout

10.1 Layout Guidelines

1. Locate the VDD capacitor as close as possible between the VDD terminal and GND of the UCCx808-x, tracked directly to both terminals.
2. A small, external filter capacitor is recommended on the CS terminal. Track the filter capacitor as directly as possible from the CS to GND terminal.
3. The tracking and layout of the FB terminal and connecting components is critical to minimizing noise pick-up and interference in the magnetic sensing block. Reduce the total surface area of trances on the FB net to a minimum.
4. The OUTA/OUTB terminal has high internal sink/source current capability. An external gate resistor is recommended. The value depends on the choice of power MOSFET, efficiency and EMI considerations. A pulldown resistor on the gate of the external MOSFET is recommended to prevent the MOSFET gate from floating on if there is an open-circuit error in the gate drive path.

10.2 Layout Example

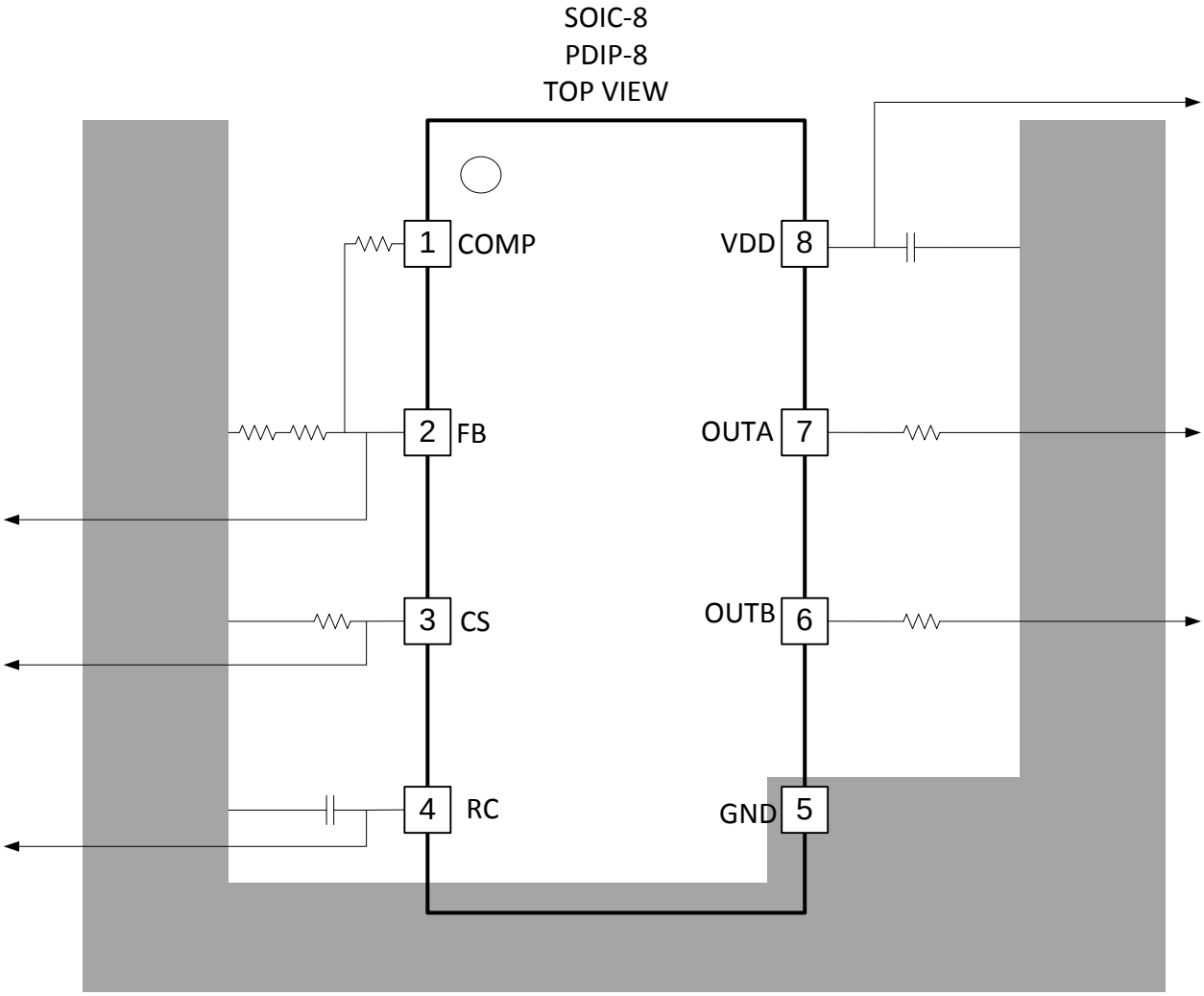


Figure 9. Layout Example

11 Device and Documentation Support

11.1 Related Links

The table below lists quick access links. Categories include technical documents, support and community resources, tools and software, and quick access to sample or buy.

Table 4. Related Links

PARTS	PRODUCT FOLDER	SAMPLE & BUY	TECHNICAL DOCUMENTS	TOOLS & SOFTWARE	SUPPORT & COMMUNITY
UCC2808-1	Click here	Click here	Click here	Click here	Click here
UCC2808-2	Click here	Click here	Click here	Click here	Click here
UCC3808-1	Click here	Click here	Click here	Click here	Click here
UCC3808-2	Click here	Click here	Click here	Click here	Click here

11.2 Documentation Support

11.2.1 Related Documentation

For related documentation, see the following:

Power Supply Control Data Book (SLUD003)

11.3 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.4 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.5 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.6 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead finish/ Ball material (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
UCC2808DTR-1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808-1	Samples
UCC2808DTR-2	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808-2	Samples
UCC2808DTR-2G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	-40 to 85	2808-2	Samples
UCC3808DTR-1	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	(3808-1, UCC3808) D-1	Samples
UCC3808DTR-2	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808-2	Samples
UCC3808DTR-2G4	ACTIVE	SOIC	D	8	2500	RoHS & Green	NIPDAU	Level-1-260C-UNLIM	0 to 70	3808-2	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
RoHS Exempt: TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.
Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

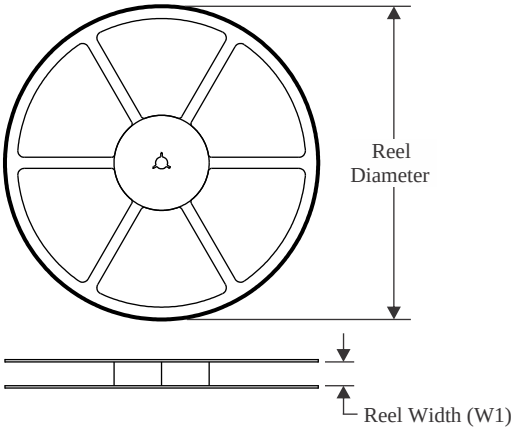
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

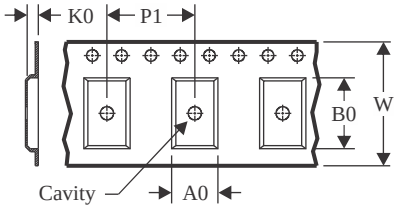
(6) Lead finish/Ball material - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead finish/Ball material values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

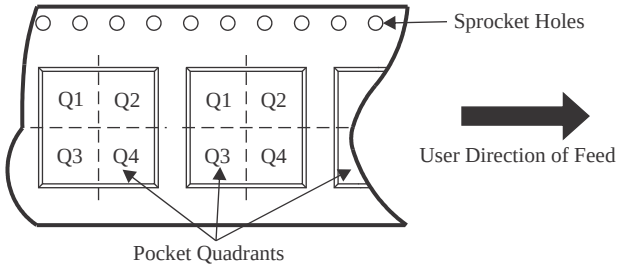


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

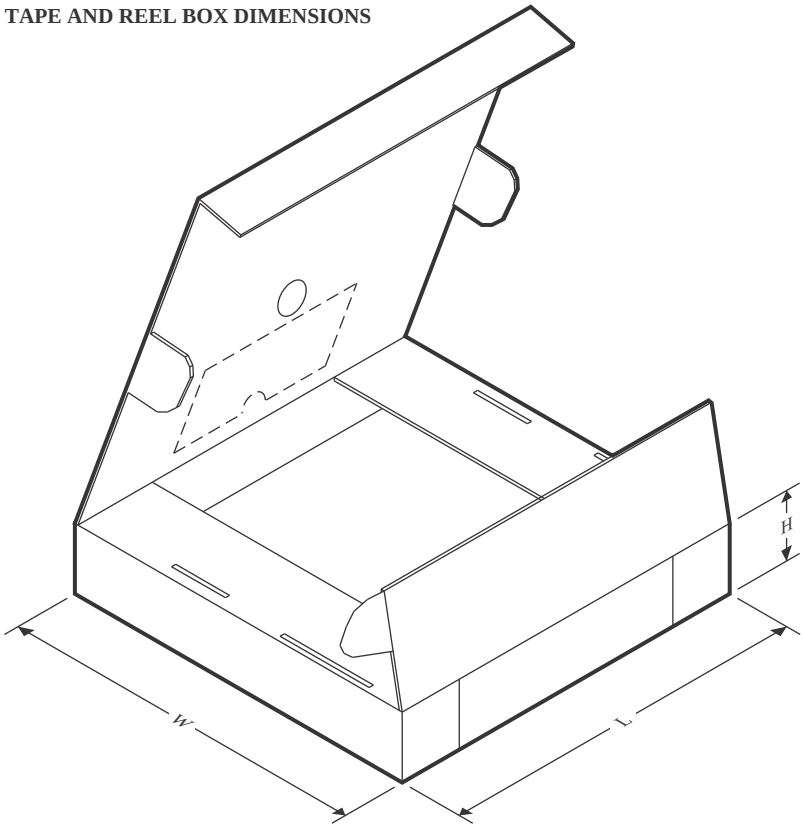
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

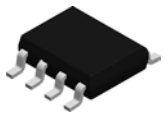
Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
UCC2808DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC2808DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808DTR-1	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1
UCC3808DTR-2	SOIC	D	8	2500	330.0	12.4	6.4	5.2	2.1	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
UCC2808DTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC2808DTR-2	SOIC	D	8	2500	340.5	338.1	20.6
UCC3808DTR-1	SOIC	D	8	2500	340.5	338.1	20.6
UCC3808DTR-2	SOIC	D	8	2500	340.5	338.1	20.6

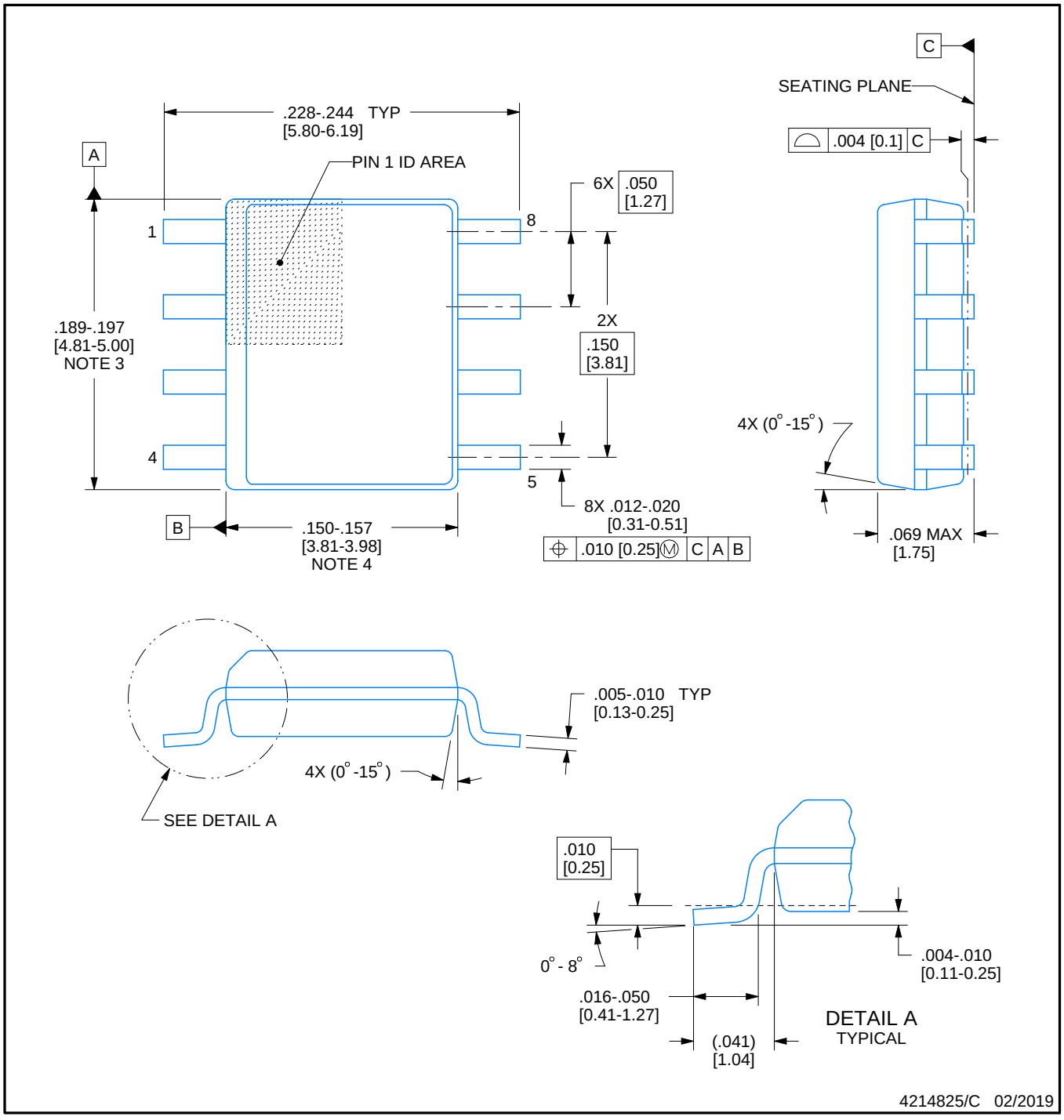


PACKAGE OUTLINE

D0008A

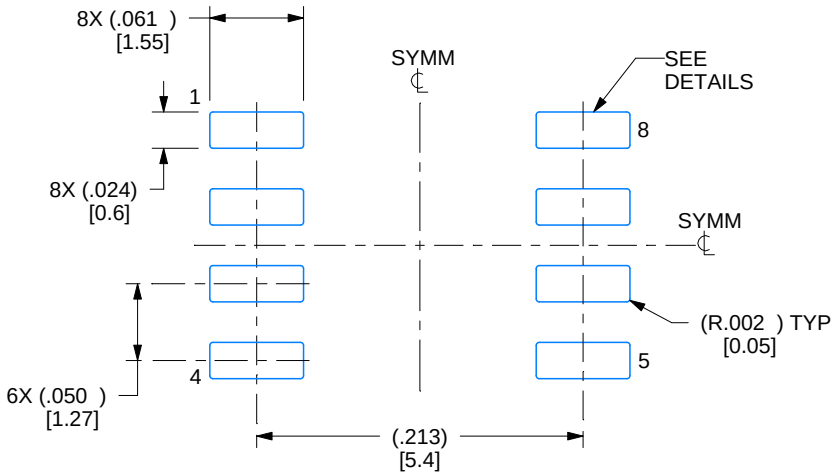
SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT

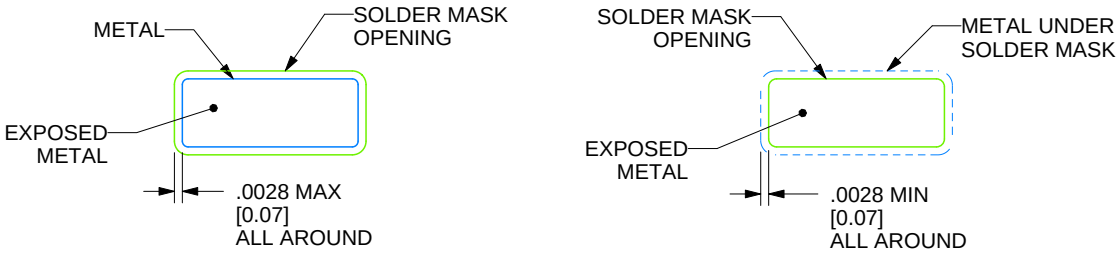


NOTES:

1. Linear dimensions are in inches [millimeters]. Dimensions in parenthesis are for reference only. Controlling dimensions are in inches. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed .006 [0.15] per side.
4. This dimension does not include interlead flash.
5. Reference JEDEC registration MS-012, variation AA.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:8X



SOLDER MASK DETAILS

4214825/C 02/2019

NOTES: (continued)

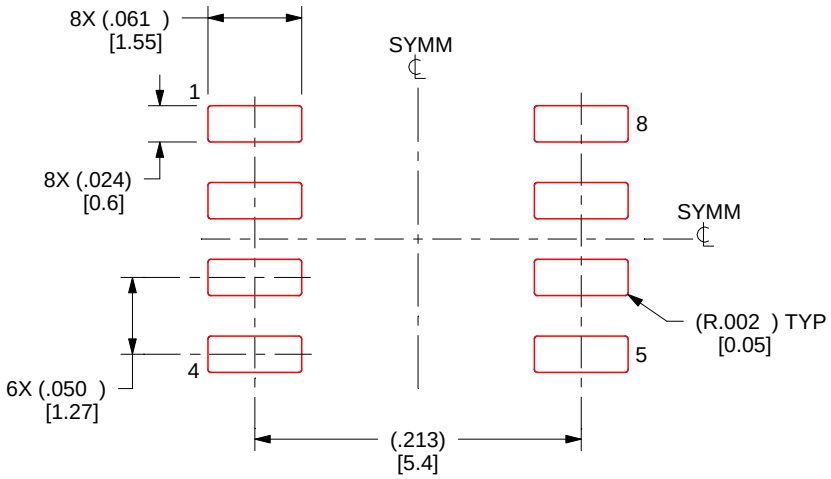
6. Publication IPC-7351 may have alternate designs.
7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

D0008A

SOIC - 1.75 mm max height

SMALL OUTLINE INTEGRATED CIRCUIT



SOLDER PASTE EXAMPLE
BASED ON .005 INCH [0.125 MM] THICK STENCIL
SCALE:8X

4214825/C 02/2019

NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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