



**THE DATASHEET OF  
A3283LLHLT**



## *Chopper-Stabilized, Precision Hall-Effect Latches*

### **Last Time Buy**

The A3283 part is in production but has been determined to be LAST TIME BUY. This classification indicates that the product is obsolete and notice has been given. Sale of this device is currently restricted to existing customer applications. The device should not be purchased for new design applications because of obsolescence in the near future. Samples are no longer available.

Date of status change: August 16, 2010

Deadline for receipt of LAST TIME BUY orders: October 29, 2010

#### **Recommended Substitutions:**

*For existing customer transition, and for new customers or new applications, refer to the [A1223](#).*

*Note: The A3280 and A3281 are obsolete. For existing customer transition, and for new customers or new applications, refer to the [A1222](#).*

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NOTE: For detailed information on purchasing options, contact your local Allegro field applications engineer or sales representative.

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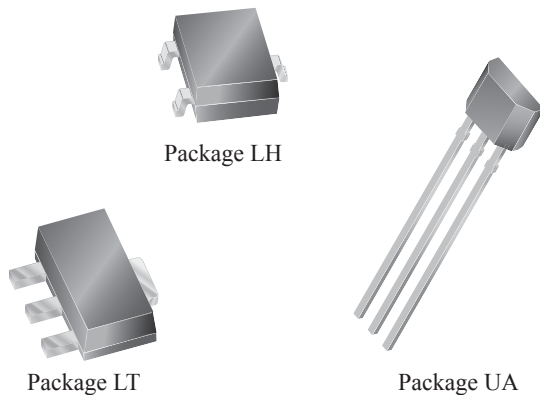
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## Chopper-Stabilized, Precision Hall-Effect Latches

### Features and Benefits

- Symmetrical switch points
- Resistant to physical stress
- Superior temperature stability
- Output short-circuit protection
- Operation from unregulated supply
- Reverse battery protection
- Solid-state reliability
- Small size

### Packages:



Not to scale

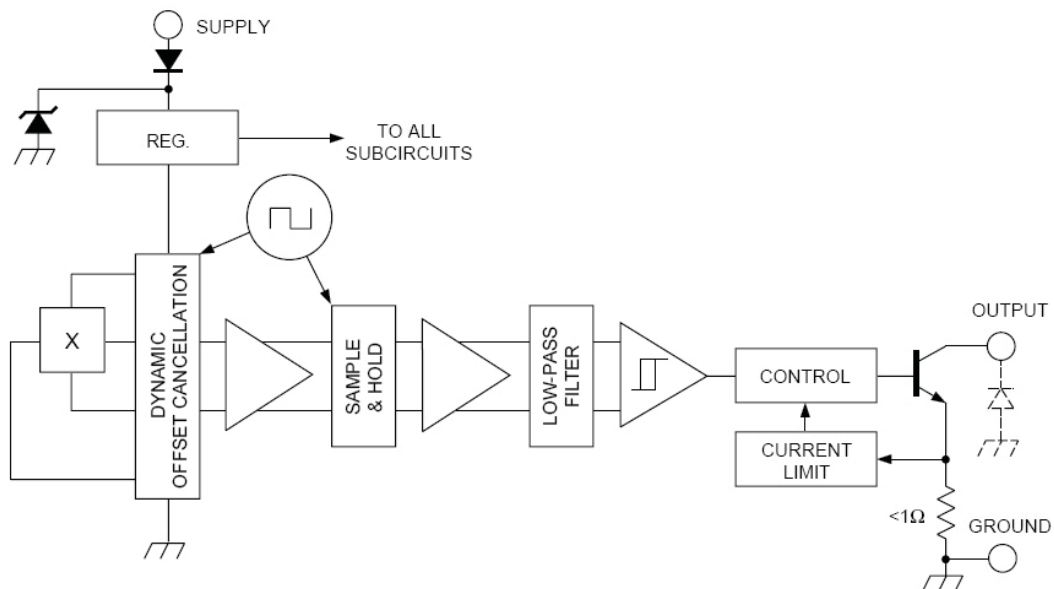
### Description

The A3280, A3281, and A3283 Hall-effect latches are extremely temperature-stable and stress-resistant sensor ICs especially suited for operation over extended temperature ranges to +150°C. Superior high-temperature performance is made possible through dynamic offset cancellation, which reduces the residual offset voltage normally caused by device overmolding, temperature dependencies, and thermal stress. The three devices are identical except for magnetic switch points.

Each device includes on a single silicon chip a voltage regulator, Hall-voltage generator, small-signal amplifier, chopper stabilization, Schmitt trigger, and a short-circuit protected open-collector output to sink up to 25 mA. A south pole of sufficient strength will turn the output on. A north pole is necessary to turn the output off. An on-board regulator permits operation with supply voltages of 4.2 to 24 volts.

Three package styles provide a magnetically optimized package for most applications. Package type LH is a modified SOT23W surface-mount package, LT is a miniature SOT89/TO-243AA transistor package for surface-mount applications; while UA is a three-lead ultra-mini-SIP for through-hole mounting. Each package type is lead (Pb) free (suffix, -T), with 100% matte tin leadframe plating.

### Functional Block Diagram



# A3280, A3281 and A3283

# Chopper-Stabilized, Precision Hall-Effect Latches

## Selection Guide

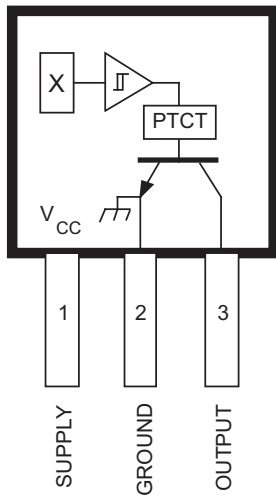
Part Number	Packing*	Mounting	Ambient, $T_A$ (°C)	$B_{RP(MIN)}$ ( $T_A = 25^\circ\text{C}$ ) (G)	$B_{OP(MAX)}$ ( $T_A = 25^\circ\text{C}$ ) (G)
A3283ELTTR-T	7-in. reel, 1000 pieces/reel	SOT89 Surface Mount	-40 to 85	-180	180
A3283EUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			
A3283LLHLT-T	7-in. reel, 3000 pieces/reel	SOT23W Surface Mount	-40 to 150		
A3283LLTTR-T	7-in. reel, 1000 pieces/reel	SOT89 Surface Mount			
A3283LUA-T	Bulk, 500 pieces/bag	3-pin SIP through hole			



\*Contact Allegro for additional packing options.

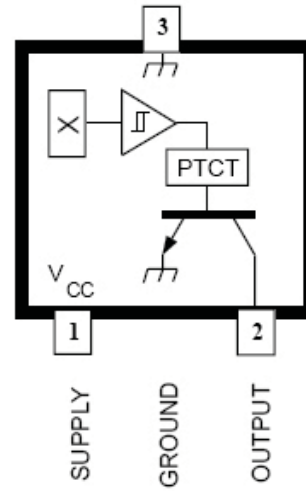
## Absolute Maximum Ratings

Characteristic	Symbol	Notes	Rating	Units
Supply Voltage	$V_{CC}$		26.5	V
Reverse Battery Voltage	$V_{RCC}$		-30	V
Magnetic Flux Density	B		Unlimited	G
Output Off Voltage	$V_{OUT}$		26	V
Continuous Output Current	$I_{OUT}$	Internal current limiting is intended to protect the device from output short circuits.	25	mA
Reverse Output Current	$I_{ROUT}$		-50	mA
Operating Ambient Temperature	$T_A$	Range E	-40 to 85	°C
		Range L	-40 to 150	°C
Maximum Junction Temperature	$T_{J(max)}$		165	°C
Storage Temperature	$T_{stg}$		-65 to 170	°C

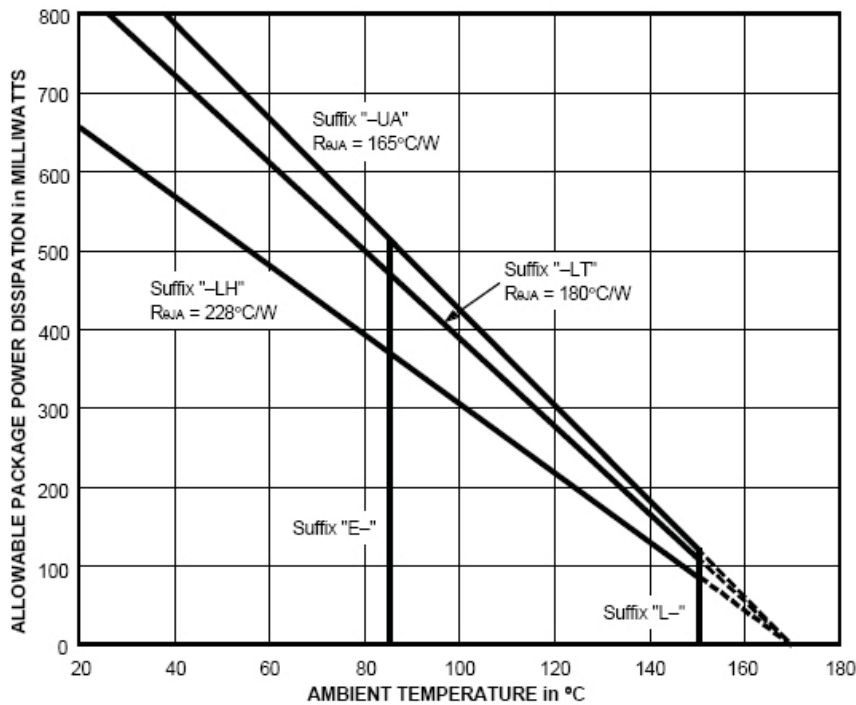


Dwg. PH-003-2

**Suffix '-LT' & '-UA' Pinning**  
(SOT89/TO-243AA & ultra-mini SIP)



**Suffix '-LH' Pinning**  
(SOT23W)



Dwg. GH-046-2D

**ELECTRICAL CHARACTERISTICS over operating temperature range.**

Characteristic	Symbol	Test Conditions	Limits			Units
			Min.	Typ.	Max.	
Supply Voltage Range	$V_{CC}$	Operating, $T_J < 170^\circ\text{C}^1$	4.2	–	24	V
Output Leakage Current	$I_{OFF}$	$V_{OUT} = 24\text{ V}$ , $B < B_{RP}$	–	–	10	$\mu\text{A}$
Output Saturation Voltage	$V_{OUT(SAT)}$	$I_{OUT} = 20\text{ mA}$ , $B > B_{OP}$	–	185	500	mV
Output Current Limit	$I_{OM}$	$B > B_{OP}$	30	–	60	mA
Power-On Time	$t_{po}$	$V_{CC} > 4.2\text{ V}$	–	–	50	$\mu\text{s}$
Chopping Frequency	$f_C$		–	340	–	kHz
Output Rise Time	$t_r$	$R_L = 820\ \Omega$ , $C_L = 20\text{ pF}$	–	0.2	2.0	$\mu\text{s}$
Output Fall Time	$t_f$	$R_L = 820\ \Omega$ , $C_L = 20\text{ pF}$	–	0.1	2.0	$\mu\text{s}$
Supply Current	$I_{CC}$	$B < B_{RP}$ , $V_{CC} = 12\text{ V}$	–	3.0	8.0	mA
		$B > B_{OP}$ , $V_{CC} = 12\text{ V}$	–	4.0	8.0	mA
Reverse Battery Current	$I_{CC}$	$V_{RCC} = -30\text{ V}$	–	–	-5.0	mA
Zener Voltage	$V_Z + V_D$	$I_{CC} = 15\text{ mA}$ , $T_A = 25^\circ\text{C}$	28	32	37	V
Zener Impedance	$Z_Z + Z_D$	$I_{CC} = 15\text{ mA}$ , $T_A = 25^\circ\text{C}$	–	50	–	$\Omega$

- NOTES:
1. Maximum voltage must be adjusted for power dissipation and junction temperature.
  2.  $B_{OP}$  = operate point (output turns on);  $B_{RP}$  = release point (output turns off).
  3. Typical Data is at  $T_A = +25^\circ\text{C}$  and  $V_{CC} = 12\text{ V}$  and is for design information only.

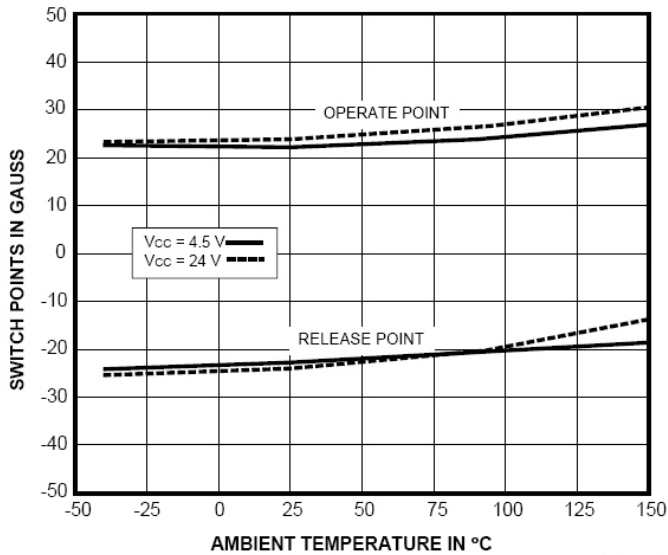
**MAGNETIC CHARACTERISTICS over operating voltage range.**

Characteristic	Test Conditions	Part Numbers <sup>1</sup>									Units
		A3280			A3281			A3283			
		Min.	Typ.	Max.	Min.	Typ.	Max.	Min.	Typ.	Max.	
Operate Point, $B_{OP}$	at $T_A = +25^\circ\text{C}$ and $T_A = \text{max.}$	5.0	22	40	15	50	90	100	150	180	G
	at $T_A = -40^\circ\text{C}$	5.0	–	40	15	–	90	100	–	200	G
Release Point, $B_{RP}$	at $T_A = +25^\circ\text{C}$ and $T_A = \text{max.}$	-40	-23	-5.0	-90	-50	-15	-180	-150	-100	G
	at $T_A = -40^\circ\text{C}$	-40	–	-5.0	-90	–	-15	-200	–	-100	G
Hysteresis, $B_{hys}$ ( $B_{OP} - B_{RP}$ )	at $T_A = +25^\circ\text{C}$ and $T_A = \text{max.}$	10	45	80	30	100	180	–	300	360	G
	at $T_A = -40^\circ\text{C}$	–	–	80	–	–	180	–	–	360	G

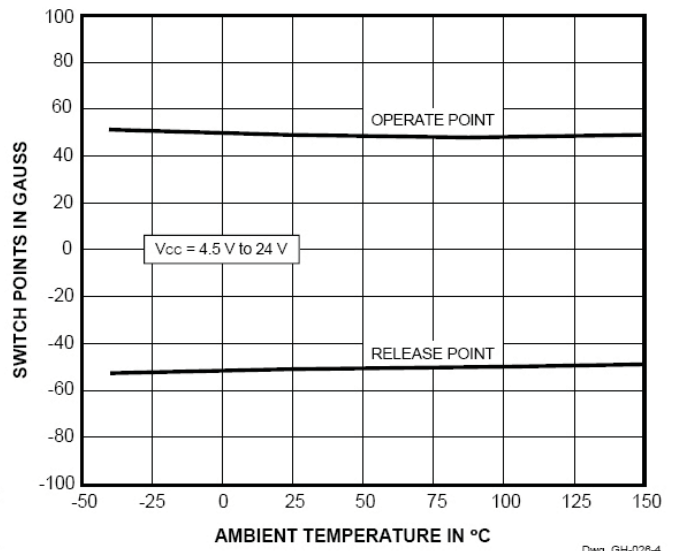
- NOTES:
1. Complete part number includes a suffix to identify operating temperature range (E or L) and package type (LH, LT, or UA).
  2. As used here, negative flux densities are defined as less than zero (algebraic convention) and -50 G is less than +10 G.
  3. Typical Data is at  $T_A = +25^\circ\text{C}$  and  $V_{CC} = 12\text{ V}$  and is for design information only.
  4. 1 gauss (G) is exactly equal to 0.1 millitesla (mT).

**TYPICAL OPERATING CHARACTERISTICS  
as a function of temperature**

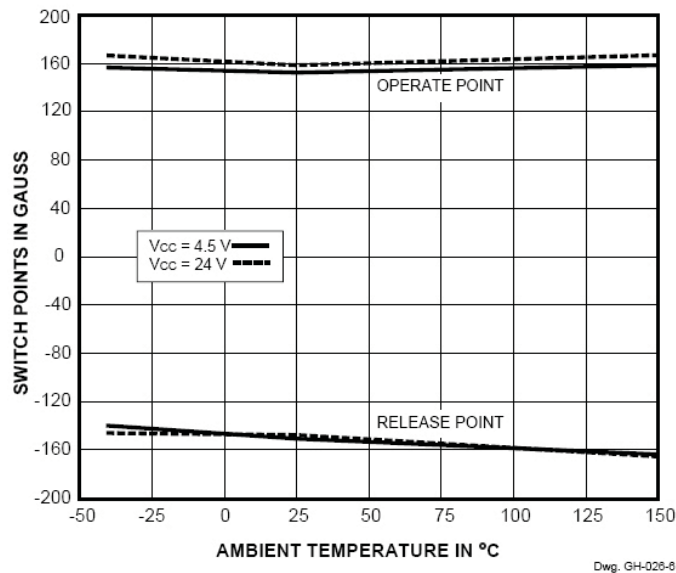
**A3280 SWITCH POINTS**



**A3281 SWITCH POINTS**

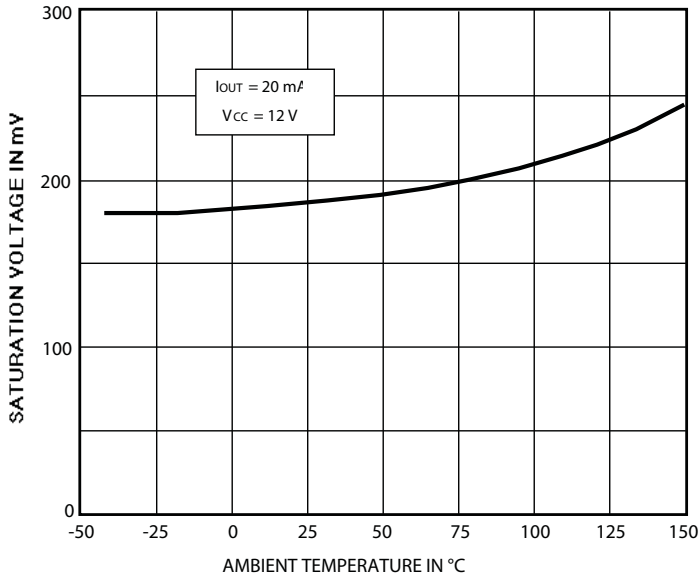


**A3283 SWITCH POINTS**



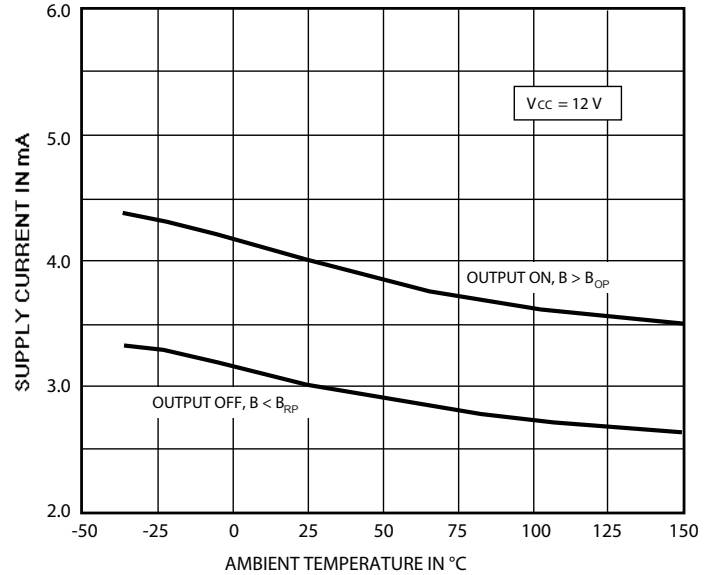
**TYPICAL OPERATING CHARACTERISTICS  
as a function of temperature (cont'd)**

**OUTPUT SATURATION VOLTAGE**



Dwg. GH-029-4

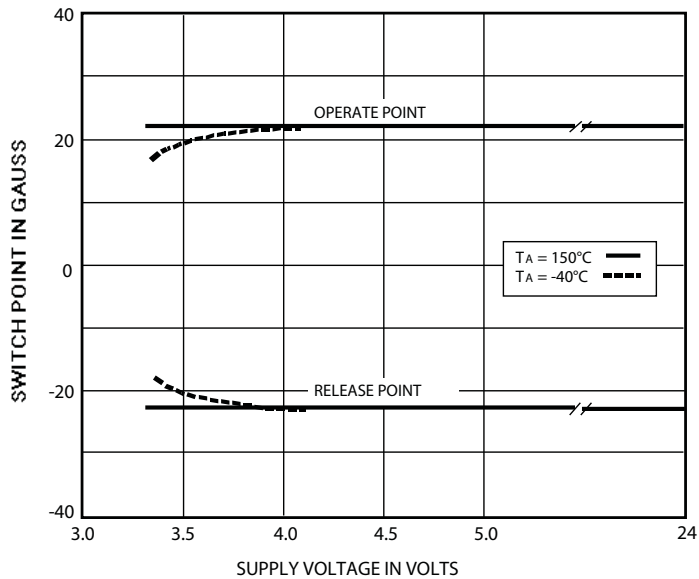
**SUPPLY CURRENT**



Dwg. GH-028-5

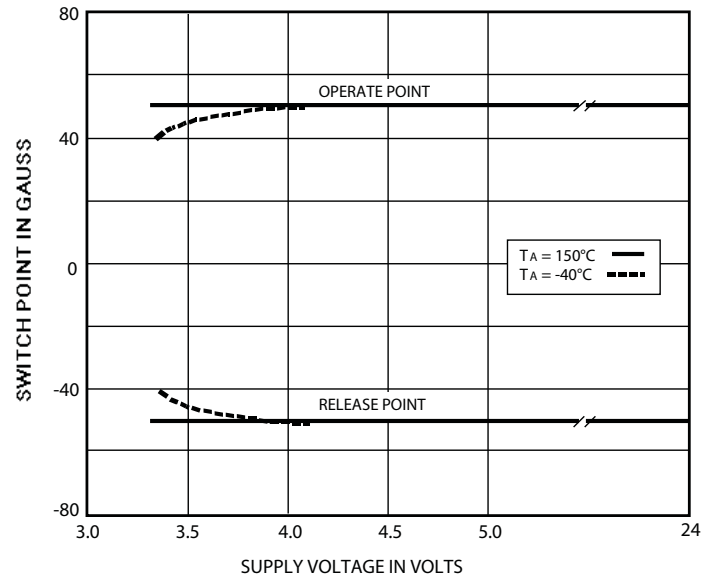
**TYPICAL OPERATING CHARACTERISTICS  
as a function of supply voltage**

**A3280 SWITCH POINTS**



Dwg. GH-021-3

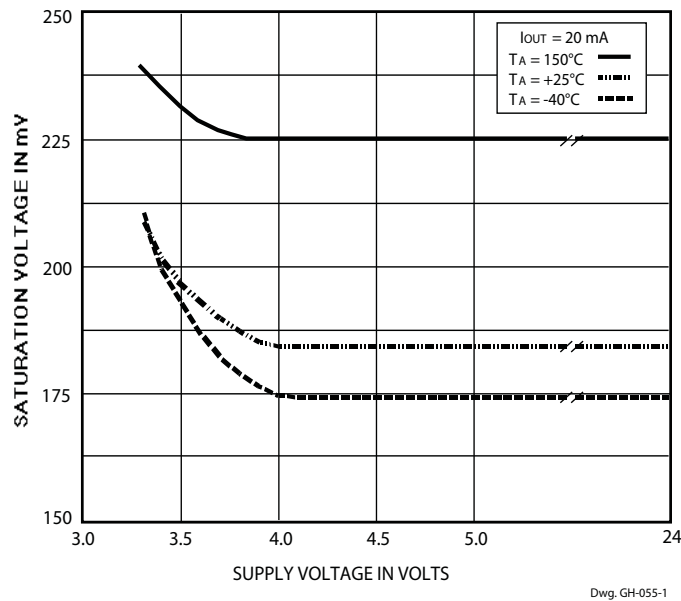
**A3281 SWITCH POINTS**



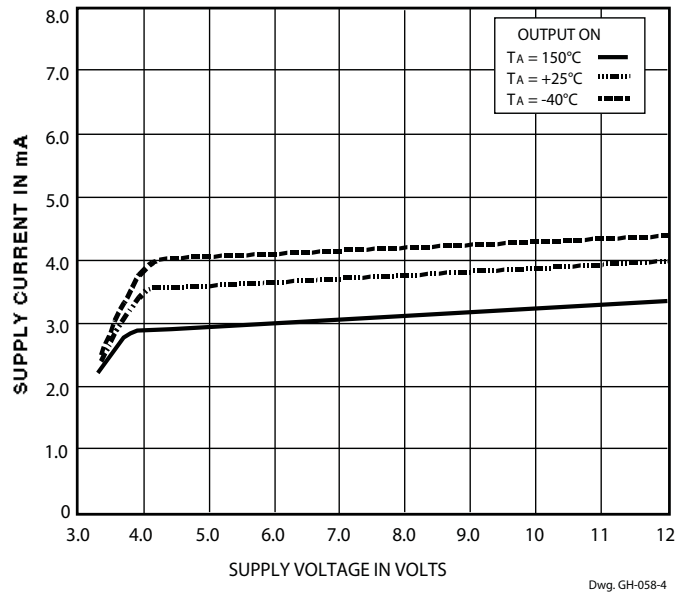
Dwg. GH-021-1

**TYPICAL OPERATING CHARACTERISTICS  
as a function of supply voltage (cont'd)**

**OUTPUT SATURATION VOLTAGE**



**SUPPLY CURRENT**



**FUNCTIONAL DESCRIPTION**

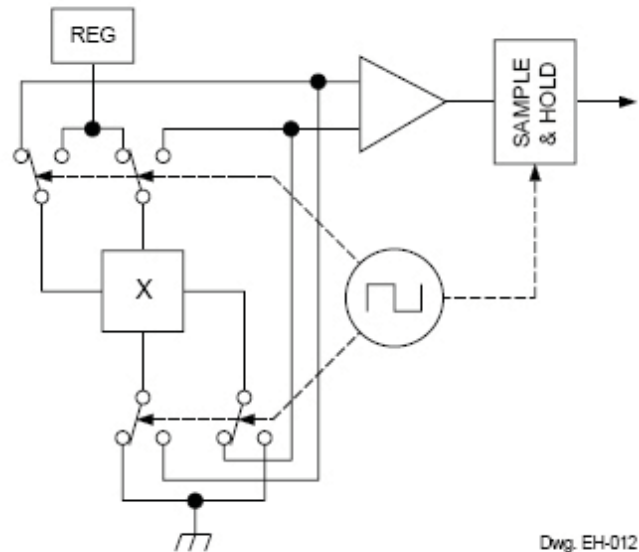
**Chopper-Stabilized Technique.** The Hall element can be considered as a resistor array similar to a Wheatstone bridge. A large portion of the offset is a result of the mismatching of these resistors. These devices use a proprietary dynamic offset cancellation technique, with an internal high-frequency clock to reduce the residual offset voltage of the Hall element that is normally caused by device overmolding, temperature dependencies, and thermal stress. The chopper-stabilizing technique cancels the mismatching of the resistor circuit by changing the direction of the current flowing through the Hall plate using CMOS switches and Hall voltage measurement taps, while maintaining the Hall-voltage signal that is induced by the external magnetic flux. The signal is then captured by a sample-and-hold circuit and further processed using low-offset bipolar circuitry. This technique produces devices that have an extremely stable quiescent Hall output voltage, are immune to thermal stress, and have precise recoverability after temperature cycling. This technique will also slightly degrade the device output repeatability. A relatively high sampling frequency is used in order that faster signals can be processed.

More detailed descriptions of the circuit operation can be found in: Technical Paper STP 97-10, *Monolithic Magnetic Hall Sensing Using Dynamic Quadrature Offset Cancellation* and Technical Paper STP 99-1, *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*.

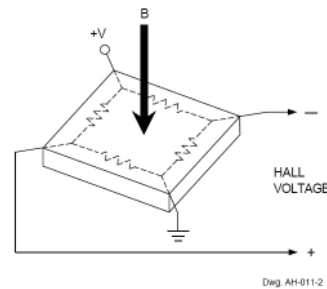
**Operation.** The output of these devices switches low (turns on) when a magnetic field perpendicular to the Hall element exceeds the operate point threshold ( $B_{OP}$ ). After turn-on, the output is capable of sinking 25 mA and the output voltage is  $V_{OUT(SAT)}$ . Note that the device latches; that is, a south pole of sufficient strength towards the branded surface of the device will turn the device on; removal of the south pole will leave the device on. When the magnetic field is reduced below the release point ( $B_{RP}$ ), the device output goes high (turns off). The difference in the magnetic operate and release points is the hysteresis ( $B_{hys}$ ) of the device. This built-in hysteresis allows clean switching of the output even in the presence of external mechanical vibration and electrical noise.

Powering up in the absence of a magnetic field (less than  $B_{OP}$  and higher than  $B_{RP}$ ) will allow an indeterminate output state. The correct state is warranted after the first excursion beyond  $B_{OP}$  or  $B_{RP}$ .

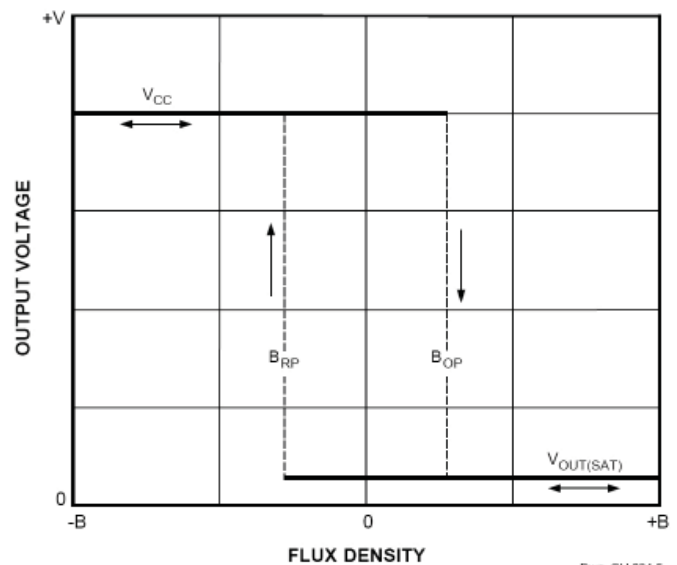
It is strongly recommended that an external bypass capacitor



Dwg. EH-012



Dwg. AH-011-2



Dwg. GH-034-5

**APPLICATIONS INFORMATION**

be connected (in close proximity to the Hall element) between the supply and ground of the device to reduce both external noise and noise generated by the chopper-stabilization technique.

The simplest form of magnet that will operate these devices is a ring magnet. Other methods of operation, such as linear magnets, are possible.

Extensive applications information for Hall-effect devices is available in:

- *Hall-Effect IC Applications Guide*, Application Note 27701;
- *Guidelines for Designing Subassemblies Using Hall-Effect De-*

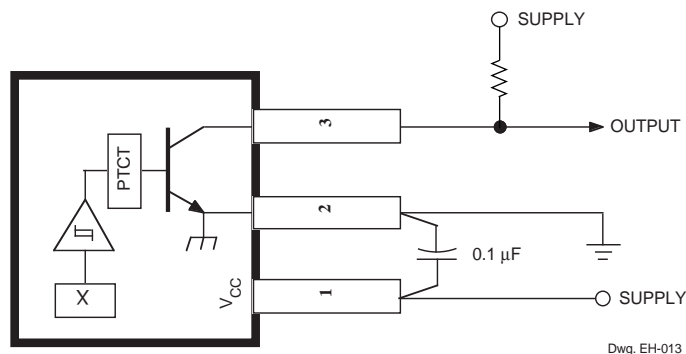
*vices*, Application Note 27703.1

More detailed descriptions of the chopper-stabilized circuit operation can be found in:

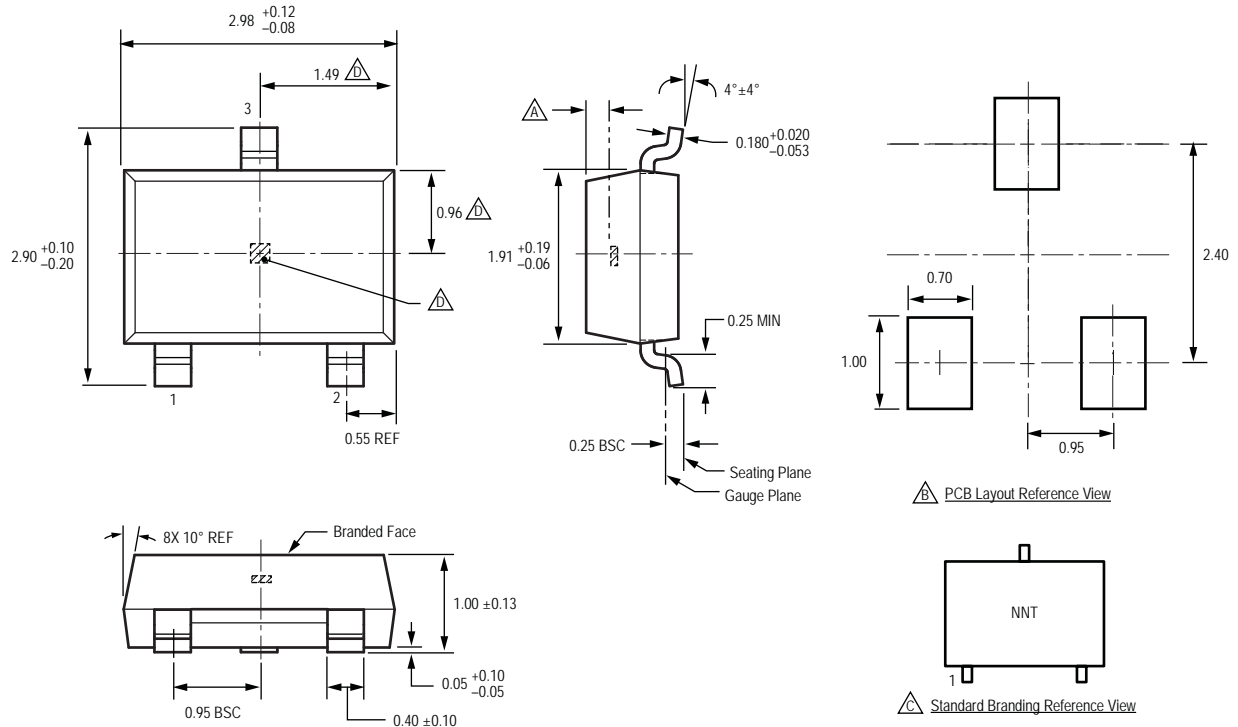
- *Monolithic Magnetic Hall Sensing Using Dynamic Quadrature Offset Cancellation*, Technical Paper STP 97-10; and
- *Chopper-Stabilized Amplifiers With A Track-and-Hold Signal Demodulator*, Technical Paper STP 99-1.

All are provided at

[www.allegromicro.com](http://www.allegromicro.com)



**Package LH, 3-Pin (SOT-23W)**

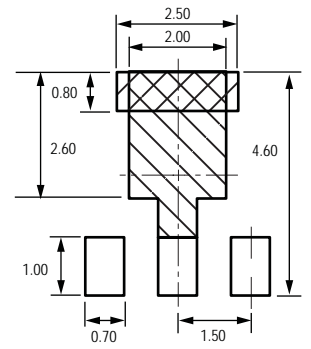
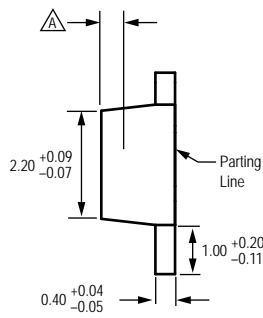
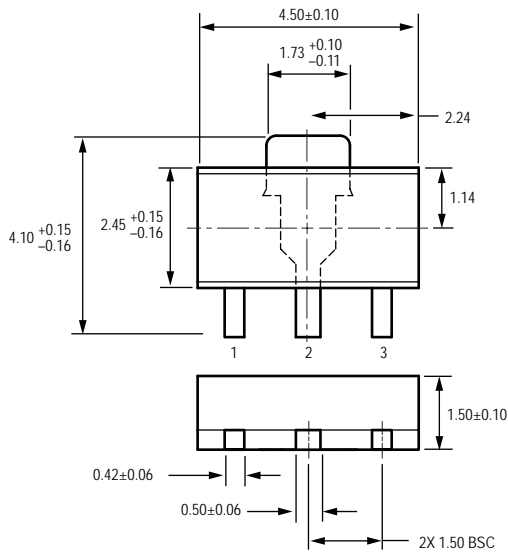


For Reference Only; not for tooling use (reference dwg. 802840)  
 Dimensions in millimeters  
 Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
 Exact case and lead configuration at supplier discretion within limits shown

- Active Area Depth, 0.28 mm REF
- Reference land pattern layout  
All pads a minimum of 0.20 mm from all adjacent pads; adjust as necessary to meet application process requirements and PCB layout tolerances
- Branding scale and appearance at supplier discretion
- Hall element, not to scale

Standard Branding Reference View  
 N = Last two digits of device part number  
 T = Temperature code

Package LT, 3-Pin SOT89

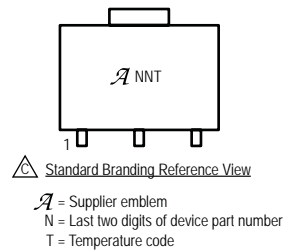


**PCB Layout Reference View**

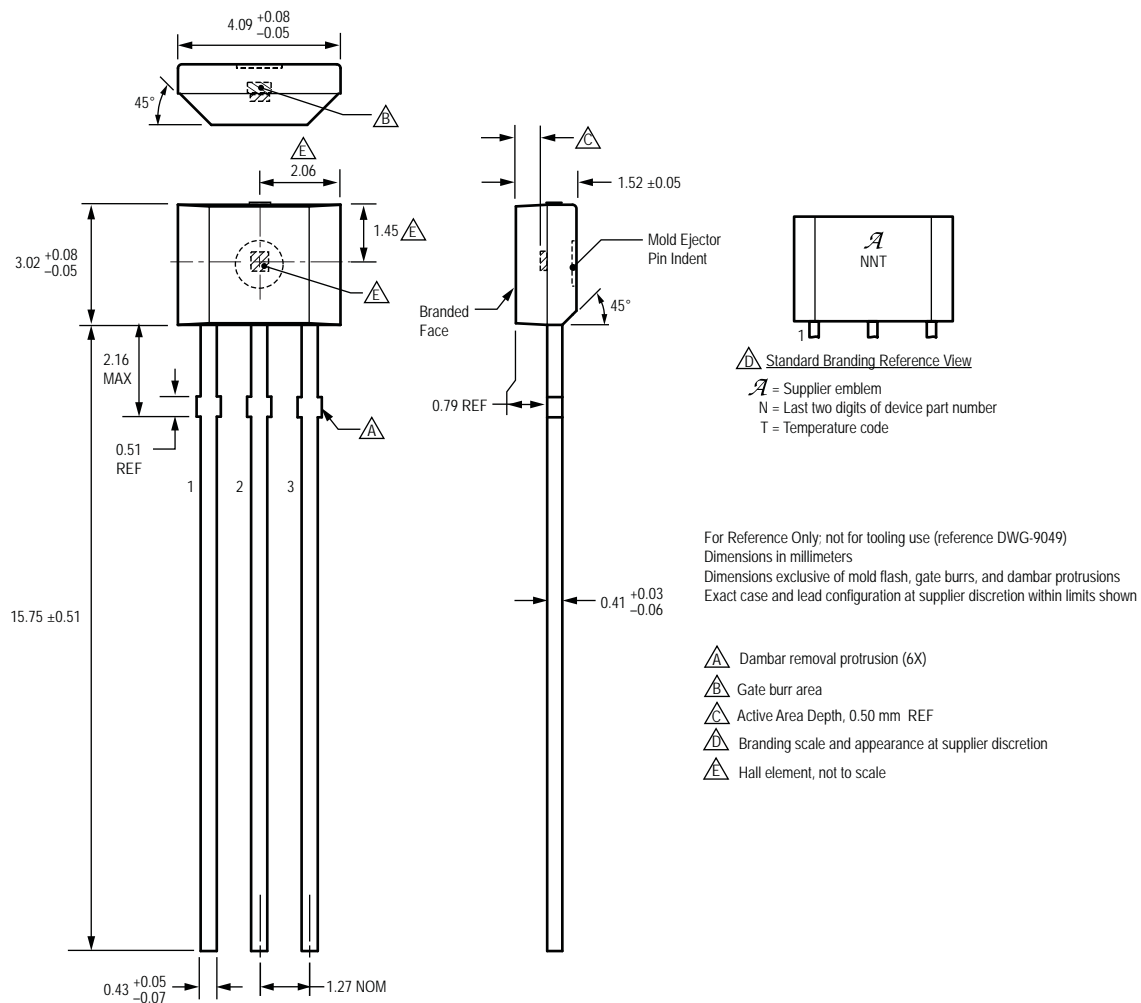
- Basic pads for low-stress, not self-aligning
- Additional pad for low-stress, self-aligning
- Additional area for IPC reference layout

For Reference Only; not for tooling use (reference JEDEC, TO-243AA)  
Dimensions in millimeters  
Dimensions exclusive of mold flash, gate burrs, and dambar protrusions  
Exact case and lead configuration at supplier discretion within limits shown

- Active Area Depth, 0.78 mm REF
- Reference land pattern layout (reference IPC7351 SOT89N);  
All pads a minimum of 0.20 mm from all adjacent pads;  
adjust as necessary to meet application process requirements and PCB layout tolerances
- Branding scale and appearance at supplier discretion
- Hall element, not to scale



Package UA, 3-Pin SIP



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