VSC8601

10/100/1000BASE-T PHY with RGMII MAC Interface

Datasheet

VMDS-10210
Revision 4.1
September 2009

Vitesse
Corporate Headquarters
741 Calle Plano
Camarillo, California 93012
United States

www.vitesse.com

Contents

Figures

Tables

Revision History

This section describes the changes that were implemented in this document. The changes are listed by revision, starting with the most current publication.

Revision 4.1

Revision 4.1 of this datasheet was published in September 2009. In revision 4.1 of the document, design considerations were added. For more information, see "Design Considerations," page 96.

Revision 4.0

Revision 4.0 of this datasheet was published in November 2007. The following is a summary of the changes implemented in the datasheet:

- The VSC8601KN package was removed. VSC8601XKN remains available.
- The electrostatic discharge voltage values were added. For charged device model, it is ±500. For human body model, it is ±1500.
- The moisture sensitivity is now specified as level 3.
- In the jumbo packet register settings (28E.11:10), the packet lengths were updated.
- In several current consumption specifications, the values for total power at 2.5 V were corrected. The previous values were slightly elevated.
- In the DC characteristics for V_{DDIO} at 3.3 V, both the input and output leakage current parameters (I_{ILEAK} and I_{OLEAK}) were increased from ±36 µA to ±43 µA.
- In the DC characteristics for V_{DDIO} at 2.5 V, the minimum input high voltage (V_{IH}) was increased from 1.7 V to 2.0 V. Both the input and output leakage current parameters (I_{ILEAK} and I_{OLEAK}) were increased from ±25 µA to ±35 µA.
- Current consumption specifications were added for both the power-down mode and the reset state.
- In the AC characteristics for the CLKOUT pin, the duty cycle ($\%_{DUTY}$) was modified from 40% minimum to 44% minimum and from 60% maximum to 56% maximum. Also, the total jitter (J_{CLK}) was raised from 491 ps maximum to 600 ps maximum, with the qualifier "time interval error" added to the condition.
- In the SMI specifications, the MDC rise and fall times were corrected from minimum values to maximum values.
- For the device reset rise time specification, a condition was added that it is measured from a 10% level to a 90% level.
- In the AC characteristics for RGMII uncompensated, the 1000BASE-T duty cycle ($t_{DUTY1000}$) was separated into two sets of values. In the first set, the values remain the same, but the added condition is: at room temperature and nominal supply and

register 28E.13:12 set to 10 or 11. In the second set, the minimum is 40% and the maximum is 60% and the condition is: register 28E.13:12 set to 00 or 01.

- In the AC characteristics for RGMII compensated, all of the setup and hold times were modified from 0 ns maximum to 3 ns maximum.
- In the description of pin MDIO, the type was corrected from open drain (OD) to input and output (I/O).
- The PLLMODE pin description was updated with additional clocking information. If a crystal or an external 25 MHz clock is used, PLLMODE must be pulled low. If an external 125 MHz clock is used, PLLMODE must be pulled high.
- A design guideline was added regarding writes from the serial management interface (SMI) after a software reset.
- A design guideline was added regarding delays in the link-up process while in the forced 100BASE-TX mode with the automatic MDI/MDI-X detection feature enabled.
- The following design guidelines were removed, because they no longer apply to the device: Remote Fault Status; DSP Optimization Script Required; Default Port Type Incorrect; and Core 1.2 V Supply Needs to Meet Specific Range.

Revision 2.2

Revision 2.2 of this datasheet was published in July 2006. The following is a summary of the changes implemented in the datasheet:

- In the inline powered Ethernet switch diagram, a reference to “SGMII interface” was corrected to “RGMII interface.”
- In the description of CRC counters, the CRC good counter’s highest value was corrected from 10,000 to 9,999 packets, after which the counter clears.
- The device revision number definition was updated from 0000 to 0001 in the identifier 2 register (address 3) and the JTAG device identification.
- In the DC Characteristics for V_{DD33}, $V_{DDIOMAC}$, or $V_{DDIOMICRO}$ at 3.3 V, the output leakage (I_{OLEAK}) was changed to match the same values as the input leakage (I_{ILEAK}) with the same condition (internal resistor included). Specifically, the values were changed from –10 µA minimum and 10 µA maximum to –36 µA minimum and 36 µA maximum.
- In the DC Characteristics for $V_{DDIOMAC}$ or $V_{DDIOMICRO}$ at 2.5 V, the output leakage (I_{OLEAK}) was changed to match the same values as the input leakage (I_{ILEAK}) with the same condition (internal resistor included). Specifically, the values were changed from –10 µA minimum and 10 µA maximum to –25 µA minimum and 25 µA maximum.
- In the DC characteristics for $V_{DDIOMAC}$ or $V_{DDIOMICRO}$ at 2.5 V, the output high voltage parameter (V_{OH}) incorrectly stated I_{OH} = 1.0 mA as a condition. It is now corrected to the condition I_{OH} = –1.0 mA.
- For all the current consumption specifications with the on-chip switching regulator enabled, the specification values for I_{VDD12} and I_{VDD12A} were removed because

they were inadvertently added in a prior revision of this document. The I_{VDD12} and I_{VDD12A} values are kept for current consumption with the regulator disabled.

- For the 100BASE current consumption specifications, all references to the speed were corrected from 100BASE-X to 100BASE-TX.
- In the AC characteristics for the CLKOUT pin, the total jitter specifications were added. They are 217 ps typical and 491 ps maximum.
- For device reset, both the reset characteristics and timing diagram were updated to include new parameters: reset rise time (t_{RST_RISE}) and supply stable time ($t_{VDDSTABLE}$).
- In the stress ratings, the power supply voltage parameter was removed because it was redundant.
- In the pin description for TX_CLK, the rate was clarified to be 2.5 MHz for 10 Mbps mode, 25 MHz for 100 Mbps mode, or 125 MHz for 1000 Mbps mode.
- The errata item “RX_CLK Can Reach as High as 55% Duty Cycle” remains in effect but all other errata items no longer apply to the latest part revision.

Revision 2.1

Revision 2.1 of this datasheet was published in February 2006. The following is a summary of the changes implemented in the datasheet:

- In the high-level block diagram, representation of the XTAL pin was corrected from “XTAL 1/2” to “XTAL1” and “XTAL2.”
- In the RGMII to Cat5 block diagram, the interface name was corrected from GMII to RGMII.
- New information was added about how to manually force the device to use MDI/MDI-X.
- The VSC8601 device switches between the low-power state and LP wake-up state every two seconds; the rate is not programmable, as was originally stated.
- In the link partner wake-up state, the device sends FLP bursts for two seconds; they are not limited to three bursts, as was originally stated.
- In the description of the PHY address for the serial management interface (SMI), the physical address was corrected from 3:0 to 4:0.
- For the enhanced LED method, controlled by MII Register 16E, two of the LED modes have changed. Mode 11, TX activity, and mode 13, RX activity, are now both reserved.
- In the description of the far-end loopback testing feature, the controlling register bit was corrected from 23.3 to 27E.10.
- For the JTAG interface instructions EXTEST and SAMPLE/PRELOAD, the values for register width were modified from TBD to 45.
- For the Mode Control register (address 0), when bit 11 (power-down) is set, RGMII in-band signaling will not function.

- In the Identifier 2 register (address 3), which enables device identification, the default for bits 9:4 was modified from TBD to 000010.
- In the LED Control register (address 27), the name for bits 2 and 1 was corrected from “link/activity” to simply “activity.”
- In the ActiPHY Control (address 20E), bit 5 was reassigned from being reserved to being the MAC RX_CLK disable parameter.
- In the extended PHY control 4 register (address 23E), all the bit settings were mistakenly omitted. They are now restored.
- In the Extended PHY Control 5 register (address 27E), the settings have changed for bits 8:6 and 5:3 (100BASE-TX and 1000BASE-T transmitter amplitude control). For bits 8:6 (100BASE-TX), the setting 011 changed from +5 amplitude to reserved, making bit setting 010 (+4 amplitude) the largest. For bits 5:3 (1000BASE-T), the setting 011 changed from +3 amplitude to reserved, making bit setting 010 (+2 amplitude) the largest.
- For added clarity, the table that lists device functions and related CMODE pins now references the associated register and bit for each function.
- For the EEPROM Configuration Contents table, some address locations were added and the introductory text was corrected.
- For the DC electrical specifications with VDDIO at 3.3 V and with VDDIO at 2.5 V, an additional condition was added. The specifications may be considered valid only when VDDREG = 3.3 V.
- The current consumption specifications were replaced with a new set of specifications.
- In the recommended operating conditions, the minimum and maximum values were modified for the VDDIOMICRO, VDDIOMAC, and VDD33 parameters at 3.3 V. For all of these parameters, the minimum changed from 3.13 V to 3.0 V and the maximum changed from 3.47 V to 3.6 V. The VDDREG parameter was added to the recommended operating conditions.
- In the stress ratings, a new rating was added for the VDDREG parameter.
- An errata section was added.

Revision 2.0

Revision 2.0 of this datasheet was published in December 2005. This was the first publication of the document.

1 Introduction

This document consists of descriptions and specifications for both functional and physical aspects of the VSC8601 10/100/1000BASE-T PHY with RGMII MAC Interface.

In addition to the datasheet, Vitesse maintains an extensive device-specific library of support and collateral materials that you may find useful in developing your own product. Depending upon the Vitesse device, this library may include:

- Software Development Kits with sample commands and scripts
- Reference designs showing the Vitesse device built in to applications in ways intended to exploit its relative strengths
- Presentations highlighting the operational features and specifications of the device to assist in developing your own product road map
- Input/Output Buffer Information specification (IBIS) models to help you create and support the interfaces available on the particular Vitesse product
- Application notes that provide detailed descriptions of the use of the particular Vitesse product to solve real-world problems
- White papers published by industry experts that provide ancillary and background information useful in developing products that take full advantage of Vitesse product designs and capabilities
- User guides that describe specific techniques for interfacing to the particular Vitesse products

Visit and register as a user on the Vitesse Web site to keep abreast of the latest innovations from research and development teams and the most current product and application documentation. The address of the Vitesse Web site is www.vitesse.com.

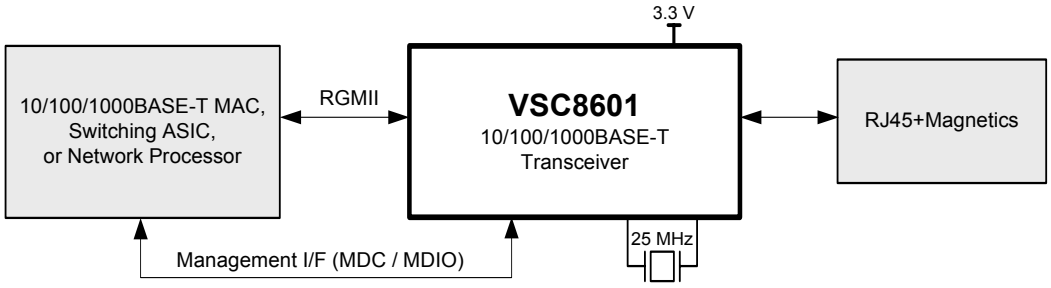
2 Product Overview

The VSC8601 device is a low-power Gigabit Ethernet (GbE) transceiver ideal for Gigabit LAN-on-Motherboard applications. The device's compact, plastic low-profile quad flat package (LQFP) with an exposed pad is optimal for footprint-sensitive applications.

Vitesse's mixed signal and digital signal processing (DSP) architecture assures robust performance. It supports both half-duplex and full-duplex 10BASE-T, 100BASE-TX, and 1000BASE-T communication speeds over Category 5 (Cat5) unshielded twisted pair (UTP) cable at distances greater than 140 m, displaying excellent tolerance to NEXT, FEXT, echo, and other types of ambient environment and system electronic noise.

The following illustration shows a high-level, generic view of a VSC8601 application.

Figure 1. Typical Application



2.1 Features

This section lists key aspects of the VSC8601 device functionality and design that distinguish it from similar products:

- 10/100/1000BASE-T PHY with industry's lowest power consumption.
- Compliant with IEEE 802.3 (10BASE-T, 100BASE-TX, 1000BASE-T) specifications.
- Supports RGMII versions 1.3 and 2.0 (2.5 V, 3.3 V) MAC interface.
- Low EMI line driver with integrated line side termination resistors.
- Up to 16 kB jumbo frame support in all speeds.
- Three programmable direct drive LEDs.
- Suite of test modes, including loopback paths, Ethernet packet generators, and CRC counters.
- The VeriPHY® suite provides extensive network cable information such as cable length, termination status, and open/short fault location.
- ActiPHY™ power saving modes.
- Advanced power management complies with Wake-on-LAN™ and PCI2.2 power requirements.

- Legacy Power-over-Ethernet (POE) support.
- Powered by a single 3.3 V supply by using the optional on-chip switching regulator.
- IEEE 1149.1 JTAG boundary-scan support.
- 10 mm × 10 mm, 64-pin, plastic LQFP package with an exposed pad.

2.2 Applications

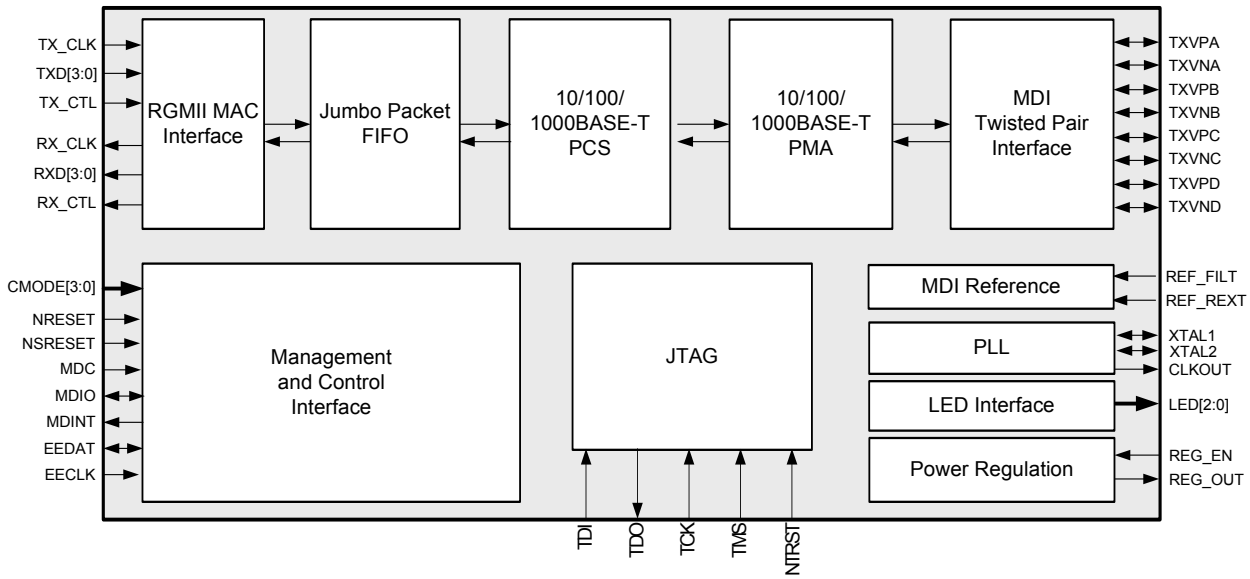
Suggested applications for the VSC8601 device include:

- LAN-on-Motherboards, NICs, and mobile PCs
- iSCSI and TOE applications
- Workgroup and desktop switches and routers
- Gigabit Ethernet SAN, NAS, and MAN systems
- Network-enabled devices such as printers, IP phones, and gaming appliances
- ATCA™ 3.0 and PICMG™ 2.16 Ethernet backplane applications

2.3 Block Diagram

The following illustration shows the primary functional blocks of the VSC8601 device.

Figure 2. High-level Block Diagram



3 Functional Descriptions

This section provides detailed information about how the VSC8601 device works, what configurations and operational features are available, and how to test its functions. It includes descriptions of the various device interfaces and how to set them up.

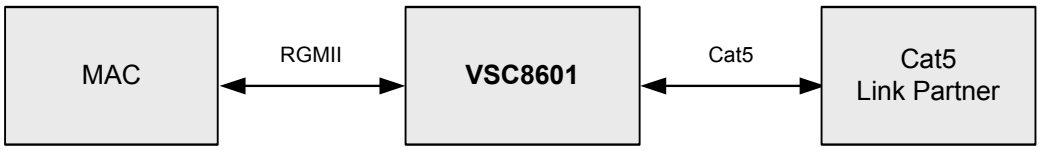
3.1 Interface and Media

The VSC8601 device operates with the interface and media shown in the following table and illustration.

Table 1. Interface and Media

Operating Mode	MAC Interface	Supported Media
RGMII - Cat5	RGMII	10/100/1000BASE-T

Figure 3. RGMII to Cat5 Block Diagram



3.2 MAC Interface

The VSC8601 supports RGMII versions 1.3 and 2.0 (2.5 V, 3.3 V) MAC interface.

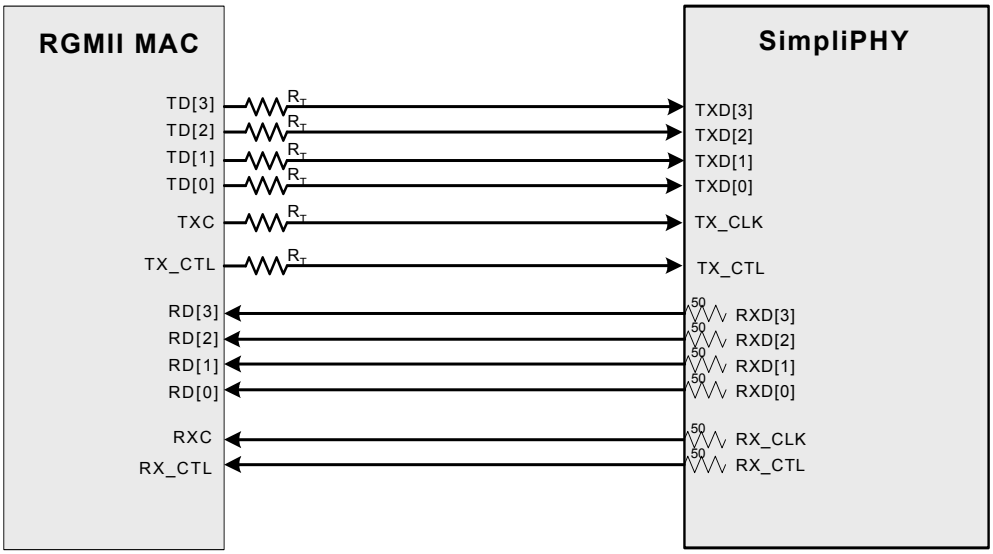
3.2.1 MAC Resistor Calibration

To simplify board design, the VSC8601 MAC interface uses SimpliPIN™ outputs that can self-calibrate to a desired impedance characteristic to eliminate the need for series termination resistors. By default, these RX output pins calibrate to 50 Ω. In addition, MII Register 19E, bits 15:14 can be used to select different target impedances. For more information, see "MAC Resistor Calibration Control," page 58.

3.2.2 RGMII MAC Interface Mode

The RGMII interface can support all three speeds (10 Mbps, 100 Mbps, and 1000 Mbps) and is used as an interface to an RGMII-compatible MAC.

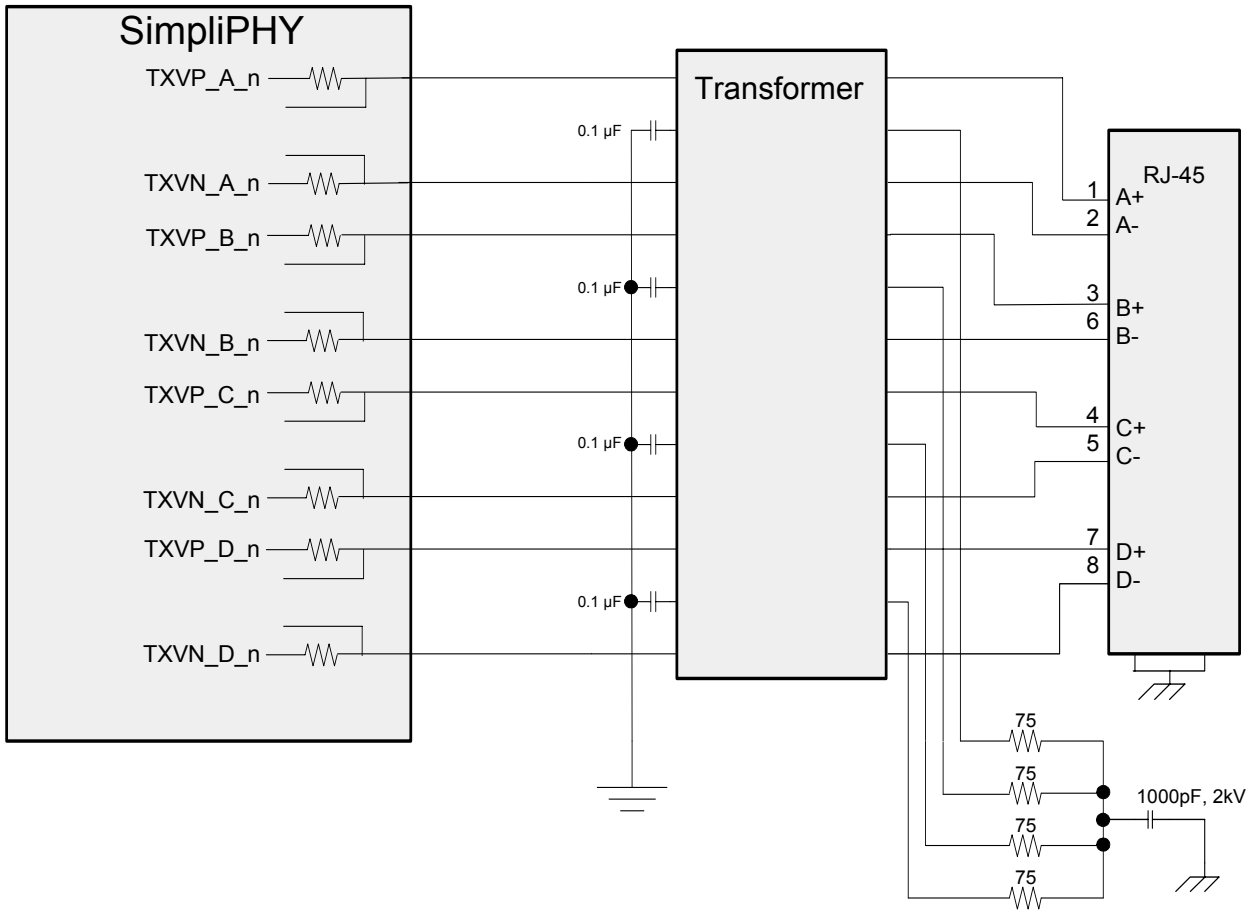
Figure 4. RGMII MAC Interface



3.3 Cat5 Media Interface

The twisted pair interface on the VSC8601 is compliant with the IEEE802.3-2000 specifications for Cat5 media. The VSC8601, unlike other Gigabit PHYs, has all passive components (required to connect the PHY's Cat5 interface to an external 1:1 transformer) fully integrated into the device. The connection of the twisted pair interface is shown in the following figure.

Figure 5. Cat5 Media Interface



3.4 Cat5 Auto-Negotiation

The VSC8601 device supports twisted pair auto-negotiation as defined by clause 28 of the IEEE standard 802.3-2000.

The auto-negotiation process consists of the evaluation of the advertised capabilities of the PHY and its link partner to determine the best possible operating mode, throughput speed, duplex configuration, and master or slave operating modes in the case of 1000BASE-T setups. Auto-negotiation also allows a connected MAC to communicate with its link partner MAC through the VSC8601 device using the optional “next pages,” which set attributes that may not otherwise be defined by the IEEE standard.

In installations where the Cat5 link partner does not support auto-negotiation, the VSC8601 automatically switches to use parallel detection to select the appropriate link speed.

Clearing VSC8601 device register 0, bit 12 disables clause 28 twisted-pair auto-negotiation. If auto-negotiation is disabled, the state of register bits 0.6, 0.13,

and 0.8 determine the device operating speed and duplex mode. For more information about configuring auto-negotiation, see "IEEE Standard and Main Registers," page 38.

3.5 Manual MDI/MDI-X Setting

As an alternative to automatic MDI/MDI-X detection (using HP Auto-MDIX technology), you can force the PHY to select MDI or MDI-X using the following scripts.

Format:

```
Phywrite ( register(dec), data(hex) )

Phywritemask ( register(dec), data(hex), mask(hex) )
```

To force MDI:

```
Phywrite ( 31, 0x2A30 )

Phywritemask ( 5, 0x0010, 0x0018 )

Phywrite ( 31, 0x0000 )
```

To force MDI-X:

```
Phywrite ( 31, 0x2A30 )

Phywritemask ( 5, 0x0018, 0x0018 )

Phywrite ( 31, 0x0000 )
```

To resume MDI/MDI-X setting based on register 18, bits 7 and 5:

```
Phywrite ( 31, 0x2A30 )

Phywritemask ( 5, 0x0000, 0x0018 )

Phywrite ( 31, 0x0000 )
```

3.6 Automatic Crossover and Polarity Detection

For trouble-free configuration and management of Ethernet links, the VSC8601 device includes a robust, automatic, media-dependent and crossed media-dependent detection feature, HP Auto-MDIX, in all of its three available speeds (10BASE-T, 100BASE-T, and 1000BASE-T). The function is fully compliant with clause 40 of the IEEE standard 802.3-2002.

Additionally, the device detects and corrects polarity errors on all MDI pairs—a useful capability that exceeds the requirements of the standard.

Both HP Auto-MDIX detection and polarity correction are enabled in the device by default. The default settings are adjustable using device register bits 18.5:4. Status bits for each of these functions are located in register 28.

The VSC8601 device's algorithm for HP Auto-MDIX successfully detects, corrects, and operates with any of the MDI wiring pair combinations listed in the following table.

Table 2. Supported MDI Pair Combinations

RJ-45 Pin Pairings				
1, 2	**3, 6**	**4, 5**	**7, 8**	**Mode**
A	B	C	D	Normal MDI
B	A	D	C	Normal MDI-X
A	B	D	C	Normal MDI with pair swap on C and D pair
B	A	C	D	Normal MDI-X with pair swap on C and D pair

Note The VSC8601 device can be configured to perform HP Auto-MDIX even when its auto-negotiation feature is disabled (setting register 0.12 to 0) and the link is forced into 10/100 speeds. To enable this feature, set register 27E.15 = 0.

3.7 Link Speed Downshift

For operation in cabling environments that are incompatible with 1000BASE-T, the VSC8601 device provides an automatic link speed "downshift" option. When enabled, the device automatically changes its 1000BASE-T auto-negotiation advertisement to the next slower speed after a set number of failed attempts at 1000BASE-T.

This is useful in networks using older cable installations that may include only pairs A and B and not pairs C and D.

To configure and monitor link speed downshifting, use register bits 20E.4:1. For more information, see "Extended PHY Control Set 1," page 50.

3.8 Transformerless Ethernet

The Cat5 media interface supports 10/100/1000BT Ethernet for backplane applications such as those specified by the PICMG™ 2.16 and ATCA™ 3.0 specifications for eight-pin channels. With proper AC coupling, the typical Cat5 transformer can be removed and replaced with capacitors.

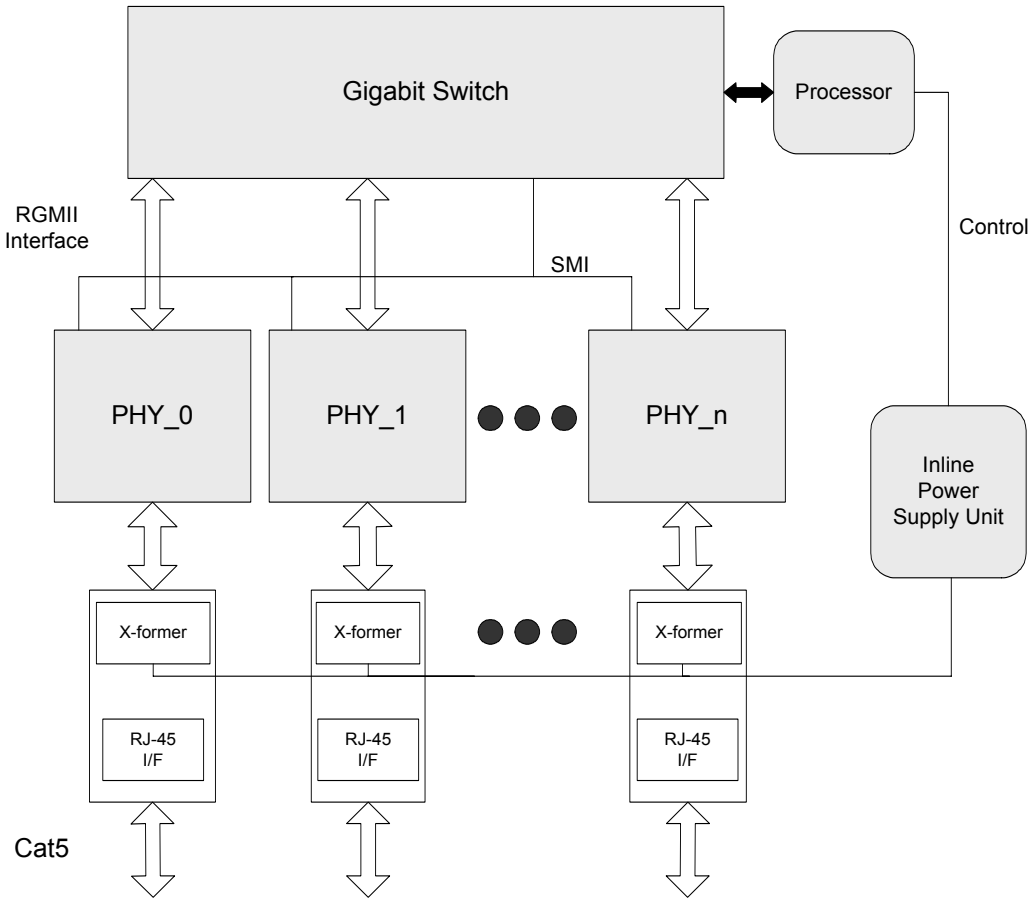
3.9 Ethernet Inline Powered Devices

The VSC8601 device can detect inline powered devices in Ethernet network applications. Its inline powered detection capability can be part of a system that allows for IP-phone and other devices, such as wireless access points, to receive power directly from their Ethernet cable, similar to office digital phones receiving power from a Private Branch Exchange (PBX) office switch over the telephone cabling. This can eliminate the need for an IP-phone to have an external power supply. It also enables the inline powered device to remain active during a power outage (assuming the Ethernet switch is connected to an uninterrupted power supply, battery, back-up power generator, or some other uninterruptible power source).

For more information about inline powered device detection, visit the Cisco Web site at www.cisco.com.

The VSC8601 device is compatible with switch designs that are intended for use in systems that supply power to Data Terminal Equipment (DTE) using the MDI or twisted pair cable, as described in clause 33 of the IEEE standard 802.3af. The following illustration shows an example of this type of application.

Figure 6. Inline Powered Ethernet Switch Diagram



The following procedure describes the process that an Ethernet switch must perform to process inline power requests made by a link partner (LP) that is, in turn, capable of receiving inline power.

1. Enable the inline powered device detection mode on each VSC8601 PHY using its serial management interface. Set register bit 23E.10 to 1.

2. Ensure that the VSC8601 device auto-negotiation enable bit (register 0.12) is also set to 1. In the application, the device sends a special Fast Link Pulse (FLP) signal to the LP. Reading register bit 23E.9:8 returns 00 during the search for devices that require Power-over-Ethernet (PoE).

3. The VSC8601 PHY monitors its inputs for the FLP signal looped back by the LP. An LP capable of receiving PoE will loopback the FLP pulses when it is in a powered-down state. This is reported when VSC8601 device register bit 23E.9:8 reads back 01. It can also be verified as an inline power detection interrupt by

reading VSC8601 device register bit 26.9, which should be a 1, and which is subsequently cleared and the interrupt de-asserted after the read.

If an LP device does not loop back the FLP after a specific time, VSC8601 device register bit 23E.9:8 automatically resets to 10.

4. If the VSC8601 PHY reports that the LP needs PoE, the Ethernet switch must enable inline power on this port, externally of the PHY.

5. The PHY automatically disables inline powered device detection if the VSC8601 device register bit 23E.9:8 automatically resets to 10, and then automatically changes to its normal auto-negotiation process. A link is then auto-negotiated and established when the link status bit is set (register bit 1.2 is set to 1).

6. In the event of a link failure (indicated when VSC8601 device register bit 1.2 reads 0), the inline power should be disabled to the inline powered device external to the PHY. The VSC8601 PHY disables its normal auto-negotiation process and re-enables its inline powered device detection mode.

3.10 ActiPHY Power Management

In addition to the IEEE-specified power-down control bit (device register bit 0.11), the device also includes an ActiPHY™ power management mode for each PHY. This mode enables support for power-sensitive applications such as laptop computers with Wake-on-LAN™ capability. It utilizes a signal-detect function that monitors the media interface for the presence of a link to determine when to automatically power-down the PHY. The PHY “wakes up” at a programmable interval and attempts to “wake up” the link partner PHY by sending a burst of FLP over copper media.

The ActiPHY power management mode in the VSC8601 device can be enabled during normal operation at any time by setting register bit 23.5 to 1.

There are three operating states possible when ActiPHY mode is enabled:

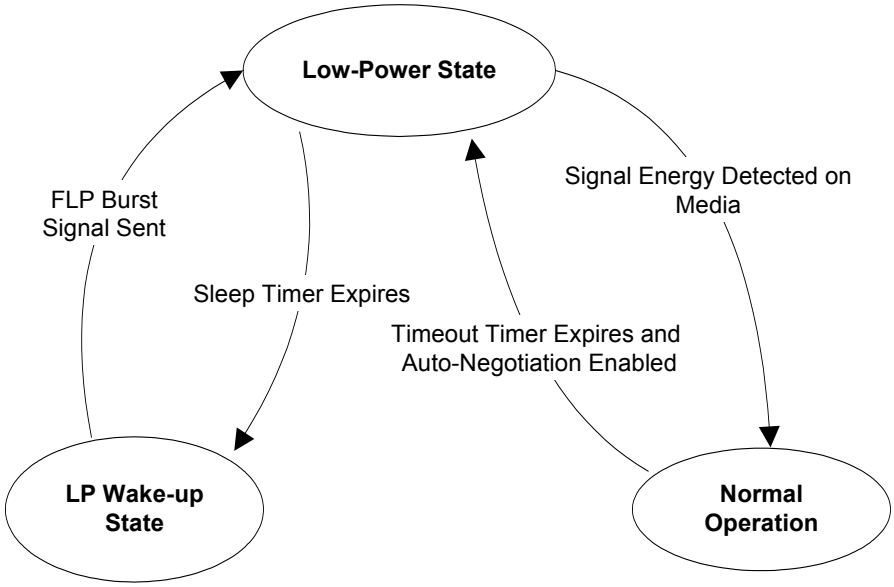
- Low-power state
- LP wake-up state
- Normal operating state (link-up state)

The VSC8601 device switches between the low-power state and LP wake-up state every two seconds until signal energy is detected on the media interface pins. When signal energy is detected, the PHY enters the normal operating state. If the PHY is in its normal operating state and the link fails, the PHY returns to the low-power state after the link status time-out timer has expired. After reset, the PHY enters the low-power state.

When auto-negotiation is enabled in the PHY, the ActiPHY state machine operates as described. If auto-negotiation is disabled and the link is forced to 10BT or 100BTX modes while the PHY is in its low-power state, the PHY continues to transition between the low-power and LP wake-up states until signal energy is detected on the media pins. At that time, the PHY transitions to the normal operating state and stays in that state even when the link is dropped. If auto-negotiation is disabled while the PHY is in the normal operation state, the PHY stays in that state when the link is dropped and does not transition back to the low-power state.

The following illustration shows the relationship between ActiPHY states and timers.

Figure 7. ActiPHY State



3.10.1 Low-Power State

In the low-power state, all major digital blocks are powered down. However, the following functionality is provided:

- SMI interface (MDC, MDIO, MDINT)
- CLKOUT

In this state, the PHY monitors the media interface pins for signal energy. The PHY comes out of low-power state and transitions to the normal operating state when signal energy is detected on the media. This happens when the PHY is connected to one of the following:

- Auto-negotiation capable link partner
- Auto-negotiation incapable (blink/forced) link partner (100BASE-TX or 10BASE-T)
- Another PHY in ActiPHY LP wake-up state

In the absence of signal energy on the media pins, the PHY transitions from the low-power state to the LP wake-up state periodically based on the programmable sleep timer (register bits 20E.14:13). The actual sleep time duration is randomized from –80 ms to +60 ms to avoid two linked PHYs in ActiPHY Mode entering a lock-up state during operation.

3.10.2 Link Partner Wake-Up State

In this state, the PHY attempts to wake up the link partner. FLP bursts are sent on alternating pairs A and B of the Cat5 media for a duration of two seconds.

In this state, the following functionality is provided:

- SMI interface (MDC, MDIO, MDINT)
- CLKOUT

After sending signal energy on the relevant media, the PHY returns to the low-power state.

3.10.3 Normal Operating State

In this state, the PHY establishes a link with a link partner. When the media is unplugged or the link partner is powered down, the PHY waits for the duration of the programmable link status time-out timer, which is set using register bit 28.7 and bit 28.2. It then enters the low-power state.

3.11 Serial Management Interface

The VSC8601 device includes an IEEE 802.3-compliant serial management interface (SMI) that is affected by use of its MDC and MDIO pins. The SMI provides access to device control and status registers. The register set that controls the SMI consists of 32 16-bit registers, including all required IEEE-specified registers. Also, there are additional pages of registers accessible by means of device register 31.

For more information, see "Extended Page Registers," page 55.

The SMI is a synchronous serial interface with bidirectional data on the MDIO pin that is clocked on the rising edge of the MDC pin. The interface can be clocked at a rate from 0 MHz to 25 MHz, depending upon the total load on MDIO. An external, 2 kΩ pull-up resistor is required on the MDIO pin.

3.11.1 SMI Frames

Data is transferred over the SMI using 32-bit frames with an optional and arbitrary length preamble. The following illustrations show the SMI frame format for the read operation and write operation.

Figure 8. SMI Read Frame

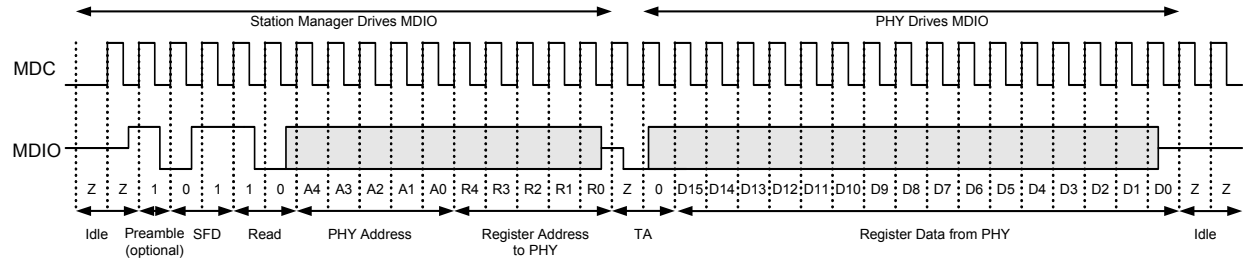
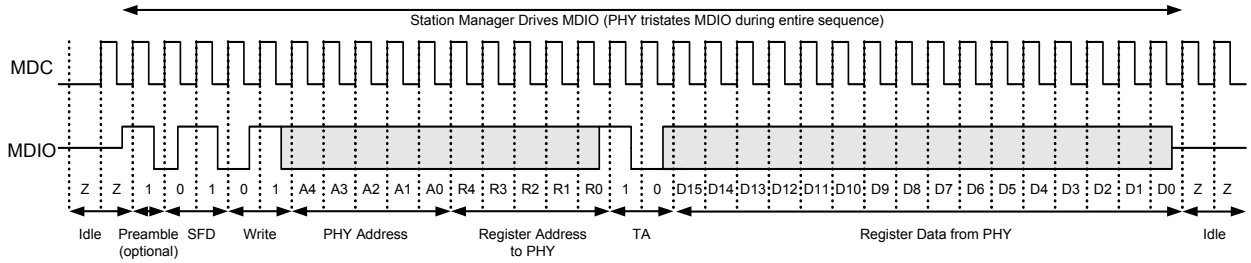


Figure 9. SMI Write Frame



The following provides additional information about the terms used in Figure 8 and Figure 9.

Idle During idle, the MDIO node goes to a high-impedance state. This allows an external pull-up resistor to pull the MDIO node up to a logical 1 state. Because the idle mode should not contain any transitions on MDIO, the number of bits is undefined during idle.

Preamble By default, preambles are not expected nor required. The preamble is a string of ones. If it exists, the preamble must be at least one bit; otherwise, it may be of an arbitrary length.

Start of Frame (SFD) A pattern of 01 indicates the start of frame. If the pattern is not 01, all following bits are ignored until the next preamble pattern is detected.

Read or Write Opcode A pattern of 10 indicates a read. A pattern of 01 indicates a write. If these bits are not either 01 or 10, all following bits are ignored until the next preamble pattern is detected.

PHY Address The VSC8601 responds to a message frame only when the received PHY address matches its physical address. The physical address is five bits long (4:0). The bits are set by the CMODE pins.

Register Address The next five bits are the register address.

Turn-around The two bits used to avoid signal contention when a read operation is performed on the MDIO are called the turn-around (TA) bits. During read operations, the VSC8601 device drives the second TA bit, which is a logical 0.

Data The 16-bits read from or written to the device are considered the data or data stream. When data is read from a PHY, it is valid at the output from one rising edge of

MDC to the next rising edge of MDC. When data is being written to the PHY, it must be valid around the rising edge of MDC.

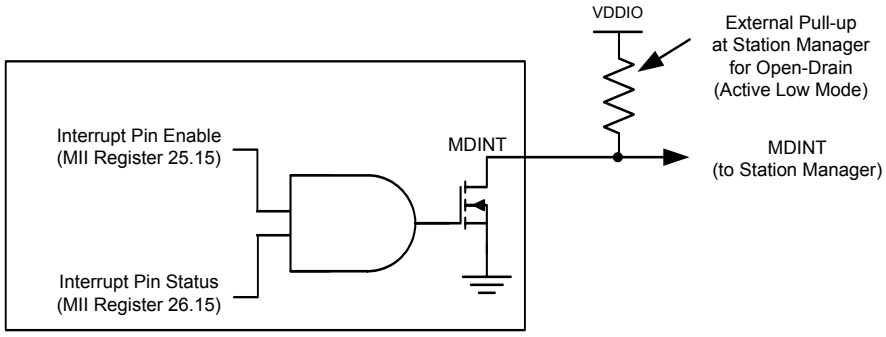
Idle The sequence is repeated.

3.11.2 SMI Interrupts

The SMI also includes an output interrupt signal, MDINT, for signaling the station manager when certain events occur in the PHY.

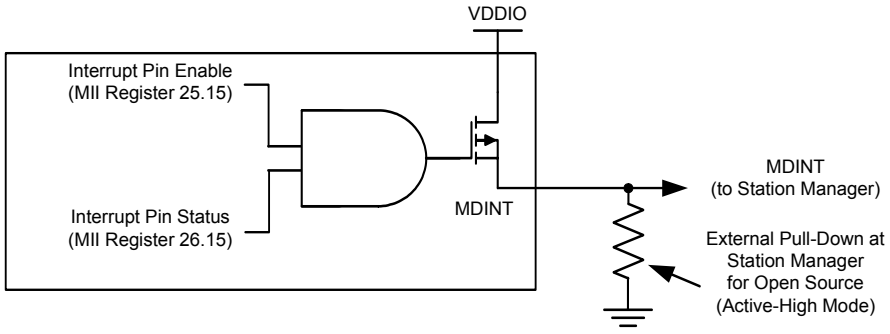
The MDINT pin can be configured for open-drain (active-low) by tying the pin to a pull-up resistor and to VDDIO. The following illustration shows this configuration.

Figure 10. MDINT Configured as an Open-Drain (Active-Low) Pin



Alternatively, each MDINT pin can be configured for open-source (active-high) by tying the pin to a pull-down resistor and to VSS. The following illustration shows this configuration.

Figure 11. MDINT Configured as an Open-Source (Active-High) Pin



When a PHY generates an interrupt, the MDINT pin is asserted (driven high or low, depending on resistor connection) if the interrupt pin enable bit (MII Register 25.15) is set.

3.12 LED Interface

The VSC8601 device drives up to three LEDs directly. All LED outputs are active-low and are driven using 3.3 V from the VDD33 power supply. When active, the pins are mainly used to sink current of the cathode side of an LED, but the pins can also supply source power to the anode portion of LEDs when they are not in the active state. This allows for two LED pins to be used to drive a multi-status, bi-colored LED.

3.12.1 Simple or Enhanced LED Method

The VSC8601 provides two methods for controlling its LEDs: simple or enhanced. The simple LED method is backward-compatible to the LED control found in prior Vitesse Ethernet PHY devices. The simple LED method eases software backward compatibility for customers switching to the VSC8601. The simple LED method is controlled by MII Register 27 and is enabled by default.

For added flexibility, the VSC8601 LED can be controlled using the enhanced LED method. The enhanced LED method is enabled by setting MII Register 17E.4 = 1. When enabled, then the LEDs are controlled by MII Registers 16E and 17E. In this method, the MII Register 27 settings are ignored.

Simple LED Method When MII Register 17E.4 = 0, the LEDs are controlled by the simple LED method. This LED method is enabled on power-up and is controlled by MII Register 27. In this method, MII Register 27 controls the LEDs. For more information, see "LED Control," page 52.

Enhanced LED Method When MII Register 17E.4 = 1, the LEDs are controlled by the enhanced LED method. In this method, MII Register 16E and 17E control the LEDs. For more information, see "Enhanced LED Method Select," page 56 and "Enhanced LED Behavior," page 57.

3.12.2 LED Modes

If you are using the enhanced LED method, there are several LED modes available. They are found in MII Register 16E. Each LED pin can be configured to display different status information. Set the LED mode either by using register 16E or with the CMODE pin setting. The following table summarizes the LED functions.

Note The modes listed in the following table are equivalent to the setting used in register 16E to configure each LED pin. For the LED states listed, 1 = pin held high (de-asserted), 0 = pin held low (asserted), and blink/pulse-stretch is dependent on the LED behavior setting in register 17E.

Table 3. LED Mode and Function Summary

Mode	Function Name	LED State and Description
0	Link/activity	1 = No link in any speed on any media interface. 0 = Valid link at any speed on any media interface. Blink or pulse-stretch = Valid link at any speed on any media interface and with activity present.
1	Link1000/activity	1 = No link in 1000BASE-T. 0 = Valid 1000BASE-T link. Blink or pulse-stretch = Valid 1000BASE-T link with activity present.

Table 3. LED Mode and Function Summary *(continued)*

Mode	Function Name	LED State and Description
2	Link100/activity	1 = No link in 100BASE-TX. 0 = Valid 100BASE-TX link. Blink or pulse-stretch = Valid 100BASE-TX link with activity present.
3	Link10/activity	1 = No link in 10BASE-T. 0 = Valid 10BASE-T link. Blink or pulse-stretch = Valid 10BASE-T link with activity present.
4	Link100/1000/activity	1 = No link in 100BASE-TX or 1000BASE-T. 0 = Valid 100BASE-TX or 1000BASE-T link. Blink or pulse-stretch = Valid 100BASE-TX or 1000BASE-T link with activity present.
5	Link10/1000/activity	1 = No link in 10BASE-T or 1000BASE-T. 0 = Valid 10BASE-T or 1000BASET-T link. Blink or pulse-stretch = Valid 10BASE-T or 1000BASE-T link with activity present.
6	Link10/100/activity	1 = No link in 10BASE-T or 100BASE-TX. 0 = Valid 10BASE-T or 100BASE-TX link. Blink or pulse-stretch = Valid 10BASE-T or 100BASE-TX link with activity present.
7	Reserved	
8	Duplex/collision	1 = Link established in half-duplex mode, or no link established. 0 = Link established in full-duplex mode. Blink or pulse-stretch = Link established in half-duplex mode but collisions are present.
9	Collision	1 = No collision detected. Blink or pulse-stretch = Collision detected.
10	Activity	1 = No activity present. Blink or pulse-stretch = Activity present (becomes TX activity present if register bit 30.14 is set to 1).
11	Reserved	
12	Auto-negotiation fault	1 = No auto-negotiation fault present. 0 = Auto-negotiation fault occurred.
13	Reserved	
14	Force LED off	1 = De-asserts the LED.
15	Force LED on	0 = Asserts the LED.

3.12.3 LED Behavior

Several LED behaviors can be programmed into the VSC8601 device. Use the settings in register 17E to program LED behavior, which includes the following:

LED Combine Enables an LED to display status for a combination of primary and secondary modes. This can be enabled or disabled for each LED pin. For example, a copper link running in 1000BASE-T mode and activity present can be displayed with one LED by configuring an LED pin to Link1000/Activity mode. The LED asserts when linked to a 1000BASE-T partner and also blinks or pulse-stretches when activity is either transmitted by the PHY or received by the link partner. The combine feature when disabled only allows status of the primary function selected. In this example, only Link1000 asserts the LED, and the secondary mode, activity, does not display if the combine feature is disabled.

LED Blink or Pulse-Stretch This behavior is used for activity and collision indication. This can be uniquely configured for each LED pin. Activity and collision events can occur randomly and intermittently throughout the link-up period. For activity or collision to be visually seen, these two modes are provided. Blink is a 50% duty cycle oscillation of asserting and de-asserting an LED pin. Pulse-stretch guarantees that an LED is asserted and de-asserted for a specific period of time when activity is either present or not present. These rates can also be configured using a register setting.

Rate of LED Blink or Pulse-Stretch This controls the LED blink rate or pulse-stretch length when blink/pulse-stretch is enabled on an LED pin. The blink rate, which alternates between a high and low voltage level at a 50% duty cycle, can be set to 2.5 Hz, 5 Hz, 10 Hz, or 20 Hz. For pulse-stretch, this can be set to 50 ms, 100 ms, 200 ms, or 400 ms.

LED Pulsing Enable To provide additional power savings, the LEDs (when asserted) can be pulsed at 5 kHz, 20% duty cycle.

3.13 Testing Features

The VSC8601 device includes several testing features designed to make it easier to perform system-level debugging and in-system production testing. This section describes the available features.

3.13.1 Ethernet Packet Generator (EPG)

The device EPG can be used at each of the 10/100/1000BASE-T speed settings to isolate problems between the MAC and the VSC8601 device, or between a locally connected PHY and its remote link partner. Enabling the EPG feature effectively disables all MAC interface transmit pins and selects the EPG as the source for all data transmitted onto the twisted pair interface.

Note The EPG is intended for use with laboratory or in-system testing equipment only. Do not use the EPG testing feature when the VSC8601 device is connected to a live network.

To enable the VSC8601 device EPG feature, set the device register bit 29E.15 to 1.

When the EPG is enabled, packet loss occurs during transmission of packets from the MAC to the PHY. However, the PHY receive output pins to the MAC are still active when

the EPG is enabled. If it is necessary to disable the MAC receive pins as well, set register bit 0.10 to 1.

When the device register bit 29E.14 is set to 1, the PHY begins transmitting Ethernet packets based on the settings in registers 29E and 30E. These registers set:

- Source and destination addresses for each packet
- Packet size
- Inter-packet gap
- FCS state
- Transmit duration
- Payload pattern

If register bit 29E.13 is set to 0, register bit 29E.14 is cleared automatically after 30,000,000 packets are transmitted.

3.13.2 CRC Counters

Two separate cyclical redundancy checking (CRC) counters are available in the VSC8601 device. There is a 14-bit CRC good counter available in register bits 18E.13:0 and a separate 8-bit CRC error counter available in register bits 23E.7:0.

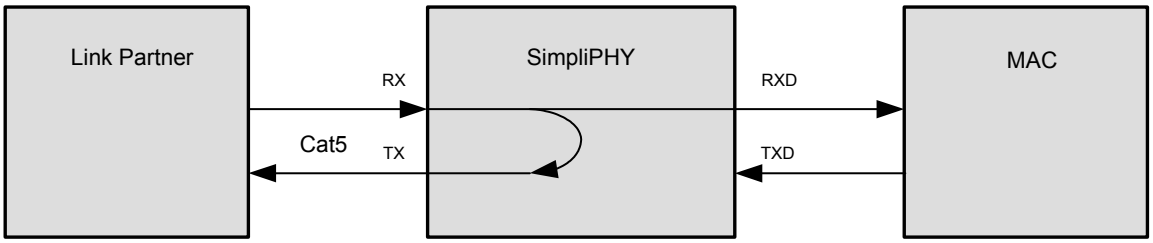
The device CRC counters operate in 10/100/1000BASE-T testing as follows:

- After receiving a packet on the media interface, register bit 18E.15 is set and cleared after being read. The packet then is counted by either the CRC good counter or the CRC error counter. Both CRC counters are also automatically cleared when read.
- The CRC good counter's highest value is 9,999 packets. Upon receiving the next packet, the counter clears and continues to count additional packets beyond that value. The CRC error counter saturates when it reaches its maximum counter limit of 255 packets.

3.13.3 Far-end Loopback

The far-end loopback testing feature is enabled by setting register bit 27E.10 to 1. When enabled, it forces incoming data from a link partner on the current media interface to be retransmitted back to the link partner on the media interface as shown in the following illustration. In addition, the incoming data also appears on the receive data pins of the MAC interface. Data present on the transmit data pins of the MAC interface is ignored when using this testing feature.

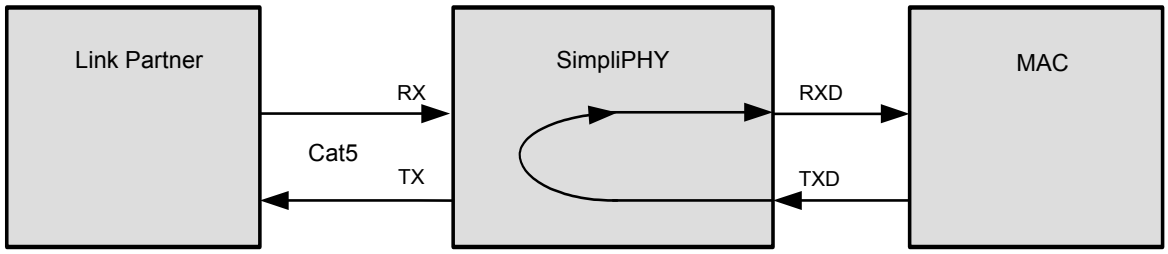
Figure 12. Far-End Loopback



3.13.4 Near-End Loopback

When the near-end loopback testing feature is enabled (by setting the device register bit 0.14 to 1), data on the transmit data pins (TXD) is looped back onto the device received data pins (RXD) as illustrated in the following illustration. When using this testing feature, no data is transmitted over the network.

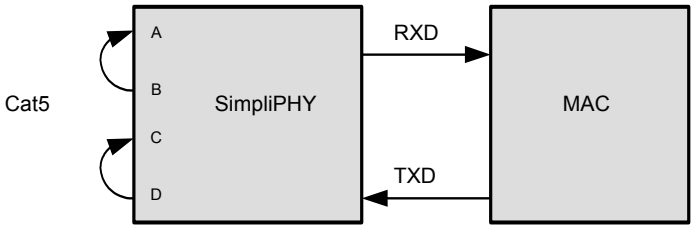
Figure 13. Near-End Loopback



3.13.5 Connector Loopback

The connector loopback testing feature allows for the twisted pair interface to be looped back externally. When using this feature, the PHY must be connected to a loopback connector or a loopback cable. Pair A should be connected to pair B and pair C to pair D, as shown in the following illustration. The connector loopback feature functions at all available interface speeds.

Figure 14. Connector Loopback



When using the connector loopback testing feature, the device auto-negotiation, speed, and duplex configuration is set using device registers 0, 4, and 9. For 1000BASE-T

connector loopback, only the following additional writes are required. Execute the additional writes in the following order:

1. Enable the 1000BASE-T connector loopback. Set register bit 24.0 to 1.

2. Disable the pair swap correction. Set register bit 18.5 to 1.

3.13.6 VeriPHY Cable Diagnostics

The VSC8601 device includes a comprehensive suite of cable diagnostic functions that are available using SMI reads and writes. These functions enable a variety of cable operating conditions and status to be accessed and checked. The VeriPHY suite has the ability to identify the cable length and operating conditions and to isolate a variety of common faults that can occur on the Cat5 twisted pair cabling.

For more information, refer to the *PHY API Software and Programmers Guide* on the Vitesse Web site at www.vitesse.com.

Note If a link is established on the twisted pair interface in 1000BASE-T mode, VeriPHY can run without disrupting the link or any data transfer. However, if a link is established in 100BASE-TX or 10BASE-T, VeriPHY causes the link to drop while the diagnostics are running. After the diagnostics are finished, the link is then re-established.

The following diagnostic functions are part of the VeriPHY suite:

- Detection of coupling between cable pairs
- Detection of cable pair termination
- Determination of cable length

Coupling Between Cable Pairs Shorted wires, improper termination, or high crosstalk resulting from an incorrect wire map can cause error conditions, such as anomalous coupling between cable pairs. These conditions can all prevent the device from establishing a link at any speed.

Cable Pair Termination Proper termination of Cat5 cable requires 100-Ω differential impedance between the positive and negative cable terminals. The IEEE standard 802.3 allows for a termination of as high as 115 Ω or as low as 85 Ω. If the termination falls outside of this range, it is reported by the VeriPHY diagnostics as an anomalous termination. The diagnostics can also determine the presence of an open or shorted cable pair.

Cable Length When the Cat5 cable in an installation is properly terminated, VeriPHY reports the approximate cable length in meters.

3.13.7 IEEE 1149.1 JTAG Boundary Scan

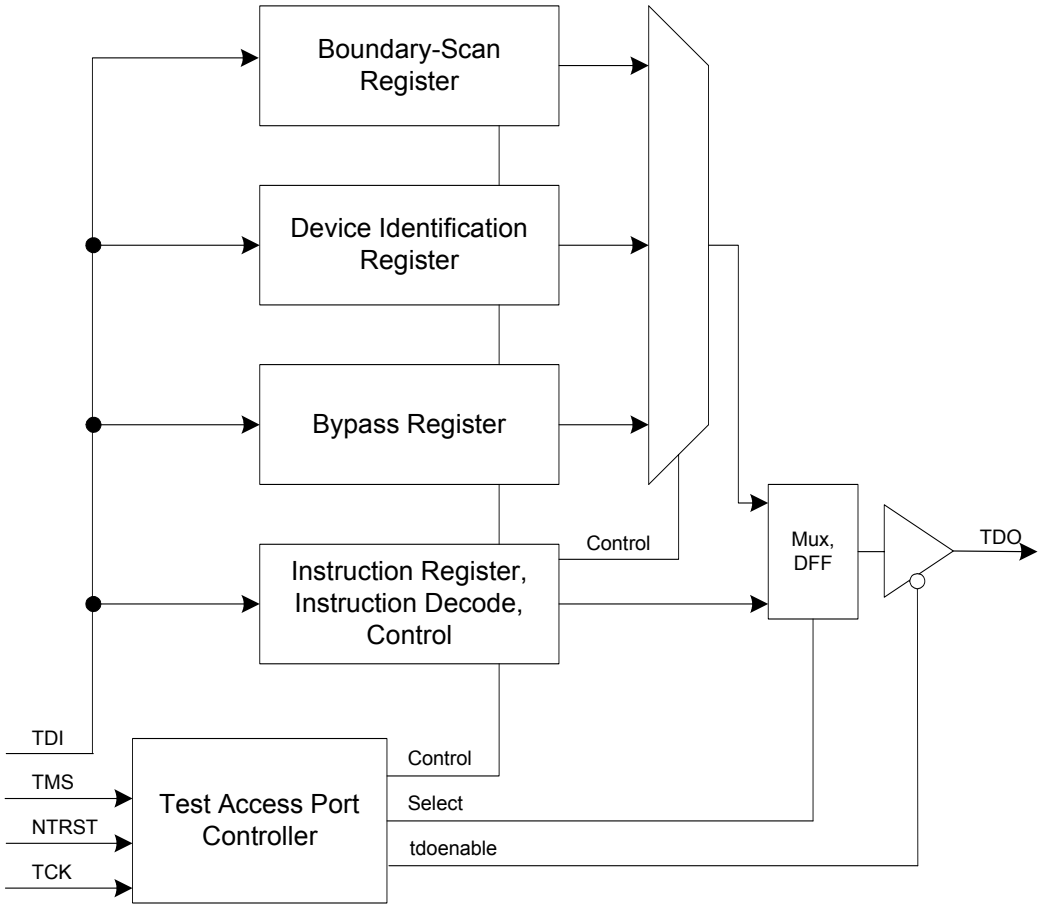
The VSC8601 device supports the Test Access Port (TAP) and boundary-scan architecture described in the IEEE standard 1149.1. The device includes an IEEE 1149.1-compliant test interface, often referred to as a “JTAG TAP Interface.”

The JTAG boundary-scan logic on the VSC8601 device, accessed using its TAP interface, consists of a boundary-scan register and other logic control blocks. The TAP controller

includes all IEEE-required signals (TMS, TCK, TDI, and TDO), in addition to the optional asynchronous reset signal NTRST.

The following illustration shows the TAP and boundary-scan architecture.

Figure 15. Test Access Port and Boundary-Scan Architecture



After a TAP reset, the Device Identification register is serially connected between TDI and TDO by default. The TAP Instruction register is loaded either from a shift register (when a new instruction is shifted in) or, if there is no new instruction in the shift register, a default value of 0110 (IDCODE) is loaded. Using this method, there is always a valid code in the instruction register, and the problem of toggling instruction bits during a shift is avoided. Unused codes are mapped to the BYPASS instruction.

3.13.8 JTAG Instruction Codes

The VSC8601 device supports the following instruction codes:

EXTEST Allows testing of off-chip circuitry and board-level interconnections by sampling input pins and loading data onto output pins. Outputs are driven by the contents of the boundary-scan cells, which have to be updated with valid values (with the PRELOAD instruction) prior to the EXTEST instruction.

SAMPLE/PRELOAD Allows a snapshot of inputs and outputs during normal system operation to be taken and examined. It also allows data values to be loaded into the boundary-scan cells prior to the selection of other boundary-scan test instructions.

IDCODE Provides the version number (bits 31:28), part number (bits 27:12), and the manufacturer identity (bits 11:1) to be serially read from the device.

The following table provides information about the meaning of IDCODE binary values stored in the device JTAG registers.

Table 4. JTAG Device Identification Register Description

Description	Device Version Number	Model Number	Manufacturing Identity	LSB
Bit field	31 through 28	27 through 12	11 through 1	0
Binary value	0001	1000 0110 0000 0001	000 0111 0100	1

CLAMP Allows the state of the signals driven from the component pins to be determined from the boundary-scan register while the bypass register is selected as the serial path between TDI and TDO. While the CLAMP instruction is selected, the signals driven from the component pins do not change.

HIGHZ Places the component in a state in which all of its system logic outputs are placed in a high impedance state. In this state, an in-circuit test system may drive signals onto the connections normally driven by a component output without incurring a risk of damage to the component. This makes it possible to use a board where not all of the components are compatible with the IEEE 1149.1 standard.

BYPASS The bypass register contains a single shift-register stage and is used to provide a minimum-length serial path (one TCK clock period) between TDI and TDO to bypass the device when no test operation is required.

The following table provides more information about the location and IEEE compliance of the JTAG instruction codes used in the VSC8601.

Table 5. JTAG Interface Instruction Codes

Instruction	Code	Selected Register	Register Width	IEEE 1149.1 Specification
EXTEST	0000	Boundary-scan	45	Mandatory
SAMPLE/PRELOAD	0001	Boundary-scan	45	Mandatory
IDCODE	0110	Device identification	32	Optional
CLAMP	0010	Bypass register	1	Optional
HIGHZ	0011	Bypass register	1	Optional
BYPASS	1111	Bypass register	1	Mandatory
RESERVED	0100, 0101, 0111, 1000-1110			

3.13.9 Boundary-Scan Register Cell Order

All inputs and outputs are observed in the boundary-scan register cells. All outputs are additionally driven by the contents of boundary-scan register cells. Bidirectional pins have all three related boundary-scan register cells: input, output, and control.

The complete boundary-scan cell order is available as a BSDL file format on the Vitesse Web site at www.vitesse.com.

4 Configuration

The VSC8601 device can be configured using three different methods:

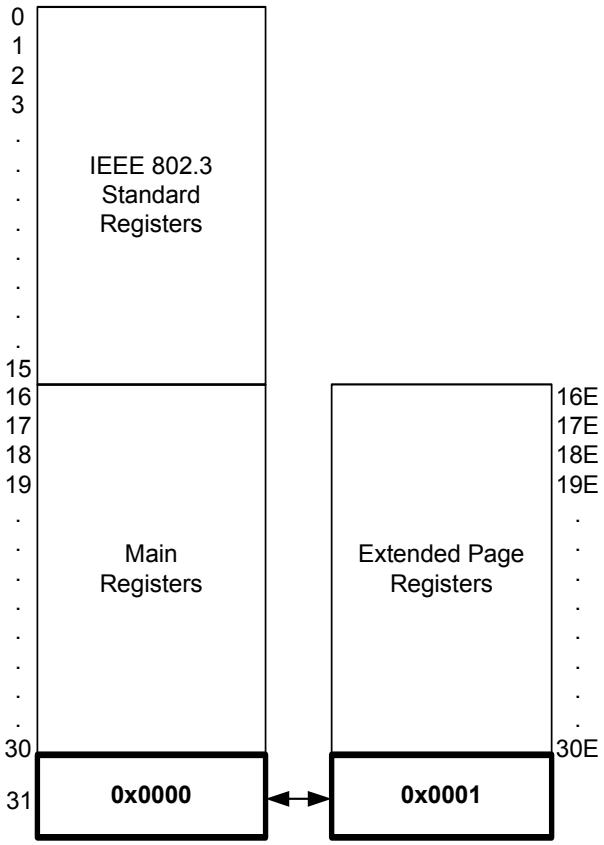
- Setting internal memory registers using the management interface.
- Setting a combination of CMODE pins and registers.
- Loading a configuration into an external EEPROM and connecting that device so that it writes configuration information at system startup.

4.1 Registers

This section provides information about how to configure the VSC8601 device using its internal memory registers and the management interface. For information about configuring the device using the CMODE pins, see "CMODE," page 64. For information about setting up an external EEPROM to perform startup configuration, see "EEPROM," page 66.

The following illustration shows the relationship between the device registers and their address spaces.

Figure 16. Register Space Diagram



4.1.1 Reserved Registers

For main registers 16 through 31 and extended page registers 16E through 30E, any bits marked as “Reserved” should be processed as read only and their states as undefined.

4.1.2 Reserved Bits

In writing to registers with reserved bits, use a “read-modify-then-write” technique, where the entire register is read but only the intended bits to be changed are modified. Reserved bits cannot be changed and their read state cannot be considered static or unchanging.

4.2 IEEE Standard and Main Registers

In the VSC8601 device, the standard registers’ page space consists of the IEEE standard registers and the Vitesse standard registers. The following table lists the names of the registers associated with the addresses as dictated by the IEEE standard.

Table 6. IEEE 802.3 Standard Registers

Register Address	Register Name
0	Mode control
1	Mode status
2	PHY identifier 1
3	PHY identifier 2
4	Auto-negotiation advertisement
5	Auto-negotiation link partner ability
6	Auto-negotiation expansion
7	Auto-negotiation next-page transmit
8	Auto-negotiation link partner next-page receive
9	1000BASE-T control
10	1000BASE-T status
11	Reserved
12	Reserved
13	Reserved
14	Reserved
15	1000BASE-T status extension 1

The following table lists the names of the registers in the main page space of the device. These registers are accessible only when register address 31 is set to 0x0000.

Table 7. Main Registers

Register Address	Register Name
16	100BASE-TX status extension
17	1000BASE-T status extension 2

Table 7. Main Registers *(continued)*

Register Address	Register Name
18	Bypass control
19	Receive error counter
20	False carrier sense counter
21	Disconnect counter
22	Extended control and status
23	Extended PHY control 1
24	Extended PHY control 2
25	Interrupt mask
26	Interrupt status
27	LED control
28	Auxiliary control and status
29	Delay skew status
30	Reserved
31	Extended register page access

4.2.1 Mode Control

The device register at memory address 0.00.15:0 controls several aspects of VSC8601 functionality. The following table lists the available bit settings in this register and what they control.

Table 8. Mode Control, Address 0 (0x00)

Bit	Name	Access	Description	Default
15	Software reset	R/W	This is a self-clearing bit that restores all serial management interface (SMI) registers to their default state, except for sticky and super sticky bits. 1 = Reset asserted. 0 = Reset de-asserted. You must wait 4 µs after setting this bit to initiate another SMI register access.	0
14	Loopback	R/W	1 = Loopback enabled. 0 = Loopback disabled. When loop back is enabled, the device functions at the current speed setting and with the current duplex mode setting (bit 8 of this register).	0
13, 6	Forced speed selection	R/W	LSB = bit 13, MSB = bit 6. 00 = 10 Mbps. 01 = 100 Mbps. 10 = 1000 Mbps. 11 = Reserved.	10
12	Auto-negotiation enable	R/W	1 = Auto-negotiation enabled. 0 = Auto-negotiation disabled.	1

Table 8. Mode Control, Address 0 (0x00) *(continued)*

Bit	Name	Access	Description	Default
11	Power-down	R/W	1 = Power-down enabled. If power-down is enabled, the RGMII's in-band signaling is disabled. When this bit is set, RGMII in-band signaling does not function.	0
10	Isolate	R/W	1 = Disable MAC interface outputs and ignore MAC interface inputs.	0
9	Restart auto-negotiation	R/W	This is a self-clearing bit. 1 = Restart auto-negotiation on media interface.	0
8	Duplex	R/W	1 = Full-duplex. 0 = Half-duplex.	0
7	Collision test enable	R/W	1 = Collision test enabled.	0
6	MSB for speed selection	R/W	See bit 13 above.	1
5:0	Reserved			000000

4.2.2 Mode Status

The register at 1.01.15:0 in the device main registers space displays the currently enabled mode setting. The following table lists possible readouts of this register.

Table 9. Mode Status, Address 1 (0x01)

Bit	Name	Access	Description	Default
15	100BASE-T4 capability	RO	1 = 100BASE-T4 capable.	0
14	100BASE-X FDX capability	RO	1 = 100BASE-X FDX capable.	1
13	100BASE-X HDX capability	RO	1 = 100BASE-X DDX capable.	1
12	10BASE-T FDX capability	RO	1 = 10BASE-T FDX capable.	1
11	10BASE-T HDX capability	RO	1 = 10BASE-T HDX capable.	1
10	100BASE-T2 FDX capability	RO	1 = 100BASE-T2 FDX capable.	0
9	100BASE-T2 HDX capability	RO	1 = 100BASE-T2 HDX capable.	0
8	Extended status enable	RO	1 = Extended status information present in register 15.	1
7	Reserved	RO		0
6	Preamble suppression capability	RO	1 = MF preamble may be suppressed. 0 = MF always required.	1
5	Auto-negotiation complete	RO	1 = Auto-negotiation complete.	0

Table 9. Mode Status, Address 1 (0x01) *(continued)*

Bit	Name	Access	Description	Default
4	Remote fault	RO	This bit latches high. 1 = Far-end fault detected.	0
3	Auto-negotiation capability	RO	1 = Auto-negotiation capable.	1
2	Link status	RO	This bit latches low. 1 = Link is up.	0
1	Jabber detect	RO	This bit latches high. 1 = Jabber condition detected.	0
0	Extended capability	RO	1 = Extended register capable.	1

4.2.3 Device Identification

All 16 bits in both register 2 and register 3 in the VSC8601 device are used to provide information associated with aspects of the device identification. The following tables list the possible readouts.

Table 10. Identifier 1, Address 2 (0x02)

Bit	Name	Access	Description	Default
15:0	Organizationally unique identifier (OUI)	RO	OUI most significant bits (3:18)	0x0007

Table 11. Identifier 2, Address 3 (0x03)

Bit	Name	Access	Description	Default
15:10	OUI	RO	OUI least significant bits (19:24)	0x0001
9:4	Vitesse model number	RO	VSC8601	000010
3:0	Device revision number	RO		0001

4.2.4 Auto-Negotiation Advertisement

The bits in address 4 in the main registers space control the VSC8601 device ability to notify other devices of the status of its auto-negotiation feature. The following table lists the available settings and readouts.

Table 12. Device Auto-Negotiation Advertisement, Address 4 (0x04)

Bit	Name	Access	Description	Default
15	Next page transmission request	R/W	1 = Request enabled	0
14	Reserved	RO		0
13	Transmit remote fault	R/W	1 = Enabled	0

Table 12. Device Auto-Negotiation Advertisement, Address 4 (0x04)

Bit	Name	Access	Description	Default
12	Reserved technologies	R/W		0
11	Advertise asymmetric pause	R/W	1 = Advertises asymmetric pause	CMODE
10	Advertise symmetric pause	R/W	1 = Advertises symmetric pause	CMODE
9	Advertise 100BASE-T4	R/W	1 = Advertises 100BASE-T4	0
8	Advertise 100BASE-TX FDX	R/W	1 = Advertise 100BASE-TX FDX	CMODE
7	Advertise 100BASE-TX HDX	R/W	1 = Advertises 100BASE-TX HDX	CMODE
6	Advertise 10BASE-T FDX	R/W	1 = Advertises 10BASE-T FDX	CMODE
5	Advertise 10BASE-T HDX	R/W	1 = Advertises 10BASE-T HDX	CMODE
4:0	Advertise selector	R/W		00001

4.2.5 Link Partner Auto-Negotiation Capability

The bits in main register 5 enable you to determine if the Cat5 link partner (LP) used with the VSC8601 device is compatible with the auto-negotiation functionality.

Table 13. Auto-Negotiation Link Partner Ability, Address 5 (0x05)

Bit	Name	Access	Description	Default
15	LP next page transmission request	RO	1 = Requested	0
14	LP acknowledge	RO	1 = Acknowledge	0
13	LP remote fault	RO	1 = Remote fault	0
12	Reserved	RO		0
11	LP advertise asymmetric pause	RO	1 = Capable of asymmetric pause	0
10	LP advertise symmetric pause	RO	1 = Capable of symmetric pause	0
9	LP advertise 100BASE-T4	RO	1 = Capable of 100BASE-T4	0
8	LP advertise 100BASE-TX FDX	RO	1 = Capable of 100BASE-TX FDX	0
7	LP advertise 100BASE-TX HDX	RO	1 = Capable of 100BASE-TX HDX	0
6	LP advertise 10BASE-T FDX	RO	1 = Capable of 10BASE-T FDX	0
5	LP advertise 10BASE-T HDX	RO	1 = Capable of 10BASE-T HDX	0
4:0	LP advertise selector	RO		00000

4.2.6 Auto-Negotiation Expansion

The bits in main register 6 work together with those in register 5 to indicate the status of the LP auto-negotiation. The following table lists the available settings and readouts.

Table 14. Auto-Negotiation Expansion, Address 6 (0x06)

Bit	Name	Access	Description	Default
15:5	Reserved	RO		00000000000
4	Parallel detection fault	RO	This bit latches high. 1 = Parallel detection fault.	0
3	LP next page capable	RO	1 = LP is next page capable.	0
2	Local PHY next page capable	RO	1 = Local PHY is next page capable.	1
1	Page received	RO	This bit latches low. 1 = New page has been received.	0
0	LP is auto-negotiation capable	RO	1 = LP is capable of auto-negotiation.	0

4.2.7 Transmit Auto-Negotiation Next Page

The settings in register 7 in the main registers space provide information about the number of pages in an auto-negotiation sequence. The following table lists the settings available.

Table 15. Auto-Negotiation Next Page Transmit, Address 7 (0x07)

Bit	Name	Access	Description	Default
15	Next page	R/W	1 = More pages follow	0
14	Reserved	RO		0
13	Message page	R/W	1 = Message page 0 = Unformatted page	1
12	Acknowledge 2	R/W	1 = Complies with request 0 = Cannot comply with request	0
11	Toggle	RO	1 = Previous transmitted LCW = 0 0 = Previous transmitted LCW = 1	0
10:0	Message/unformatted code	R/W		00000000001

4.2.8 Auto-Negotiation Link Partner Next Page Receive

The bits in register 8 of the main register space work together with register 7 to determine certain aspects of the LP auto-negotiation. The following table lists the possible readouts.

Table 16. Auto-Negotiation LP Next Page Receive, Address 8 (0x08)

Bit	Name	Access	Description	Default
15	LP next page	RO	1 = More pages follow	0
14	Acknowledge	RO	1 = LP acknowledge	0
13	LP message page	RO	1 = Message page 0 = Unformatted page	0
12	LP Acknowledge 2	RO	1 = LP complies with request	0
11	LP toggle	RO	1 = Previous transmitted LCW = 0 0 = Previous transmitted LCW = 1	0
10:0	LP message / unformatted code	RO		00000000000

4.2.9 1000BASE-T Control

The VSC8601 device's 1000BASE-T functionality is controlled by the bits in register 9 of the main register space. The following table lists the settings and readouts available.

Table 17. 1000BASE-T Control, Address 9 (0x09)

Bit	Name	Access	Description	Default
15:13	Transmitter test mode	R/W	000 = Normal. 001 = Mode 1: Transmit waveform test. 010 = Mode 2: Transmit jitter test as master. 011 = Mode 3: Transmit jitter test as slave. 100 = Mode 4: Transmitter distortion test. 101 to 111 = Reserved: Operation not defined.	000
12	Master/slave manual configuration	R/W	1 = Master/slave manual configuration enabled.	0
11	Master/slave value	R/W	This register is only valid when bit 9.12 is set to 1. 1 = Configure PHY as master during negotiation. 0 = Configure PHY as slave during negotiation.	0
10	Port type	R/W	1 = Multi-port device. 0 = Single-port device.	0
9	1000BASE-T FDX capability	R/W	1 = PHY is 1000BASE-T FDX capable.	CMODE
8	1000BASE-T HDX capability	R/W	1 = PHY is 1000BASE-T HDX capable.	CMODE
7:0	Reserved	R/W		0x00

Note Transmitter Test Mode (bits 15:13) operates in the manner described in IEEE standard 802.3, section 40.6.1.1.2.

4.2.10 1000BASE-T Status

The bits in register 10 of the main register space allow you to read the status of the 1000BASE-T communications enabled in the device. The following table lists these readouts.

Table 18. 1000BASE-T Status, Address 10 (0x0A)

Bit	Name	Access	Description	Default
15	Master/slave configuration fault	RO	This bit latches high. 1 = Master/slave configuration fault detected. 0 = No master/slave configuration fault detected.	0
14	Master/slave configuration resolution	RO	1 = Local PHY configuration resolved to master. 0 = Local PHY configuration resolved to slave.	1
13	Local receiver status	RO	1 = Local receiver okay.	0
12	Remote receiver status	RO	1 = Remote receiver OK.	0
11	LP 1000BASE-T FDX capability	RO	1 = LP 1000BASE-T FDX capable.	0
10	LP 1000BASE-T HDX capability	RO	1 = LP 1000BASE-T HDX capable.	0
9:8	Reserved	RO		00
7:0	Idle error count	RO	This is a self-clearing bit.	0x00

4.2.11 Main Registers Reserved Addresses

In the VSC8601 device main registers page space, registers 11 through 15 (0x0B through 0x0E) are reserved.

4.2.12 1000BASE-T Status Extension 1

Register 15 provides additional information about the operation of the device 1000BASE-T communications. The following table lists the readouts available.

Table 19. 1000BASE-T Status Extension 1, Address 15 (0x0F)

Bit	Name	Access	Description	Default
15	1000BASE-X FDX capability	RO	1 = PHY is 1000BASE-X FDX capable	0
14	1000BASE-X HDX capability	RO	1 = PHY is 1000BASE-X HDX capable	0
13	1000BASE-T FDX capability	RO	1 = PHY is 1000BASE-T FDX capable	1
12	1000BASE-T HDX capability	RO	1 = PHY is 1000BASE-T HDX capable	1
11:0	Reserved	RO		0x000

4.2.13 100BASE-TX Status Extension

Register 16 in the main registers page space of the VSC8601 device provides additional information about the status of the device's 100BASE-TX operation.

Table 20. 100BASE-TX Status Extension, Address 16 (0x10)

Bit	Name	Access	Description	Default
15	100BASE-TX descrambler	RO	1 = Descrambler locked.	0
14	100BASE-TX lock error	RO	This is a self-clearing bit. 1 = Lock error detected.	0
13	100BASE-TX disconnect state	RO	This is a self-clearing bit. 1 = PHY 100BASE-TX link disconnect detected.	0
12	100BASE-TX current link status	RO	1 = PHY 100BASE-TX link active.	0
11	100BASE-TX receive error	RO	This is a self-clearing bit. 1 = Receive error detected.	0
10	100BASE-TX transmit error	RO	This is a self-clearing bit. 1 = Transmit error detected.	0
9	100BASE-TX SSD error	RO	This is a self-clearing bit. 1 = Start-of-stream delimiter error detected.	0
8	100BASE-TX ESD error	RO	This is a self-clearing bit. 1 = End-of-stream delimiter error detected.	0
7:0	Reserved	RO		

4.2.14 1000BASE-T Status Extension 2

The second status extension register is at address 17 in the device main registers space. It provides information about another set of parameters associated with 1000BASE-T communications. For information about the first status extension register, see Table 20, page 46. The following table lists the settings available.

Table 21. 1000BASE-T Status Extension 2, Address 17 (0x11)

Bit	Name	Access	Description	Default
15	1000BASE-T descrambler	RO	1 = Descrambler locked.	0
14	1000BASE-T lock error	RO	This is a self-clearing bit. 1 = Lock error detected.	0
13	1000BASE-T disconnect state	RO	This is a self-clearing bit. 1 = PHY 1000BASE-T link disconnect detected.	0
12	1000BASE-T current link status	RO	1 = PHY 1000BASE-T link active.	0
11	1000BASE-T receive error	RO	This is a self-clearing bit. 1 = Receive error detected.	0
10	1000BASE-T transmit error	RO	This is a self-clearing bit. 1 = Transmit error detected.	0

Table 21. 1000BASE-T Status Extension 2, Address 17 (0x11) *(continued)*

Bit	Name	Access	Description	Default
9	1000BASE-T SSD error	RO	This is a self-clearing bit. 1 = Start-of-stream delimiter error detected.	0
8	1000BASE-T ESD error	RO	This is a self-clearing bit. 1 = End-of-stream delimiter error detected.	0
7	1000BASE-T carrier extension error	RO	This is a self-clearing bit. 1 = Carrier extension error detected.	0
6	Non-compliant BCM5400 detected	RO	1 = Non-compliant BCM5400 detected.	0
5	MDI crossover error	RO	1 = MDI crossover error detected.	0
4:0	Reserved	RO		

4.2.15 Bypass Control

The bits in the Bypass Control register in the VSC8601 device control aspects of functionality in effect when the device is disabled so that traffic can bypass it in your design. The following table lists the settings available.

Table 22. Bypass Control, Address 18 (0x12)

Bit	Name	Access	Description	Default
15	Transmit disable	R/W	1 = PHY transmitter disabled.	0
14:9	Reserved	RO		
8	1000BASE-T transmitter test clock	R/W	1 = Enabled.	0
7	Force non-compliant BCM5400 detection	R/W	This is a sticky bit. 1 = Force non-compliant BCM5400 detection.	0
6	Non-compliant BCM5400 detection disable	R/W	This is a sticky bit. 1 = Non-compliant BCM5400 detection disable.	1
5	Disable pair swap correction	R/W	This is a sticky bit. 1 = Disable the automatic pair swap correction.	0
4	Disable polarity correction	R/W	This is a sticky bit. 1 = Disable polarity inversion correction on each subchannel.	0
3	Parallel detect control	R/W	This is a sticky bit. 1 = Do not ignore advertised ability. 0 = Ignore advertised ability.	1
2	Reserved	RO		
1	Disable automatic 1000BASE-T next page exchange	R/W	This is a sticky bit. 1 = Disable automatic 1000BASE-T next page exchanges.	0
0	CLKOUT output enable	R/W	This is a sticky bit. 1 = Enable clock output pin.	CMODE

Note If bit 1 is set to 1 in this register, automatic exchange of next pages is disabled, and control is returned to the user through the SMI after the base page is exchanged. The user then must send the correct sequence of next pages to the link partner, determine the common capabilities, and force the device into the correct configuration following the successful exchange of pages.

4.2.16 Receive Error Counter

The following table lists the readouts you can expect.

Table 23. Receive Error Counter, Address 19 (0x13)

Bit	Name	Access	Description	Default
15:8	Reserved	RO		00000000
7:0	Receive error counter	RO	This is a self-clearing bit. Counts the number of non-collision packets with receive errors since last read. Each time the PHY detects a non-collision packet containing at least one error, these bits are incremented. The counter stops counting at 0FFh. This register is cleared only when read, or upon either a hardware or software reset. These bits are valid only in 100BASE-TX and 1000BASE-T modes.	00000000

4.2.17 False Carrier Sense Counter

The following table lists the readouts you can expect.

Table 24. False Carrier Sense Counter, Address 20 (0x14)

Bit	Name	Access	Description	Default
15:8	Reserved	RO		00000000
7:0	False carrier sense counter	RO	This is a self-clearing bit. Counts the number of false carrier events since last read. The PHY increments these bits each time it detects a false carrier on the receive input. The counter stops counting at 0FFh. This register is cleared only when read, or upon either a hardware or software reset. These bits are valid only in 100BASE-TX and 1000BASE-T modes.	00000000

4.2.18 Disconnect Counter

The following table lists the readouts you can expect.

Table 25. Disconnect Counter, Address 21 (0x15)

Bit	Name	Access	Description	Default
15:8	Reserved	RO		00000000
7:0	Disconnect counter	RO	This is a self-clearing bit. Counts the number of non-collision packets with receive errors after the last read. The PHY increments these bits each time the Carrier Integrity Monitor (CIM) enters the link unstable state. The counter stops counting at 0FFh. This register is cleared only when read or upon a hardware or software reset.	00000000

4.2.19 Extended Control and Status

The bits in register 22 provide additional device control and readouts. The following table lists the settings available.

Table 26. Extended Control and Status, Address 22 (0x16)

Bit	Name	Access	Description	Default
15	Force 10BASE-T link high	R/W	This is a sticky bit. 1 = Bypass link integrity test. 0 = Enable link integrity test.	0
14	Jabber detect disable	R/W	This is a sticky bit. 1 = Disable jabber detect.	0
13	Disable 10BASE-T echo	R/W	This is a sticky bit. 1 = Disable 10BASE-T echo.	1
12	SQE disable mode	R/W	1 = Disable SQE transmit.	1
11:10	10BASE-T squelch control	R/W	This is a sticky bit. 00 = Normal squelch. 01 = Low squelch. 10 = High squelch. 11 = Reserved.	00
9	Reserved			
8	EOF Error	RO	This bit is self-clearing. 1 = EOF error detected.	0
7	10BASE-T disconnect state	RO	This bit is self-clearing. 1 = 10BASE-T link disconnect detected.	0
6	10BASE-T link status	RO	1 = 10BASE-T link active.	0
5:0	Reserved	RO		

The following information applies to the extended control and status bits:

- When bit 15 is set, the link integrity state machine is bypassed and the PHY is forced into a link pass status.

- When bits 11:0 are set to 00, the squelch threshold levels are based on the IEEE standard for 10BASE-T. When set to 01, the squelch level is decreased, which may improve the bit error rate performance on long loops. When set to 10, the squelch level is increased and may improve the bit error rate in high-noise environments.

4.2.20 Extended PHY Control Set 1

The bits in the extended control set control the MAC auto-negotiation functioning, SGMII alignment errors, and EEPROM status. The following table lists the available settings.

Table 27. Extended PHY Control 1, Address 23 (0x17)

Bit	Name	Access	Description	Default
15:9	Reserved	RO		
8	RGMII skew timing compensation enable	R/W	This is a sticky bit. 0 = Disabled. 1 = Adds 2 ns delay to the RX_CLK and TX_CLK pins.	CMODE
7:6	Reserved	RO		
5	ActiPHY mode enable	R/W	This is a sticky bit. 1 = Enabled.	CMODE
4:1	Reserved	RO		
0	Reserved	RO		

Note After configuring bit 12 of the extended PHY control register set 1, a software reset (register 0, bit 15) must be written to change the device operating mode. Bit 1 allows for flexibility in printed circuit board layouts because it can reorder the TXD pins.

4.2.21 Extended PHY Control Set 2

The second set of extended controls is located in register 24 in the main register space for the device. The following table lists the settings and readouts available.

Table 28. Extended PHY Control 2, Address 24 (0x18)

Bit	Name	Access	Description	Default
15:13	100BASE-TX edge rate control	R/W	This is a sticky bit. 011 = +5 Edge rate (slowest). 010 = +4 Edge rate. 001 = +3 Edge rate. 000 = +2 Edge rate. 111 = +1 Edge rate. 110 = Default edge rate. 101 = –1 Edge rate. 100 = –2 Edge rate (fastest).	110
12:4	Reserved	RO		

Table 28. Extended PHY Control 2, Address 24 (0x18) *(continued)*

Bit	Name	Access	Description	Default
3:1	Cable length status	RO	The following are approximate lengths: 000 = < 10 m. 001 = 10—20 m. 010 = 20—40 m. 011 = 40—80 m. 100 = 80—100 m. 101 = 100—140 m. 110 = 140—180 m. 111 = >180 m.	000
0	1000BASE-T connector loopback	R/W	1 = Enabled.	0

4.2.22 Interrupt Mask

The bits in register 25 control the device interrupt mask. The following table lists the settings available.

Table 29. Interrupt Mask, Address 25 (0x19)

Bit	Name	Access	Description	Default
15	MDINT interrupt status enable	R/W	This is a sticky bit. 1 = Enabled.	0
14	Speed state change mask	R/W	This is a sticky bit. 1 = Enabled.	0
13	Link state change mask	R/W	This is a sticky bit. 1 = Enabled.	0
12	FDX state change mask	R/W	This is a sticky bit. 1 = Enabled.	0
11	Auto-negotiation error mask	R/W	1 = Enabled.	0
10	Auto-negotiation complete mask	R/W	This is a sticky bit. 1 = Enabled.	0
9	Inline powered device detect mask	R/W	This is a sticky bit. 1 = Enabled.	0
8:3	Reserved	RO		
2	Link speed downshift detect mask	R/W	This is a sticky bit. 1 = Enabled.	0
1	Master/Slave resolution error mask	R/W	This is a sticky bit. 1 = Enabled.	0
0	Reserved	RO		

Note When bit 25.15 is set, the MDINT pin is enabled. When enabled, the state of this pin reflects the state of bit 26.15. Clearing this bit only inhibits the MDINT pin from being asserted.

4.2.23 Interrupt Status

The status of interrupts already written to the device are available for reading from register 26 in the main registers space. The following table lists the readouts you can expect.

Table 30. Interrupt Status, Address 26 (0x1A)

Bit	Name	Access	Description	Default
15	Interrupt status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
14	Speed state change status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
13	Link state change status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
12	FDX state change status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
11	Auto-negotiation error status	RO	This is a self-clearing bit. 1 = Interrupt pending.	
10	Auto-negotiation complete status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
9	Inline powered device detect status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
8:3	Reserved	RO		
2	Link speed downshift detect status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
1	Master/Slave resolution error status	RO	This is a self-clearing bit. 1 = Interrupt pending.	0
0	Reserved	RO		

The following information applies to the interrupt status bits:

- All set bits in this register are cleared after being read (self-clearing). If bit 26.15 is set, the cause of the interrupt can be read by reading bits 26.14:0.
- For bits 26.14 and 26.12, bit 0.12 must be set for this interrupt to assert.
- For bit 26.2, bits 4.8:5 must be set for this interrupt to assert.

4.2.24 LED Control

If you are using the simple LED method of control, you can control the LEDs using the following settings. If you are using the enhanced LED method, there are different register settings you can use. For information about the enhanced LED register settings, see "Enhanced LED Method Select," page 56.

Table 31. LED Control, Address 27 (0x1B)

Bit	Name	Access	Description	Default
15:14	Reserved	RO		

Table 31. LED Control, Address 27 (0x1B) *(continued)*

Bit	Name	Access	Description	Default
13	Link 100 LED force on (LED2 pin)	R/W	This is a sticky bit. 1 = Forced on. 0 = Default.	0
12	Link 100 LED disable (LED2 pin)	R/W	This is a sticky bit. 1 = Disabled. 0 = Default.	0
11	Link 1000 LED force on (LED1 pin)	R/W	This is a sticky bit. 1 = Forced on. 0 = Default.	0
10	Link 1000 LED disable (LED1 pin)	R/W	This is a sticky bit. 1 = Disabled. 0 = Default.	0
9:8	Reserved	RO		
7	Activity LED force on (LED0 pin)	R/W	This is a sticky bit. 1 = Forced on. 0 = Default.	0
6	Activity LED disable (LED0 pin)	R/W	This is a sticky bit. 1 = Disabled. 0 = Default.	0
5:4	Reserved	RO		
3	LED pulse enable	RW	This is a sticky bit. 0 = Normal operation. 1 = LEDs pulse with a 5 KHz, 20% duty cycle when active.	0
2	Activity LED blink enable	RW	This is a sticky bit. 1 = Enable.	0
1	Activity LED blink rate	RW	This is a sticky bit. 1 = 10 Hz blink rate. 0 = 5 Hz blink rate.	0
0	Reserved	RO		

4.2.25 Auxiliary Control and Status

The following table lists the settings available.

Table 32. Auxiliary Control and Status, Address 28 (0x1C)

Bit	Name	Access	Description	Default
15	Auto-negotiation complete	RO	Duplicate of bit 1.5.	0
14	Auto-negotiation disabled	RO	Inverted duplicate of bit 0.12.	0
13	MDI/MDI-X crossover indication	RO	1 = MDI/MDI-X crossover performed internally.	0
12	CD pair swap	RO	1 = CD pairs are swapped.	0
11	A polarity inversion	RO	1 = Polarity swap on pair A.	0
10	B polarity inversion	RO	1 = Polarity swap on pair B.	0
9	C polarity inversion	RO	1 = Polarity swap on pair C.	0

Table 32. Auxiliary Control and Status, Address 28 (0x1C) *(continued)*

Bit	Name	Access	Description	Default
8	D polarity inversion	RO	1 = Polarity swap on pair D.	0
7:6	Reserved	RO		
5	FDX status	RO	1 = Full duplex. 0 = Half duplex.	0
4:3	Speed status	RO	00 = Speed is 10BASE-T. 01 = Speed is 100BASE-TX. 10 = Speed is 1000BASE-T. 11 = Reserved.	00
2	Reserved	RO		
1	Sticky Reset Enable	R/W	This is a super-sticky bit. 1 = Enabled. When enabled, all MII register bits listed as sticky retain their values during a software reset. 0 = Disabled. When disabled, all MII register bits listed as sticky change to their default values during a software reset. Note that bits listed as super sticky retain their values during a software reset regardless of this setting.	1
0	Reserved	RO		

4.2.26 Delay Skew Status

The following table lists the settings available.

Table 33. Delay Skew Status, Address = 29 (0x1D)

Bit	Name	Access	Description	Default
15	Reserved	RO		
14:12	Pair A delay skew	RO	Skew in integral symbol times	000
11	Reserved	RO		
10:8	Pair B delay skew	RO	Skew in integral symbol times	000
7	Reserved	RO		
6:4	Pair C delay skew	RO	Skew in integral symbol times	000
3	Reserved	RO		
2:0	Pair D delay skew	RO	Skew in integral symbol times	000

4.2.27 Reserved Address Space

The bits in register 30 (0x1E) are reserved.

4.3 Extended Page Registers

To provide functionality beyond the IEEE802.3-specified 32 registers and main device registers, the VSC8601 device includes an extended set of registers that provide an additional 15 register spaces.

To access the extended page registers (16E through 30E), enable extended register access by writing 0x0001 to register 31. For more information, see Table 35, page 56.

When extended page register access is enabled, reads and writes to registers 16 through 30 affect the extended registers 16E through 30E instead of those same registers in the IEEE-specified register space. Registers 0 through 15 are not affected by the state of the extended page register access.

Writing 0x0000 to register 31 restores the normal register access.

The following table lists the addresses and register names in the extended register page space. These registers are accessible only when the device register 31 is set to 0x0001.

Table 34. Extended Registers Page Space

Register Address	Register Name
16E	Enhanced LED method select
17E	Enhanced LED behavior
18E	CRC good counter
19E	MAC resistor calibration control
20E	Extended PHY control 3
21E	EEPROM interface status and control
22E	EEPROM data read or write
23E	Extended PHY control 4
24E	Reserved
25E	Reserved
26E	Reserved
27E	Extended PHY control 5
28E	RGMII skew control
29E	Ethernet packet generator (EPG) 1
30E	Ethernet packet generator (EPG) 2

4.3.1 Extended Page Access

The register at address 31 controls the access to the extended page registers for the VSC8601 device. The following table lists the settings available.

Table 35. Extended Page Access, Address 31 (0x1F)

Bit	Name	Access	Description	Default
15:0	Extended page register access	R/W	0x0000 = MII register 16 through 30 accesses main register space 0x0001 = MII register 16 through 30 accesses extended register space	0x0000

4.3.2 Enhanced LED Method Select

If you are using the enhanced LED method of control, you can control the LEDs using the following settings. If you are using the simple LED method, there are different register settings you can use. For information about the simple LED register settings, see "LED Control," page 52.

Table 36. Enhanced LED Method Select, Address 16E (0x10)

Bit	Name	Access	Description	Default
15:12	Reserved	RO		
11:8	LED2 mode select	R/W	This is a sticky bit. Select from LED modes 0-15 listed below.	0010
7:4	LED1 mode select	R/W	This is a sticky bit. Select from LED modes 0-15 listed below.	0001
3:0	LED0 mode select	R/W	This is a sticky bit. Select from LED modes 0-15 listed below.	1010

The following table shows the LED functional modes that can be programmed into any of the device's LED outputs. For more information about accessing or reading the status of the outputs, see Table 36, page 56.

Table 37. Available LED Mode Settings

Mode	Bit Setting	LED Indicates
0	0000	Link/Activity
1	0001	Link1000/Activity
2	0010	Link100/Activity
3	0011	Link10/Activity
4	0100	Link100/1000/Activity
5	0101	Link10/1000/Activity
6	0110	Link10/100/Activity
7	0111	Reserved
8	1000	Duplex/Collision
9	1001	Collision
10	1010	Activity

Table 37. Available LED Mode Settings *(continued)*

Mode	Bit Setting	LED Indicates
11	Reserved	
12	1100	Autoneg_Fault
13	Reserved	
14	1110	Force LED off
15	1111	Force LED on

4.3.3 Enhanced LED Behavior

The following table lists the settings available.

Table 38. Enhanced LED Behavior, Address 17E (0x11)

Bit	Name	Access	Description	Default
15:13	Reserved	RO		
12	LED pulsing enable	R/W	This is a sticky bit. 0 = Normal operation. 1 = LEDs pulse with a 5 KHz, 20% duty cycle when active.	0
11:10	LED blink / pulse-stretch rate	R/W	This is a sticky bit. 00 = 2.5 Hz blink rate / 400 ms pulse-stretch. 01 = 5 Hz blink rate / 200 ms pulse-stretch. 10 = 10 Hz blink rate / 100 ms pulse-stretch. 11 = 20 Hz blink rate / 50 ms pulse-stretch.	01
9:8	Reserved	RO		
7	LED2 pulse-stretch / blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	1
6	LED1 pulse-stretch / blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	1
5	LED0 pulse-stretch / blink select	R/W	This is a sticky bit. 1 = Pulse-stretch. 0 = Blink.	1
4	LED mode	R/W	This is a sticky bit. 1 = Enhanced LED method (controlled by MII register 16E and 17E). 0 = Simple LED method (controlled by MII register 27).	0
3	Reserved	RO		
2	LED2 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (Link/Activity, Duplex/Collision). 1 = Disable Combination (Link only, Duplex only).	0

Table 38. Enhanced LED Behavior, Address 17E (0x11) *(continued)*

Bit	Name	Access	Description	Default
1	LED1 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (Link/Activity, Duplex/Collision). 1 = Disable Combination (Link only, Duplex only).	0
0	LED0 combine feature disable	R/W	This is a sticky bit. 0 = Combine enabled (Link/Activity, Duplex/Collision). 1 = Disable Combination (Link only, Duplex only).	0

Note Bit 4 must be set to 1 before register 16E and 17E are enabled for enhanced LED control. If set to 0, then the LED features in 16E and 17E are not relevant. If set to 1, then the LED features in register 27 are not relevant.

4.3.4 CRC Good Counter

Register 31E makes it possible to read the contents of the CRC good counter; the number of CRC routines that have executed successfully. The following table lists the possible readouts.

Table 39. CRC Good Counter, Address 18E (0x12)

Bit	Name	Access	Description	Default
15	Packet since last read	RO	This is a self-clearing bit. 1 = Packet received since last read.	0
14	Reserved	RO		
13:0	CRC good counter contents	RO	This is a self-clearing bit. Counter containing the number of packets with valid CRCs. This counter does not stop counting and will roll over.	0x000

4.3.5 MAC Resistor Calibration Control

The following table lists the settings available.

Table 40. MAC Resistor Calibration Control, Address 19E (0x13)

Bit	Name	Access	Description	Default
15:14	MAC resistor calibration control setting	R/W	This is a sticky bit. 00 = 50 Ω. 01 = 60 Ω. 10 = 30 Ω. 11 = 45 Ω.	CMODE
13:0	Reserved	RO		

4.3.6 Extended PHY Control 3

Register 20E controls the ActiPHY sleep timer, its wake-up timer, the frequency of the CLKOUT signal, and its link speed downshifting feature. The following table lists the settings available.

Table 41. Extended PHY Control 3, Address 20E (0x14)

Bit	Name	Access	Description	Default
15	Reserved	RO		
14:13	ActiPHY sleep timer	R/W	This is a sticky bit. 00 = 1 second. 01 = 2 seconds. 10 = 3 seconds. 11 = 4 seconds.	01
12:11	Reserved	RO		
10:9	ActiPHY link status time-out control	R/W	00 = 1 second. 01 = 2 second. 10 = 3 second. 11 = 4 second.	01
8:6	Reserved	RO		
5	MAC RX_CLK Disable	R/W	1 = RX_CLK is held low. 0 = RX_CLK is in normal operation.	0
4	Enable link speed auto-downshift feature	R/W	This is a sticky bit. 1 = Enable auto link speed downshift from 1000BASE-T.	CMODE
3:2	Link speed auto-downshift control	R/W	This is a sticky bit. 00 = Downshift after two failed 1000BASE-T auto-negotiation attempts. 01 = Downshift after three failed 1000BASE-T auto-negotiation attempts. 10 = Downshift after four failed 1000BASE-T auto-negotiation attempts. 11 = Downshift after five failed 1000BASE-T auto-negotiation attempts.	01
1	Link speed auto-downshift status	RO	0 = No downshift. 1 = Downshift is required or has occurred.	0
0	Reserved	RO		

4.3.7 EEPROM Interface Status and Control

Register 21E is used to affect control over device function when you have incorporated a startup EEPROM into your design.

Table 42. EEPROM Interface Status and Control, Address 21E (0x15)

Bit	Name	Access	Description	Default
15	Reserved	RO		

Table 42. EEPROM Interface Status and Control, Address 21E (0x15)

Bit	Name	Access	Description	Default
14	Re-read EEPROM after software reset	R/W	This is a super-sticky bit. 1 = Contents of EEPROM to be re-read after software reset.	0
13	Enable EEPROM access	R/W	This is a self-clearing bit. 1 = Execute read or write EEPROM based on the settings of register 21E, bit 12.	0
12	EEPROM read or write	R/W	1 = Read from EEPROM. 0 = Write to EEPROM.	1
11	EEPROM ready	RO	1 = EEPROM is ready for read or write.	1
10:0	EEPROM address	R/W	Sets the address of the EEPROM to which the read or write is to be directed.	00000000000

4.3.8 EEPROM Data Read/Write

Register 22E in the extended register space enables access to the contents of the external EEPROM in your design. The following table lists the writes needed to obtain the data from the external device.

Table 43. EEPROM Read or Write, Address 22E (0x16)

Bit	Name	Access	Description	Default
15:8	EEPROM read data	RO	Eight-bit data read from EEPROM; requires setting register 21E, bit 13.	0x00
7:0	EEPROM write data	R/W	Eight-bit data to be written to EEPROM.	0x00

4.3.9 Extended PHY Control 4

The register at address 23E consists of the fourth set bits that control various aspects of inline powering and the CRC error counter in the VSC8601 device.

Table 44. Extended PHY Control 4, Address 23E (0x17)

Bit	Name	Access	Description	Default
15:11	PHY address	RO	PHY address; latched on reset.	CMODE
10	Inline powered device detection	R/W	This is a sticky bit. 1 = Enabled.	0
9:8	Inline powered device detection status	RO	00 = Searching for devices. 01 = Device found; requires inline power. 10 = Device found; does not require inline power. 11 = Reserved.	00

Table 44. Extended PHY Control 4, Address 23E (0x17) *(continued)*

Bit	Name	Access	Description	Default
7:0	CRC error counter	RO	This is a self-clearing bit. CRC error counter for the Ethernet packet generator. The value saturates at 0xFF and subsequently clears when read and restarts count.	0x00

Note Bits 9:8 are only valid if bit 10 is set.

4.3.10 Reserved Extended Registers

The bits in the extended register page space at addresses 24E, 25E, and 26E (0x18, 0x19, and 0x1A, respectively) are reserved.

4.3.11 Extended PHY Control 5

The following table lists the settings available.

Table 45. Extended PHY Control 5, Address 27E (0x1B)

Bit	Name	Access	Description	Default
15	HP Auto-MDIX in forced 10/100	R/W	This is a sticky bit. 1 = Disabled. For more information about HP Auto-MDIX, see "Automatic Crossover and Polarity Detection," page 20.	1
14	Reserved	RO		
13:12	CRS behavior control	R/W	This is a sticky bit. Controls the CRS Behavior. The effect of each setting depends on whether it is half-duplex or full-duplex operation. For half-duplex operation: 00: CRS = RX_DV + TX_EN 01: CRS = RX_DV + TX_EN 10: CRS = RX_DV 11: CRS = RX_DV. For full-duplex operation: 00: CRS = RX_DV 01: CRS = 0 10: CRS = RX_DV 11: CRS = 0.	00
11	EEPROM present	RO	1 = Configuration EEPROM detected on the EECLK and EEDAT pins.	0
10	Far End loopback mode	R/W	1 = Enabled.	0
9	PICMG 2.16 reduced power mode	R/W	This is a sticky bit. 1 = Enabled.	0

Table 45. Extended PHY Control 5, Address 27E (0x1B) *(continued)*

Bit	Name	Access	Description	Default
8:6	100BASE-TX transmitter amplitude control	R/W	This is a sticky bit. 011 = Reserved. 010 = +4 amplitude setting (largest). 001 = +3 amplitude setting. 000 = +2 amplitude setting. 111 = +1 amplitude setting. 110 = Default amplitude. 101 = –1 amplitude setting. 100 = –2 amplitude setting (smallest).	110
5:3	1000BASE-T transmitter amplitude control	R/W	This is a sticky bit. 011 = Reserved. 010 = +2 amplitude setting (largest). 001 = +1 amplitude setting. 000 = Default amplitude. 111 = –1 amplitude setting. 110 = –2 amplitude setting. 101 = –3 amplitude setting. 100 = –4 amplitude setting (smallest)	000
2:0	1000BASE-T edge rate control	R/W	This is a sticky bit. 011 = +4 edge rate (slowest). 010 = +3 edge rate. 001 = +2 edge rate. 000 = +1 edge rate. 111 = default edge rate. 110 = –1 edge rate. 101 = –2 edge rate. 100 = –3 edge rate (fastest)	111

4.3.12 RGMII Skew Control

The following table lists the settings available.

Table 46. RGMII Skew Control, Address 28E (0x1C)

Bit	Name	Access	Description	Default
15:14	RGMII TX skew compensation enable	R/W	This is a sticky bit. 00 = 0 ns. 01 = 1.4 ns. 10 = 1.7 ns. 11 = 2.0 ns.	CMODE
13:12	RGMII RX skew compensation enable	R/W	This is a sticky bit. 00 = 0 ns. 01 = 1.4 ns. 10 = 1.7 ns. 11 = 2.0 ns.	CMODE
11:10	Jumbo packet mode	R/W	This is a sticky bit. 00 = Normal IEEE 1.5 kB packet length. 01 = Normal IEEE 9 kB packet length. 10 = Normal IEEE 12 kB packet length. 11 = Normal IEEE 16 kB packet length.	00
9	10BASE-T no preamble mode	R/W	This is a sticky bit. 1 = Enabled, no preamble required. 0 = Disabled, preamble required.	0

Table 46. RGMII Skew Control, Address 28E (0x1C) *(continued)*

Bit	Name	Access	Description	Default
8:0	Reserved	RO		

4.3.13 Ethernet Packet Generator (EPG) Control 1

The EPG control register provides access to and control of various aspects of the EPG testing feature. There are two, separate EPG control registers. The following table lists the setting available in the first register.

Table 47. EPG Control Register 1, Address 29E (0x1D)

Bit	Name	Access	Description	Default
15	EPG enable	R/W	1 = Enable EPG	0
14	EPG run or stop	R/W	1 = Run EPG	0
13	Transmission duration	R/W	1 = Continuous (sends in 10,000-packet increments) 0 = Send 30,000,000 packets and stop	0
12:11	Packet length	R/W	00 = 125 bytes 01 = 64 bytes 10 = 1518 bytes 11 = 10,000 bytes (Jumbo packet)	0
10	Inter-packet gap	R/W	1 = 8,192 ns 0 = 96 ns	0
9:6	Destination address	R/W	Lowest nibble of the six-byte destination address	0001
5:2	Source address	R/W	Lowest nibble of the six-byte destination address	0000
1	Payload type	R/W	1 = Randomly generated payload pattern 0 = Fixed based on payload pattern	0
0	Bad frame check sequence (FCS) generation	R/W	1 = Generate packets with bad FCS 0 = Generate packets with good FCS	0

The following information applies to the EPG control number 1:

- Do not run the EPG when the VSC8601 device is connected to a live network.
- Bit 29E.13 (Continuous EPG mode control): When enabled, this mode causes the device to send continuous packets. When disabled, the device continues to send packets only until it reaches the next 10,000-packet increment mark. It then ceases to send packets.
- The six-byte destination address in bits 9:6 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- The six-byte source address in bits 5:2 is assigned one of 16 addresses in the range of 0xFF FF FF FF FF F0 through 0xFF FF FF FF FF FF.
- If any of bits 13:0 are changed while the EPG is running (bit 14 is set to 1), bit 14 must be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.3.14 Ethernet Packet Generator Control 2

The register at address 30E consists of the second of bits that provide access to and control over various aspects of the EPG testing feature. For information about the first set of EPG control bits, see Table 47, page 63. The following table lists the settings available.

Table 48. EPG Control Register 2, Address 30E (0x1E)

Bit	Name	Access	Description	Default
15:0	EPG packet payload	R/W	Data pattern repeated in the payload of packets generated by the EPG	0x00

Note If any of bits 15:0 in this register are changed while the EPG is running (bit 14 of register 29E is set to 1), that bit (29E.14) must first be cleared and then set back to 1 for the change to take effect and to restart the EPG.

4.4 CMODE

The information in this section consists of a detailed description of the methods to configure the VSC8601 device using its CMODE pins. It includes descriptions of the registers that work together with the CMODE pins to control the device function.

There are four configuration mode (CMODE) pins on the VSC8601 device. For more information about the physical location of the CMODE pins, see "Pin Descriptions," page 84. Each CMODE pin maps to a configuration bit, which means there are 16 possible settings for the device.

4.4.1 CMODE Pins and Related Functions

The following table lists the pin numbers and device functionality that is controlled by each configuration bit.

Table 49. CMODE Configuration Pins and Device Functions

CMODE Pin	Bit 3 (MSB) Control	Bit 2 Controls	Bit 1 Controls	Bit 0 (LSB) Controls
3	PHY address [3]	PHY address [4]	MAC calibration setting[1]	MAC calibration setting[0]
2	PHY address [2]	ActiPHY	RGMII clock skew[1]	RGMII clock skew[0]
1	PHY address [1]	Link speed downshift	Speed/Duplex Modes [1]	Speed/Duplex modes [0]
0	PHY address [0]	CLKOUT enable	Advertise asymmetric pause	Advertise symmetric pause

4.4.2 Functions and Related CMODE Pins

The following table lists the pin and bit settings according to the device function and CMODE pin used to configure it.

Table 50. Device Functions and Associated CMODE Pins

Function	CMODE Pin	Bit	Associated Register, Bit	Result
PHY Address [4:0]	3 to 0	3 and 2		Sets the PHY address.
Link speed downshift	1	2	Register 20E, bit 4	0 = Link only according to the auto-negotiation resolution. 1 = Enable link speed downshift feature.
Speed and duplex	1	1 and 0	Register 4, bits 8:5 and Register 9, bits 9:8	00 = 10/100/1000BASE-T FDX/HDX. 01 = 10/100/1000BASE-T FDX; 10/100BASE-T HDX. 10 = 1000BASE-T FDX only. 11 = 10/100BASE-T FDX/HDX.
RGMII clock skew	2	1 and 0	Register 23, bit 8	00 = No skew on RX_CLK and TX_CLK. 01 = 1.4 ns skew on RX_CLK and TX_CLK. 10 = 1.7 ns skew on RX_CLK and TX_CLK. 11 = 2.0 ns skew on RX_CLK and TX_CLK.
Advertise asymmetric pause	0	1	Register 4, bit 11	0 = Not advertised. 1 = Advertised.
Advertise symmetric pause	0	0	Register 4, bit 10	0 = Not advertised. 1 = Advertised.
CLKOUT enable	0	2	Register 18, bit 0	0 = Disabled. 1 = Enabled.
ActiPHY	2	2	Register 23, bit 5	0 = Disabled. 1 = Enabled.
MAC resistor calibration setting	3	1 and 0	Register 19E, bits 15:14	00 = 50 Ω. 01 = 60 Ω. 10 = 30 Ω. 11 = 45 Ω.

4.4.3 CMODE Resistor Values

To affect the VSC8601 device configuration, find the parameter in Table 49, page 64 or in Table 50, page 65, and connect the associated pin to the resistor specified in the following table. This sets the bits as shown.

Table 51. CMODE Resistor Values and Resultant Bit Settings

With CMODE Pin Tied To	With 1% Resistor Value	Set Bit 3 (MSB) to:	Set Bit 2 to:	Set Bit 1 to:	Set Bit 0 (LSB) to:
VSS	0	0	0	0	0
VSS	2.26 kΩ	0	0	0	1
VSS	4.02 kΩ	0	0	1	0
VSS	5.90 kΩ	0	0	1	1

Table 51. CMODE Resistor Values and Resultant Bit Settings *(continued)*

With CMODE Pin Tied To	With 1% Resistor Value	Set Bit 3 (MSB) to:	Set Bit 2 to:	Set Bit 1 to:	Set Bit 0 (LSB) to:
VSS	8.25 kΩ	0	1	0	0
VSS	12.1 kΩ	0	1	0	1
VSS	16.9 kΩ	0	1	1	0
VSS	22.6 kΩ	0	1	1	1
VDD33	0	1	0	0	0
VDD33	2.26 kΩ	1	0	0	1
VDD33	4.02 kΩ	1	0	1	0
VDD33	5.90 kΩ	1	0	1	1
VDD33	8.25 kΩ	1	1	0	0
VDD33	12.1 kΩ	1	1	0	1
VDD33	16.9 kΩ	1	1	1	0
VDD33	22.6 kΩ	1	1	1	1

Using resistors with the CMODE pins can be optional in designs that access the device's MDC/MDIO pins. In designs that do this, all configurations otherwise affected on the device by using the CMODE pins can be changed using the regular device register settings, and all the CMODE pins can be pulled to VSS (ground). However, the PHYADDR [4:0] still requires CMODE configuration.

4.5 EEPROM

The VSC8601 device EEPROM interface makes it possible to set up the device to self-configure its internal registers based on the information programmed into and stored in an external device. To accomplish this, the EEPROM is read on power-up or de-assertion of the NRESET bit. For field configuration, the EEPROM can also be accessed using VSC8601 device registers 21E and 22E.

The EEPROM used to interface to the VSC8601 device must have a two-wire interface. A device such as the Atmel part AT24CXXX is suggested.

As defined by the interface, data is clocked from the VSC8601 device on the falling edge of EECLK. The device determines that an external EEPROM is present if EEDAT is connected to a 4.7 kΩ external pull-up resistor. The EEDAT pin can be left floating or grounded to indicate that no EEPROM is present.

4.5.1 EEPROM Contents Description

When an EEPROM is present, the VSC8601 device looks for the command header, 0xBDBD at address 0 and 1 of the EEPROM. The address is incremented by 256 until the header is found. If the header is not found or no EEPROM is connected, the VSC8601 device bypasses the EEPROM read step.

When an EEPROM is present, the VSC8601 device waits for an acknowledgement for approximately three seconds (in accordance with the ATMEL EEPROM protocol). If there

is no acknowledgement for three seconds, the VSC8601 device aborts its attempt to connect to the EEPROM and reverts to its otherwise normal operating mode.

After the header value is found, the two-byte address value shown in the following table indicates the EEPROM word address where the base address location for the device is located. At the base address location, the next set of bytes indicates where the configuration data contents to be programmed into the VSC8601 device are located. At the programming location, the first two bytes represent the total number of bytes (11 bits long, with MSB first) where the Total_Number_Bytes[10:0] is equal to the number of SMI writes multiplied by 3 (one byte for SMI port and register address and two bytes for data). Data is read from the EEPROM sequentially until all SMI write commands are completed.

Table 52. EEPROM Configuration Contents

10-bit Address	Content (Bits 7:0)
0	0xBD
1	0xBD
2	PHY_ADDR[4:0], Base_Address_Location[10:8]
3	Base_Address_Location[7:0] (K)
	Address length not specified
	Address length not specified
K	00000, Config Location[10:8]
K+1	Config_Location[7:0] (X)
	Address length not specified
	Address length not specified
X	00000, Total_Number_Bytes[10:8]
X+1	Total_Number_Bytes [7:0] (M)
X+2	Register address a
X+3	Data[15:8] to be written to register address a
X+4	Data[7:0] to be written to register address a
X+5	Register address b
X+6	Data[15:8] to be written to register address b
X+7	Data[7:0] to be written to register address b
	Address length not specified
X+(M–2)	Register address x
X+(M–1)	Data[15:8] to be written to register address x
X+M	Data[7:0] to be written to register address x
	Address length not specified
	Address length not specified
Max Address	

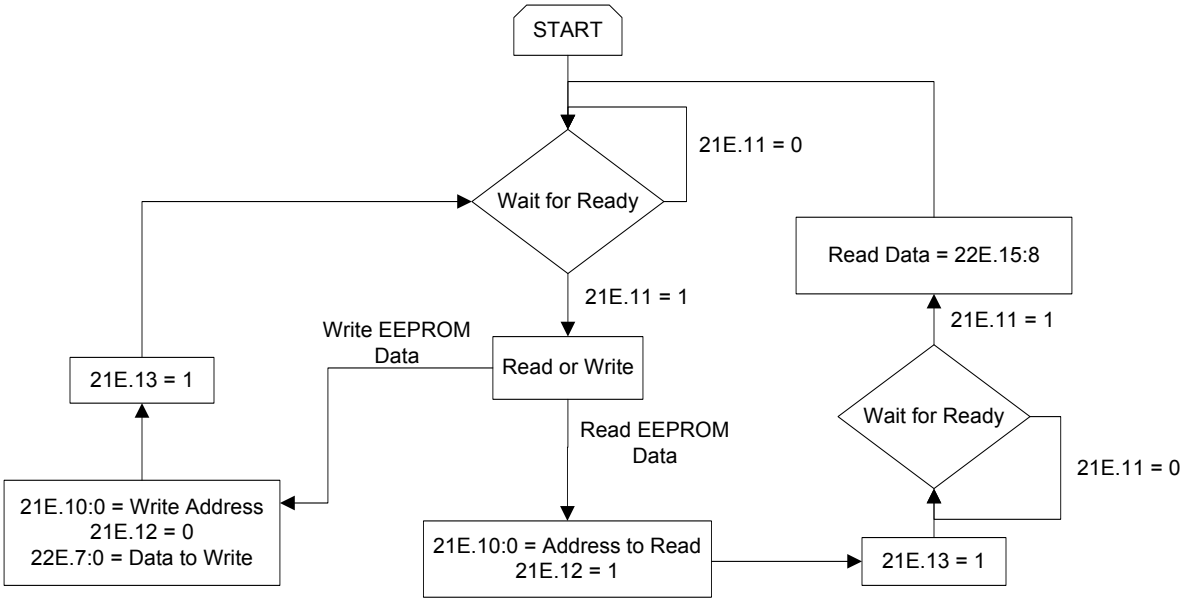
4.5.2 Read/Write Access to the EEPROM

The VSC8601 device also has the ability to read from and write to an EEPROM such as an ATMEL AT24CXXX that is directly connected to its EECLK and EEDAT pins. If it is

required to be able to write to the EEPROM, refer to the EEPROM's specific datasheet to ensure that write protection on the EEPROM is not set.

The following illustration shows the interaction of the VSC8601 device and the EEPROM.

Figure 17. EEPROM Read and Write Register Flow



To read a value from a specific address of the EEPROM:

1. Read the VSC8601 device register bit 21E.11 and ensure that it is set.
2. Write the EEPROM address to be read to register bits 21E.10:0.
3. Set both register bits 21E.12 and 21E.13 both to 1.
4. When register bit 21E.11 changes to 1, read the 8-bit data value found at register bits 22E.15:8. This is the contents of the address just read by the PHY.

To write a value to a specific address of the EEPROM:

1. Read the VSC8601 device register bit 21E.11 and ensure that it is set.
2. Write the address to be written to register bits 21E.10:0.
3. Set register bit 21E.12 to 0.
4. Set register bits 22E.7:0 with the 8-bit value to be written to the EEPROM.
5. Set register bit 21E.13 to 1.
6. To avoid collisions during read and write transactions, always wait until register bit 21E.11 changes to 1 before performing another EEPROM read or write operation.

5 Electrical Specifications

This section provides the DC characteristics, AC characteristics, recommended operating conditions, and stress ratings for the VSC8601 device. It includes information on the various timing functions of the device.

5.1 DC Characteristics

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only in the environment characterized by the specifications listed as recommended operating conditions for the VSC8601 device. For more information about the recommended operating conditions, see "Operating Conditions," page 82.

5.1.1 VDDIO at 3.3 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when all of these apply:

- V_{DDIO} is 3.3 V
- V_{DD33} is 3.3 V
- V_{DD12} is 1.2 V
- V_{DD12A} is 1.2 V
- V_{DDREG} is 3.3 V

Table 53. DC Characteristics for VDD33, VDDIOMAC, or VDDIOMICRO at 3.3 V

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.4	3.6	V	I_{OH} = –4 mA
Output low voltage	V_{OL}	0	0.5	V	I_{OL} = 4 mA
Input high voltage	V_{IH}	2.0	5.0	V	For JTAG pins
Input high voltage	V_{IH}	2.1	3.6	V	For all other input pins
Input low voltage	V_{IL}	–0.3	0.9	V	
Input leakage current	I_{ILEAK}	–43	43	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–43	43	µA	Internal resistor included
Output low current drive strength	I_{OL}		11	mA	
Output high current drive strength	I_{OH}	–20		mA	

5.1.2 VDDIO at 2.5 V

In addition to any parameter-specific conditions, the specifications listed in the following table may be considered valid only when all of these apply:

- V_{DDIO} is 2.5 V
- V_{DD33} is 3.3 V
- V_{DD12} is 1.2 V
- V_{DD12A} is 1.2 V
- V_{DDREG} is 3.3 V

Table 54. DC Characteristics for VDDIOMAC or VDDIOMICRO at 2.5 V

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Output high voltage	V_{OH}	2.0	2.8	V	I_{OH} = –1.0 mA
Output low voltage	V_{OL}	–0.3	0.4	V	I_{OL} = 1.0 mA
Input high voltage	V_{IH}	2.0	3.0	V	For all other pins
Input low voltage	V_{IL}	–0.3	0.7	V	
Input leakage current	I_{ILEAK}	–35	35	µA	Internal resistor included
Output leakage current	I_{OLEAK}	–35	35	µA	Internal resistor included
Output low current drive strength	I_{OL}		9	mA	
Output high current drive strength	I_{OH}	–11		mA	

5.2 Current Consumption

The current consumption values listed in this section are based on nominal values and the PHY operating with full-duplex enabled and a 64-bit random data pattern at 100% utilization. Values are grouped by the type of link and whether the on-chip switching regulator is enabled.

5.2.1 Consumption with 1000BASE-T Link

The following table shows the current consumption values with a 1000BASE-T link and the on-chip switching regulator enabled.

Table 55. Current Consumption: 1000BASE-T, Regulator Enabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	115	mA
Current with V_{DDREG}	I_{VDDREG}	75	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	32	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	23	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA

Table 55. Current Consumption: 1000BASE-T, Regulator Enabled *(continued)*

Parameter	Symbol	Typical	Unit
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		734	mW
Total power at 2.5 V		686	mW

The following table shows the current consumption values with a 1000BASE-T link and the on-chip switching regulator disabled.

Table 56. Current Consumption: 1000BASE-T, Regulator Disabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	115	mA
Current with V_{DDREG}	I_{VDDREG}	< 1	mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	136	mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	34	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	32	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	23	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		689	mW
Total power at 2.5 V		641	mW

5.2.2 Consumption with 100BASE-TX Link

The following table shows the current consumption values with a 100BASE-TX link and the on-chip switching regulator enabled.

Table 57. Current Consumption: 100BASE-TX, Regulator Enabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	94	mA
Current with V_{DDREG}	I_{VDDREG}	35	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	5	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	3	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		442	mW
Total power at 2.5 V		433	mW

The following table shows the current consumption values with a 100BASE-TX link and the on-chip switching regulator disabled.

Table 58. Current Consumption: 100BASE-TX, Regulator Disabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	94	mA

Table 58. Current Consumption: 100BASE-TX, Regulator Disabled *(continued)*

Parameter	Symbol	Typical	Unit
Current with V_{DDREG}	I_{VDDREG}	< 1	mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	55	mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	24	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	5	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	3	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		422	mW
Total power at 2.5 V		413	mW

5.2.3 Consumption with 10BASE-T Link

The following table shows the current consumption values with a 10BASE-T link and the on-chip switching regulator enabled.

Table 59. Current Consumption: 10BASE-T, Regulator Enabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	155	mA
Current with V_{DDREG}	I_{VDDREG}	19	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	< 1	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		573	mW
Total power at 2.5 V		573	mW

The following table shows the current consumption values with a 10BASE-T link and the on-chip switching regulator disabled.

Table 60. Current Consumption: 10BASE-T, Regulator Disabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	155	mA
Current with V_{DDREG}	I_{VDDREG}	< 1	mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	24	mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	18	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	< 1	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		562	mW
Total power at 2.5 V		562	mW

5.2.4 Consumption with No Link and ActiPHY Enabled

The following table shows the current consumption values with no link, ActiPHY enabled, and the on-chip switching regulator enabled.

Table 61. Current Consumption: No Link, ActiPHY Enabled, Regulator Enabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	21	mA
Current with V_{DDREG}	I_{VDDREG}	21	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	12	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	8	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		178	mW
Total power at 2.5 V		158	mW

The following table shows the current consumption values with no link, ActiPHY enabled, and the on-chip switching regulator disabled.

Table 62. Current Consumption: No Link, ActiPHY Enabled, Regulator Disabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	21	mA
Current with V_{DDREG}	I_{VDDREG}	< 1	mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	27	mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	20	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	12	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	8	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		165	mW
Total power at 2.5 V		146	mW

5.2.5 Consumption with No Link and ActiPHY Disabled

The following table shows the current consumption values with no link, ActiPHY disabled, and the on-chip switching regulator enabled.

Table 63. Current Consumption: No Link, ActiPHY Disabled, Regulator Enabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	107	mA
Current with V_{DDREG}	I_{VDDREG}	22	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	12	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	8	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA

Table 63. Current Consumption: No Link, ActiPHY Disabled, Regulator Enabled

Parameter	Symbol	Typical	Unit
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		466	mW
Total power at 2.5 V		446	mW

The following table shows the current consumption values with no link, ActiPHY disabled, and the on-chip switching regulator disabled.

Table 64. Current Consumption: No Link, ActiPHY Disabled, Regulator Disabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	107	mA
Current with V_{DDREG}	I_{VDDREG}	< 1	mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	27	mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	23	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	12	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	8	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	< 1	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	< 1	mA
Total power at 3.3 V		453	mW
Total power at 2.5 V		433	mW

5.2.6 Consumption in Power-Down Mode

The following table shows the current consumption values in power-down mode (register address 0.11 = 1) with the regulator enabled.

Table 65. Current Consumption: Power-Down, Regulator Enabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	15	mA
Current with V_{DDREG}	I_{VDDREG}	15	mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	0	mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	0	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	0	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	0	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	0	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	0	mA
Total power at 3.3 V		99	mW

The following table shows the current consumption values in power-down mode (register address 0.11 = 1) with the regulator disabled.

Table 66. Current Consumption: Power-Down, Regulator Disabled

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	15	mA
Current with V_{DDREG}	I_{VDDREG}	0	mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	12	mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	20	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	0	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	0	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	0	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	0	mA
Total power at 3.3 V		87.9	mW

5.2.7 Consumption in Reset State

The following table shows the current consumption values in the reset state (NRESET pin pulled low).

Table 67. Current Consumption: Reset State

Parameter	Symbol	Typical	Unit
Current with V_{DD33} at 3.3 V	I_{VDD33}	7	mA
Current with V_{DDREG}	I_{VDDREG}	0	mA
Current with V_{DD12} at 1.2 V	I_{VDD12}	0	mA
Current with V_{DD12A} at 1.2 V	I_{VDD12A}	0	mA
Current with $V_{DDIOMAC}$ at 3.3 V	$I_{VDDIOMAC}$	0	mA
Current with $V_{DDIOMAC}$ at 2.5 V	$I_{VDDIOMAC}$	0	mA
Current with $V_{DDIOMICRO}$ at 3.3 V	$I_{VDDIOMICRO}$	0	mA
Current with $V_{DDIOMICRO}$ at 2.5 V	$I_{VDDIOMICRO}$	0	mA
Total power at 3.3 V		23.1	mW

5.3 AC Characteristics

The AC specifications are grouped according to specific device pins and associated timing characteristics.

5.3.1 Reference Clock Input

The following table lists the specifications for the reference clock input frequency including various frequencies, duty cycle, and accuracy.

Table 68. AC Characteristics for REFCLK Input

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Frequency with 25 MHz input	f_{CLK25}		25		MHz
Frequency with 125 MHz input	f_{CLK125}		125		MHz
Frequency accuracy	f_{TOL}			50	ppm
Duty cycle	$\%_{DUTY}$	40		60	%
Rise time with 25 MHz input (20% to 80%)	t_{R25}			4	ns
Rise time with 125 MHz input (20% to 80%)	t_{R125}			1	ns

When using the 25 MHz crystal clock input option, the additional specifications in the following table are required.

Table 69. AC Characteristics for REFCLK Input with 25 MHz Clock Input

Parameter	Minimum	Typical	Maximum	Unit
Crystal parallel load capacitance	18		20	pF
Crystal equivalent series resistance		10	30	Ω

5.3.2 Clock Output

The specifications in the following table show the AC characteristics for the clock output of the VSC8601 device.

Table 70. AC Characteristics for the CLKOUT Pin

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
CLKOUT frequency	f_{CLK}		125.00		MHz	125 MHz output clock
CLKOUT cycle time	t_{CYC}		8.0		ns	125 MHz output clock
Frequency stability	$f_{STABILITY}$			50	ppm	
Duty cycle	$\%_{DUTY}$	44	50	56	%	
Clock rise and fall times (20% to 80%)	t_R and t_F			1	ns	
Total jitter	J_{CLK}		217	600	ps	Measured peak-to-peak, time interval error

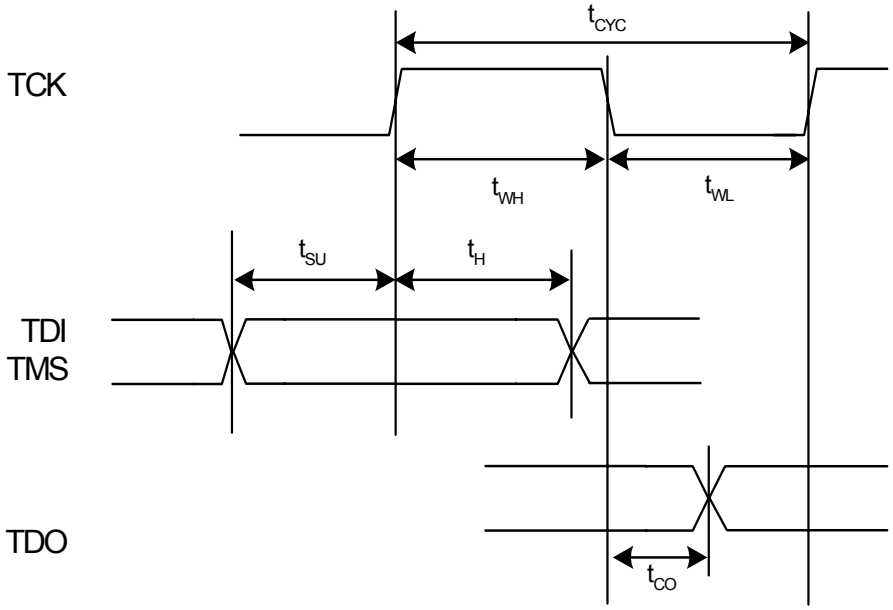
5.3.3 JTAG Interface

The following table lists the characteristics for the JTAG testing feature. For information about the JTAG interface timing, see Figure 18, page 77.

Table 71. AC Characteristics for the JTAG Interface

Parameter	Symbol	Minimum	Maximum	Unit
TCK frequency	f_{CLK}		10	MHz
TCK cycle time	t_{CYC}	100		ns
TCK time high	t_{WH}	45		ns
TCK time low	t_{WL}	45		ns
Setup time to TCK rising	t_{SU}	10		ns
Hold time from TCK rising	t_{H}	10		ns
TCK to TDO valid	t_{CO}		15	ns

Figure 18. JTAG Interface Timing



5.3.4 SMI Interface

Use the information in the following table when incorporating the VSC8601 device SMI interface into your own design. For information about the SMI interface timing, see Figure 19, page 78.

Table 72. AC Characteristics for the SMI Interface

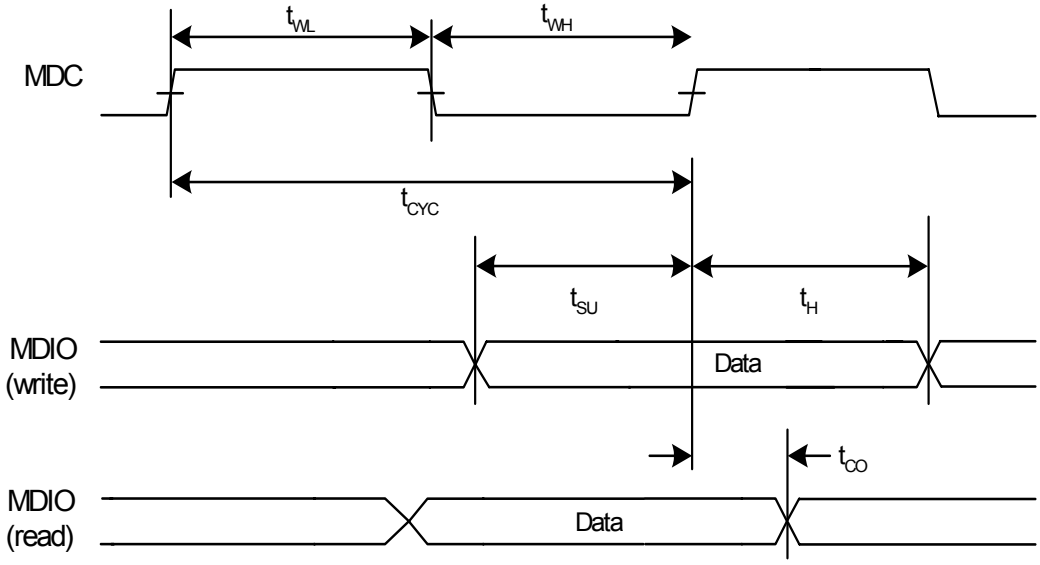
Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC frequency(1)	f_{CLK}		2.5	12.5	MHz	
MDC cycle time	t_{CYC}	80	400		ns	

Table 72. AC Characteristics for the SMI Interface *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
MDC time high	t_{WH}	20	50		ns	
MDC time low	t_{WL}	20	50		ns	
Setup to MDC rising	t_{SU}	10			ns	
Hold from MDC rising	t_H	10			ns	
MDC rise time	t_R			100 t_{CYC} × 10%(1)	ns	For MDC = 0 – 1 MHz For MDC = 1 MHz – f_{CLK}(MAX)
MDC fall time	t_F			100 t_{CYC} × 10%(1)		
MDC to MDIO valid	t_{CO}		10	300	ns	Time dependant on value of external pull-up resistor on MDIO pin

1. For f_{CLK} above 1 MHz, the maximum rise time and fall time is in relation to the frequency of the MDC clock period. For example, if f_{CLK} is 2 MHz, the maximum clock rise time and fall time is 50 ns.

Figure 19. SMI Interface Timing



5.3.5 Device Reset

The following specifications apply to the device reset functionality. For more information about the reset timing, see Figure 20, page 79.

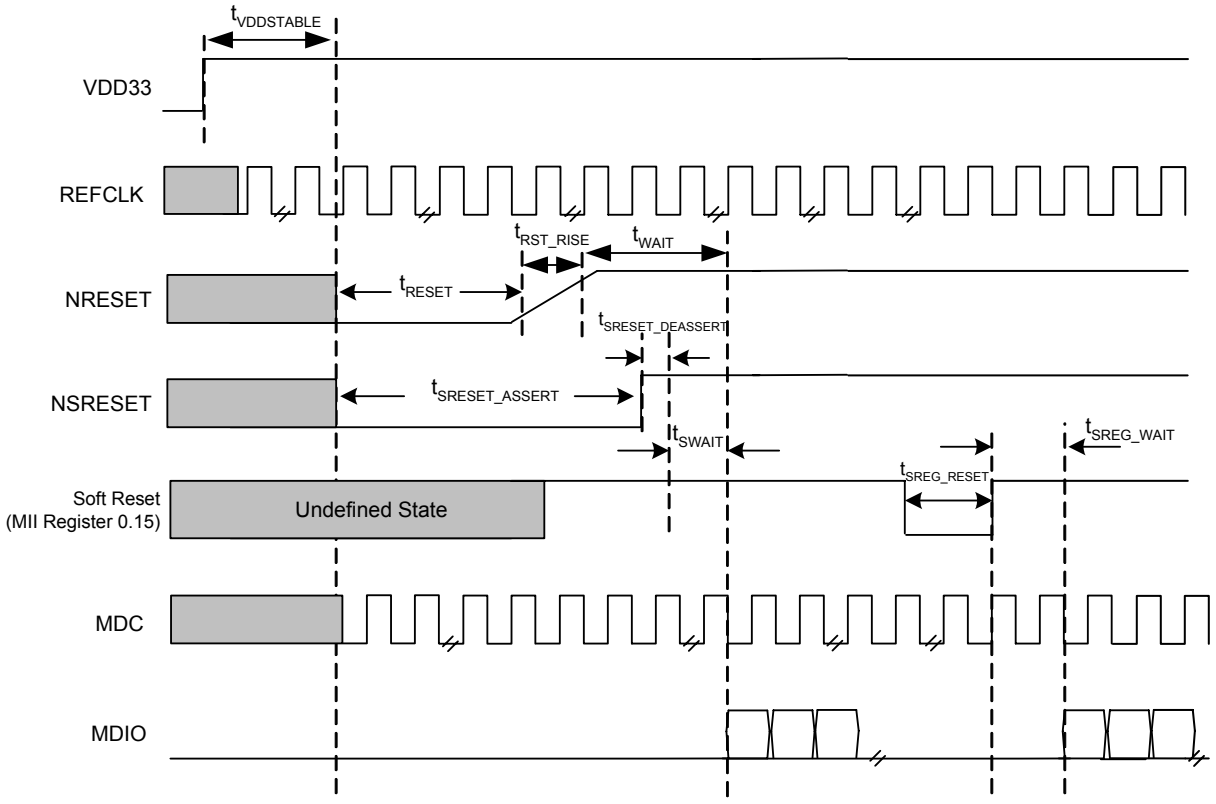
Table 73. AC Characteristics for Device Reset

Parameter	Symbol	Minimum	Maximum	Unit	Condition
NRESET assertion time	t_{RESET}	100		ns	
Wait time between NRESET de-assert and access of the SMI interface	t_{WAIT}	20 220		ms ms	Register 21E.14 = 0 Register 21E.14 = 1

Table 73. AC Characteristics for Device Reset *(continued)*

Parameter	Symbol	Minimum	Maximum	Unit	Condition
Soft reset (pin) assertion	t_{SRESET_ASSERT}	4		ms	
Soft reset (pin) de-assertion	$t_{SRESET\_DEASSERT}$	4		ms	
Reset rise time	t_{RST_RISE}	0 25		ms ms	If REG_EN pin = 0 If REG_EN pin = 1 Measured from a 10% level to a 90% level
Supply stable time	$t_{VDDSTABLE}$	10		ms	
Wait time between soft reset pin de-assert and access of the SMI interface	t_{SWAIT}	4 300 200 200		µs µs ms ms	Registers 28.1 = 1, 21E.14 = 0 Registers 28.1 = 0, 21E.14 = 0 Registers 28.1 = 0, 21E.14 = 1 Registers 28.1 = 1, 21E.14 = 1
Soft reset MII register 0.15 assertion	t_{SREG_RESET}	100		ns	
Wait time between Soft Reset (MII Register 0.15) de-assert and access to the SMI interface	t_{SREG_WAIT}	4 300 200 200		µs µs ms ms	Registers 18.1 = 1, 21E.14 = 0 Registers 18.1 = 0, 21E.14 = 0 Registers 18.1 = 0, 21E.14 = 1 Registers 18.1 = 1, 21E.14 = 1

Figure 20. Reset Timing



Note The NRESET and NSRESET are mutually exclusive.

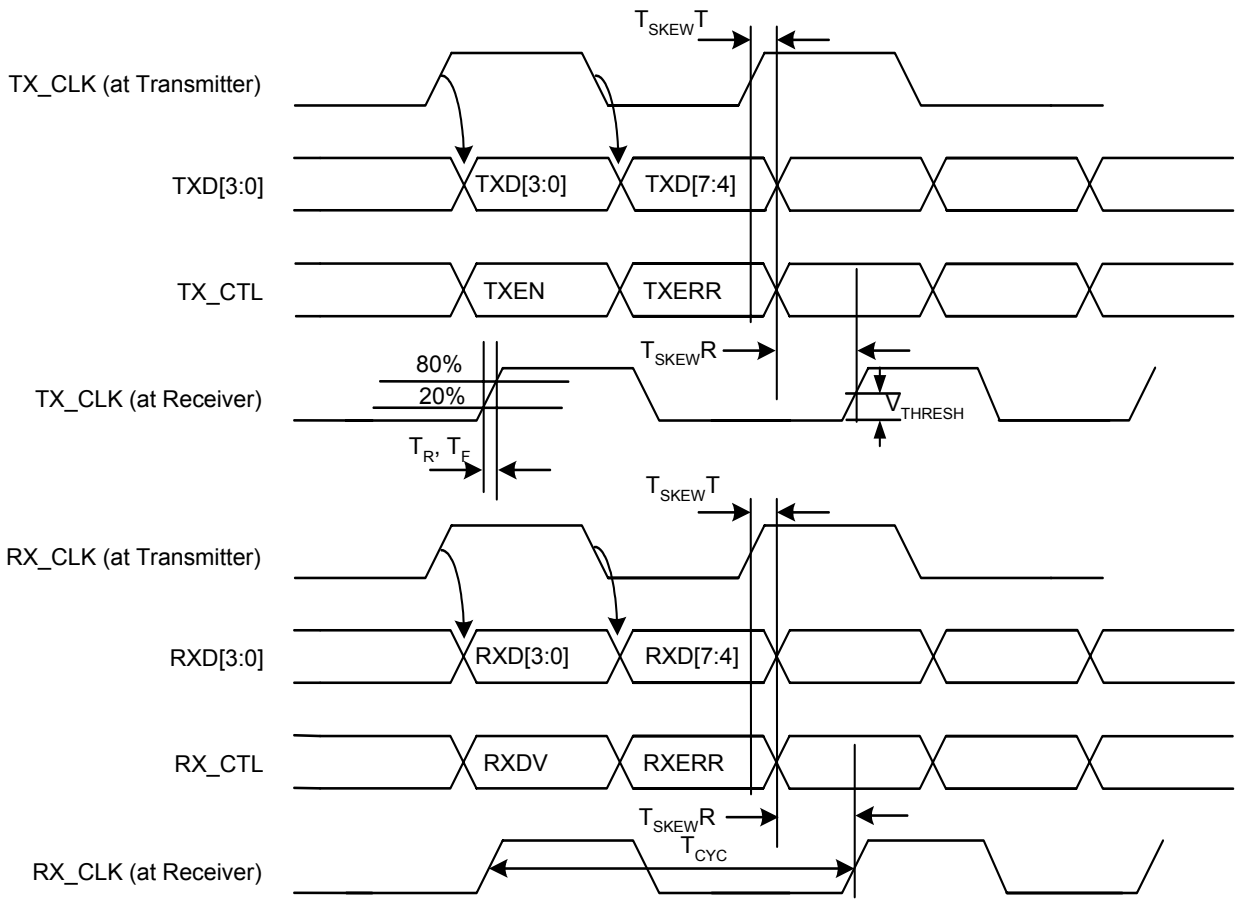
5.3.6 RGMII Uncompensated

The following table lists the characteristics when using the device in RGMII uncompensated mode. For more information about the RGMII uncompensated timing, see Figure 21, page 81.

Table 74. AC Characteristics for RGMII Uncompensated

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Clock frequency			125 25 2.5		MHz	1000BASE-T operation 100BASE-TX operation 10BASE-T operation
1000BASE-T duty cycle	$t_{DUTY1000}$	45	50	55	%	At room temperature and nominal supply and register 28E.13:12 set to 10 or 11
1000BASE-T duty cycle	$t_{DUTY1000}$	40	50	60	%	Register 28E.13:12 set to 00 or 01
10/100BASE-T duty cycle	$t_{DUTY10/100}$	40	50	60	%	
Data to clock output skew (at PHY)	$t_{SKEW}T$	–500	0	500	ps	
Data to clock output skew (at receiver)	$t_{SKEW}R$	1.0	1.8	2.6	ns	
TX_CLK switching threshold	V_{THRESH}		1.25 1.65		V V	$V_{DDIOMAC}$ = 2.5 V $V_{DDIOMAC}$ = 3.3 V
TX_CLK rise and fall times	t_R and t_F			750	ps	

Figure 21. RGMII Uncompensated Timing



5.3.7 RGMII Compensated

The following table lists the characteristics when using the device in RGMII compensated mode. For more information about the RGMII compensated timing, see Figure 22, page 82.

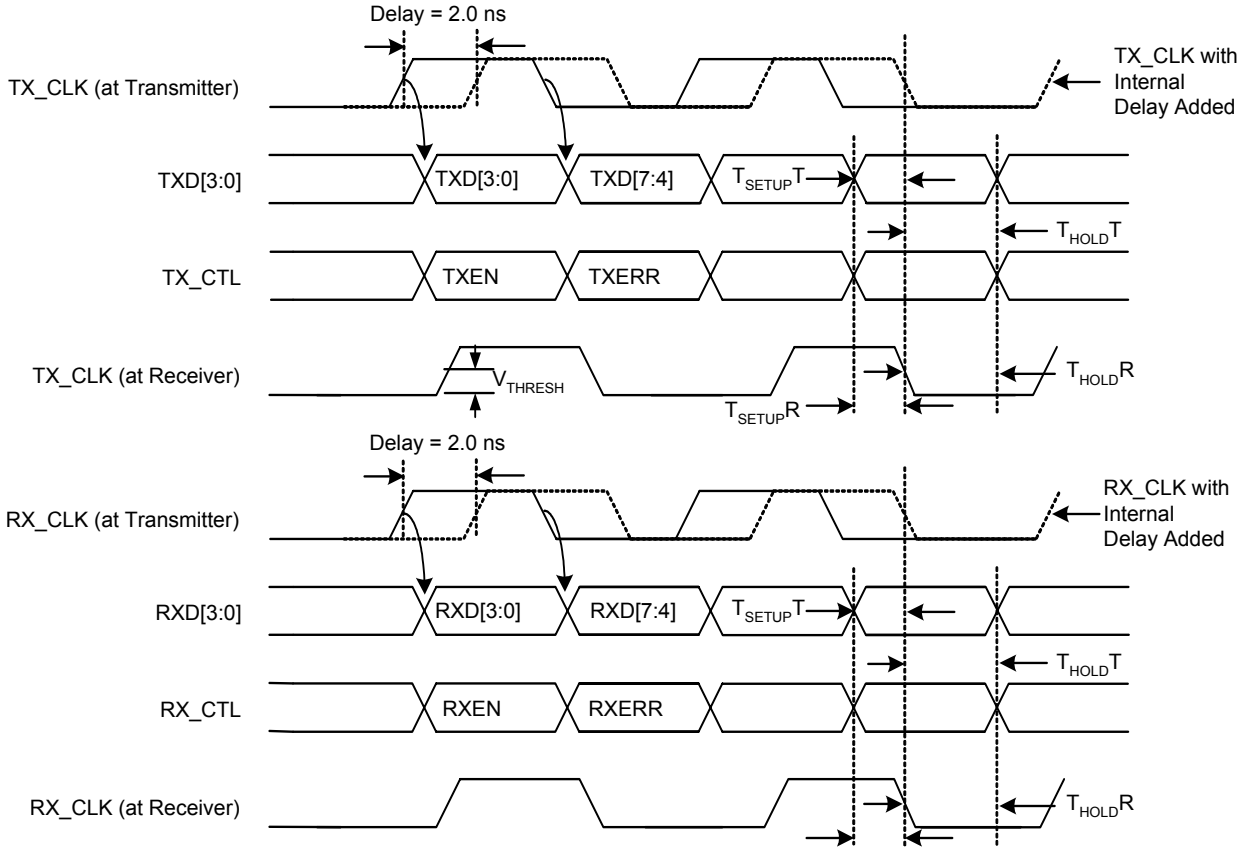
Table 75. AC Characteristics for RGMII Compensated

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Data to clock output setup (at PHY integrated delay)	$t_{SETUP}T$	1.2	2.0	3	ns	
Data to clock output setup (at receiver integrated delay)	$t_{SETUP}R$	1.0	2.0	3	ns	
Data to clock output hold (at transmitter integrated delay)	$t_{HOLD}T$	1.2	2.0	3	ns	

Table 75. AC Characteristics for RGMII Compensated *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit	Condition
Data to clock output hold (at PHY integrated delay)	$t_{HOLD}R$	1.0	2.0	3	ns	
TX_CLK switching threshold	v_{THRESH}		1.25 1.65		V V	$V_{DDIOMAC}$ = 2.5 V $V_{DDIOMAC}$ = 3.3 V

Figure 22. RGMII Compensated Timing



5.4 Operating Conditions

The following table lists the recommended operating conditions for the VSC8601 device.

Table 76. Recommended Operating Conditions

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for $V_{DDIOMICRO}$ at 2.5 V	$V_{DDIOMICRO}$	2.37	2.5	2.63	V

Table 76. Recommended Operating Conditions *(continued)*

Parameter	Symbol	Minimum	Typical	Maximum	Unit
Power supply voltage for $V_{DDIOMICRO}$ at 3.3 V	$V_{DDIOMICRO}$	3.0	3.3	3.6	V
Power supply voltage for $V_{DDIOMAC}$ at 2.5 V	$V_{DDIOMAC}$	2.37	2.5	2.63	V
Power supply voltage for $V_{DDIOMAC}$ at 3.3 V	$V_{DDIOMAC}$	3.0	3.3	3.6	V
Power supply voltage for V_{DD33}	V_{DD33}	3.0	3.3	3.6	V
Power supply voltage for V_{DDREG}	V_{DDREG}	3.0	3.3	3.6	V
Power supply voltage for V_{DD12}	V_{DD12}	1.14	1.2	1.26	V
Power supply voltage for V_{DD12A}	V_{DD12A}	1.14	1.2	1.26	V
Operating temperature(1)	T	0		90	°C

1. Lower limit of specification is ambient temperature, and upper limit is case temperature.

5.5 Stress Ratings

This section contains the stress ratings for the VSC8601 device.

Warning Stresses listed in the following table may be applied to devices one at a time without causing permanent damage. Functionality at or exceeding the values listed is not implied. Exposure to these values for extended periods may affect device reliability.

Table 77. Stress Ratings

Parameter	Symbol	Minimum	Maximum	Unit
DC input voltage on $V_{DDIOMICRO}$ supply pin	$V_{DDIOMICRO}$	–0.5	4.0	V
DC input voltage on $V_{DDIOMAC}$ supply pin	$V_{DDIOMAC}$	–0.5	4.0	V
DC input voltage on V_{DD33} supply pin	V_{DD33}	–0.5	4.0	V
DC input voltage on V_{DDREG} supply pin	V_{DDREG}	–0.5	4.0	V
DC input voltage on V_{DD12} supply pin	V_{DD12}	–0.5	1.5	V
DC input voltage on V_{DD12A} supply pin	V_{DD12A}	–0.5	1.5	V
DC input voltage on JTAG pins, 5 V tolerant	V_{DD}(5 V)	–0.5	5.5	V
DC input voltage on any non-supply pin	V_{DD}(PIN)	–0.5	V_{DD} + 0.5	V
Storage temperature	T_S	–65	150	°C
Electrostatic discharge voltage, charged device model	V_{ESD_CDM}	–500	500	V
Electrostatic discharge voltage, human body model	V_{ESD_HBM}	–1500	1500	V

Warning This device can be damaged by electrostatic discharge (ESD) voltage. Vitesse recommends that all integrated circuits be handled with appropriate precautions. Failure to observe proper handling and installation procedures may adversely affect reliability of the device.

6 Pin Descriptions

The VSC8601 device has 64 pins, which are described in this section.

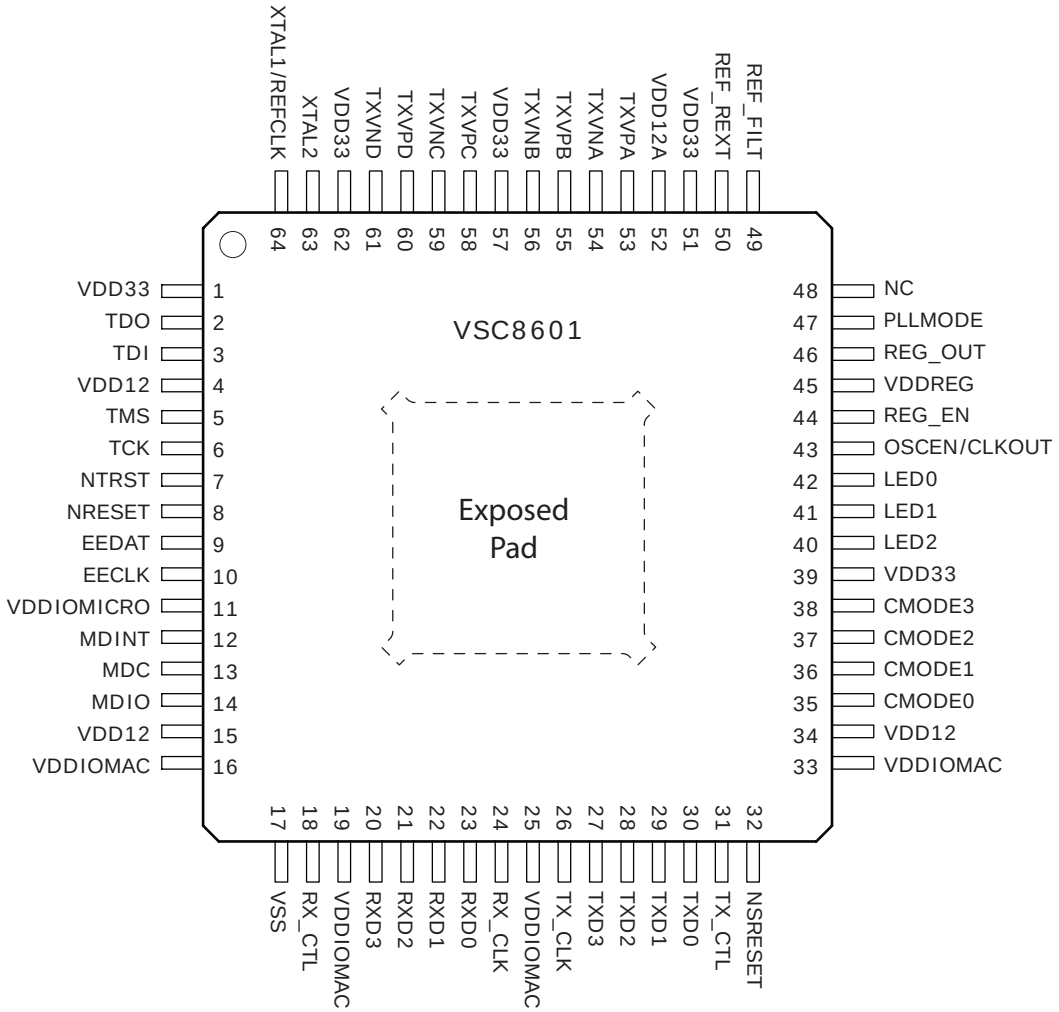
The pin information is also provided as an attached Microsoft Excel file, so that you can copy it electronically. In Adobe Reader, double-click the attachment icon.

6.1 Pin Diagram

The following illustration shows the pin diagram for the VSC8601 device.

Note The exposed pad is internally connected to ground and should be connected to VSS on the board as well.

Figure 23. Pin Diagram



6.2 Pins by Function

This section contains the functional pin descriptions for the VSC8601 device. The following table contains notations for definitions of the various pin types.

Table 78. Pin Type Symbols

Symbol	Pin Type	Description
I	Input	Input with no on-chip pull-up or pull-down resistor.
I/O	Input and Output	Input and output signal with no on-chip pull-up or pull-down resistor.
I_{PU}	Input with pull-up	Input with on-chip 100 kΩ pull-up resistor to VDDIO.
I_{PD}	Input with pull-down	Input with on-chip 100 kΩ pull-down resistor to VSS.
I_{PD}/O	Bidirectional with pull-down	Input and output signal with on-chip 100 kΩ pull-down resistor to VSS.
I_{PU}/O	Bidirectional with pull-up	Input and output signal with on-chip 100 kΩ pull-up resistor to VDDIO or VDD33.
O	Output	Output signal.
O_{ZC}	Impedance controlled output	Integrated (on-chip) source series terminated, output signal.
OD	Open drain	Open drain output.
OS	Open source	Open source output.
A_{DIFF}	Analog differential	Analog differential signal pair for twisted pair interface.
A_{BIAS}	Analog bias	Analog bias pin.
I_A	Analog input	Analog Input for sensing variable voltage levels.
I_{PU5V}	Input with pull-up	Input with on-chip 100 kΩ pull-up resistor to VDD33. These pins are 5 V tolerant.
O_{CRYST}	Crystal output	Crystal clock output pin. If not used, leave unconnected.
NC	No connect	No connect pins must be left floating.

6.2.1 Twisted Pair Interface

The following table lists the device pins associated with the device two-wire, twisted pair interface.

Table 79. Twisted Pair Interface Pins

Pin	Name	Type	Description
53	TXVPA	A_{DIFF}	TX/RX channel A positive signal
54	TXVNA	A_{DIFF}	TX/RX channel A negative signal
55	TXVPB	A_{DIFF}	TX/RX channel B positive signal
56	TXVNB	A_{DIFF}	TX/RX channel B negative signal
58	TXVPC	A_{DIFF}	TX/RX channel C positive signal
59	TXVNC	A_{DIFF}	TX/RX channel C negative signal
60	TXVPD	A_{DIFF}	TX/RX channel D positive signal
61	TXVND	A_{DIFF}	TX/RX channel D negative signal

6.2.2 RGMII MAC Interface

The following table lists the device pins associated with the RGMII MAC interface. Note that the pins in this table are referenced to $VDDIO_{MAC}$ and can be set to a 2.5 V or 3.3 V power supply.

Table 80. RGMII MAC Interface Pins

Pin	Name	Type	Description
20 21 22 23	RXD3 RXD2 RXD1 RXD0	O_{ZC}	Multiplexed receive data. Bits[3:0] are synchronously output on the rising edge of RX_CLK and bits[7:4] on the falling edge of RX_CLK.
24	RX_CLK	O_{ZC}	Receive clock. Receive data is sourced from the PHY synchronously on the rising edge of RX_CLK and is the recovered clock from the media.
18	RX_CTL	O_{ZC}	Multiplexed receive data valid, receive error. This output is sampled by the MAC on opposite edges of RX_CLK to indicate two receive conditions from the PHY: 1. On the rising edge of RX_CLK, this output serves as RXDV and signals valid data is available on the RXD input data bus. 2. On the falling edge of RX_CLK, this output signals a receive error from the PHY, based on a logical derivative of RXDV and RXER, as stated by the RGMII specification.
27 28 29 30	TXD3 TXD2 TXD1 TXD0	I_{PD}	Multiplexed transmit data. Bits[3:0] are synchronously output on the rising edge of TX_CLK and bits[7:4] on the falling edge of TX_CLK.
26	TX_CLK	I	Transmit clock. This clock is 2.5 MHz for 10 Mbps mode, 25 MHz for 100 Mbps mode, and 125 MHz for 1000 Mbps mode. If left unconnected, these pins require a pull-down resistor to ground.
31	TX_CTL	I_{PD}	Multiplexed transmit enable, transmit error. This input is sampled by the PHY on opposite edges of TX_CLK to indicate two transmit conditions of the MAC: 1. On the rising edge of TX_CLK, this input serves as TXEN, indicating valid data is available on the TXD input data bus. 2. On the falling edge of TX_CLK, this input signals a transmit error from the MAC, based on a logical derivative of TXEN and TXER, as stated by the RGMII specification.
32	NSRESET	I_{PU}	Soft Reset. Active low input that places the device in a low-power state. Although the device is powered down, the sticky serial management interface registers retain their value.

Table 80. RGMII MAC Interface Pins *(continued)*

Pin	Name	Type	Description
43	OSCEN/CLKOUT	I_{PU}/O	OSCEN. This pin is sampled on the rising edge of NRESET. If HIGH (or left floating), then the on-chip oscillator circuit is enabled. If LOW, the oscillator circuit is disabled and the device must be supplied with a 25 MHz or 125 MHz reference clock to the REFCLK pin. CLKOUT. After NRESET is deasserted and OSCEN state is established, this pin becomes the clock output. The clock output can be enabled or disabled through a CMODE pin setting. Also, it can generate a reference clock frequency of 125 MHz. This pin is not active when NRESET is asserted. When disabled, the pin is held low.

6.2.3 Serial Management Interface (SMI)

The following table lists the device pins associated with the device serial management interface (SMI). Note that the pins in this table are referenced to $VDDIO_{MICRO}$ and can be set to a 2.5 V, or 3.3 V power supply.

Table 81. SMI Pins

Pin	Name	Type	Description
13	MDC	I_{PU}	Management data clock. A 0 MHz to 12.5 MHz reference input is used to clock serial MDIO data into and out of the PHY.
14	MDIO	I/O	Management data input/output pin. Serial data is written or read from this pin bidirectionally between the PHY and station manager, synchronously on the positive edge of MDC. One external pull-up resistor is required at the station manager, and its value depends on the MDC clock frequency and the total sum of the capacitive loads from the MDIO pins.
12	MDINT	OS/OD	Management interrupt signal. After reset, the device configures this pin, along with others from other devices, as active-low (open drain) or active-high (open source) based on the polarity of an external 10 kΩ resistor connection. These pins can be tied together in a wired-OR configuration with only a single pull-up or pull-down resistor.
9	EEDAT	I_{PD}/O	(Optional) EEPROM serial I/O data. Used to configure PHYs in a system without a station manager. Connect to the SDA pin of the ATMEL “AT24CXXX” serial EEPROM device family. The VSC8601 determines that an external EEPROM is present by monitoring the EEDAT pin at power-up or when NRESET is de-asserted. If EEDAT has a 4.7 kΩ external pull-up resistor, the VSC8601 assumes an EEPROM is present. The EEDAT pin can be left floating or grounded to indicate no EEPROM.

Table 81. SMI Pins *(continued)*

Pin	Name	Type	Description
10	EECLK	O_{ZC}	(Optional) EEPROM Serial Output Clock. Used to configure PHYs in a system without a station manager. Connect to the SCL pin of the ATMEL "AT24CXXX" serial EEPROM device family.
8	NRESET	I_{PU}	Device Reset. Active low input that powers down the device and sets the register bits to their default state.

6.2.4 JTAG

The following table lists the device pins associated with the device JTAG testing facility.

Table 82. JTAG Pins

Pin	Name	Type	Description
3	TDI	I_{PU5V}	JTAG test serial data input.
2	TDO	O	JTAG test serial data output.
5	TMS	I_{PU5V}	JTAG test mode select.
6	TCK	I_{PU5V}	JTAG test clock input.
7	NTRST	I_{PU5V}	JTAG reset. If JTAG is not used, then tie this pin to VSS (ground) with a pull-down resistor.

6.2.5 Miscellaneous

The following table lists the device pins associated with a particular interface or facility on the device.

Table 83. Miscellaneous Pins

Pin	Name	Type	Description
38 37 36 35	CMODE3 CMODE2 CMODE1 CMODE0	I_A	Configuration mode (CMODE) pins. For more information, see "CMODE," page 64.
64	XTAL1/REFCLK	I	Crystal oscillator input. If OSCEN=high, then a 25 MHz parallel resonant crystal with ±50 ppm frequency tolerance should be connected across XTAL1 and XTAL2. A 33 pF capacitor should also tie the XTAL1 pin to ground. Reference clock input. If OSCEN=low, the clock input frequency can either be 25 MHz (PLLMODE=0) or 125 MHz (PLLMODE is high).
63	XTAL2	O_{CRYST}	Crystal oscillator output. The crystal should be connected across XTAL1 and XTAL2. A 33 pF capacitor should also tie the XTAL2 pin to ground. If not using a crystal oscillator, this output pin can be left floating if driving XTAL1/REFCLK with a reference clock.

Table 83. Miscellaneous Pins *(continued)*

Pin	Name	Type	Description
47	PLLMODE	I	PLL mode input select. Sampled on power-up or reset. If PLLMODE is low, then REFCLK must be 25 MHz. If PLLMODE is high, then REFCLK must be 125 MHz. If a crystal or an external 25 MHz clock is used, PLLMODE must be pulled low. If an external 125 MHz clock is used, PLLMODE must be pulled high.
40 41 42	LED2 LED1 LED0	O	LED direct-drive outputs. All LEDs pins are active-low. For more information about LED operation, see "LED Interface," page 28.
50	REF_REXT	A_{BIAS}	Reference external connects to an external 2 kΩ (1%) resistor to analog ground.
49	REF_FILT	A_{BIAS}	Reference filter connects to an external 1 µF capacitor to analog ground.
44	REG_EN	I	Regulator enable. Active high input enables the on-chip switching regulator and generates a 1.2 V supply voltage.
46	REG_OUT	A_{BIAS}	Regulator output. When REG_EN is enabled, REG_OUT supplies a 1.2 V supply that has been regulated from the 3.3 V supply. When connecting to the 1.2 V supply pins, additional requirements are a 4.7 µH to 5.1 µH inductor in series as well as 10 µF and 1 µF capacitors to ground. The on-chip switching regulator is optional, and 1.2 V power can be supplied externally.
48	NC	NC	No connects. Do not connect them together or to ground. Leave these pins unconnected (floating).

6.2.6 Power Supply

The following table lists the device power supply pins.

Table 84. Power Supply Pins

Pin	Name	Type	Description
1, 39, 51, 57, 62	VDD33	3.3 V	General 3.3 V supply.
45	VDDREG	3.3 V	On-chip switching regulator 3.3 V supply.
11	VDDIOMICRO	3.3 V 2.5 V	I/O micro power supply.
16, 19, 25, 33	VDDIOMAC	3.3 V 2.5 V	I/O MAC power supply.
4, 15, 34	VDD12	1.2 V	Internal digital core voltage.
52	VDD12A	1.2 V	1.2 V analog power requiring additional PCB power supply filtering.
17 , PAD(1)	VSS	0 V	General device ground.

1. Exposed pad is on the bottom of the package.

6.2.7 Power Supply and Associated Function

Although certain function pins may not be used for a specific application, all power supply pins must be connected to their respective voltage input.

Table 85. Power Supply Pins and Associated Function Pins

Pins	Nominal Voltage	Associated Functional Pins
VDD33	3.3 V	LED[2:0], CLKOUT, NRESET, JTAG (5), XTAL1, XTAL2, CMODE, TXVP, TXVN, REF_FILT, REF_REXT
VDDIOMICRO	2.5 V, 3.3 V	MDC, MDIO, MDINT, EECLK, EEDAT
VDDIOMAC	2.5 V, 3.3 V	RXD, RX_CTL, RX_CLK, TXD, TX_CTL, TX_CLK, NSRESET

6.3 Pins by Name

This section provides an alphabetical list of the VSC8601 pins.

CMODE0	35
CMODE1	36
CMODE2	37
CMODE3	38
EECLK	10
EEDAT	9
LED0	42
LED1	41
LED2	40
MDC	13
MDINT	12
MDIO	14
NC	48
NRESET	8
NSRESET	32
NTRST	7
OSCEN/CLKOUT	43
PLLMODE	47
REF_FILT	49
REF_REXT	50
REG_EN	44
REG_OUT	46
RX_CLK	24
RX_CTL	18
RXD0	23
RXD1	22
RXD2	21
RXD3	20
TCK	6
TDI	3
TDO	2
TMS	5
TX_CLK	26
TX_CTL	31
TXD0	30
TXD1	29
TXD2	28
TXD3	27
TXVNA	54
TXVNB	56
TXVNC	59
TXVND	61
TXVPA	53
TXVPB	55
TXVPC	58
TXVPD	60
VDD12	4
VDD12	15
VDD12	34
VDD12A	52
VDD33	1
VDD33	39
VDD33	51
VDD33	57
VDD33	62
VDDIOMAC	16
VDDIOMAC	19
VDDIOMAC	25
VDDIOMAC	33
VDDIOMICRO	11
VDDREG	45
VSS	17
XTAL1/REFCLK	64
XTAL2	63

6.4 Pins by Number

This section provides a numeric list of the VSC8601 pins.

1	VDD33
2	TDO
3	TDI
4	VDD12
5	TMS
6	TCK
7	NTRST
8	NRESET
9	EEDAT
10	EECLK
11	VDDIOMICRO
12	MDINT
13	MDC
14	MDIO
15	VDD12
16	VDDIOMAC
17	VSS
18	RX_CTL
19	VDDIOMAC
20	RXD3
21	RXD2
22	RXD1
23	RXD0
24	RX_CLK
25	VDDIOMAC
26	TX_CLK
27	TXD3
28	TXD2
29	TXD1
30	TXD0
31	TX_CTL
32	NSRESET
33	VDDIOMAC
34	VDD12
35	CMODE0
36	CMODE1
37	CMODE2
38	CMODE3
39	VDD33
40	LED2
41	LED1
42	LED0
43	OSCEN/CLKOUT
44	REG_EN
45	VDDREG
46	REG_OUT
47	PLLMODE
48	NC
49	REF_FILT
50	REF_REXT
51	VDD33
52	VDD12A
53	TXVPA
54	TXVNA
55	TXVPB
56	TXVNB
57	VDD33
58	TXVPC
59	TXVNC
60	TXVPD
61	TXVND
62	VDD33
63	XTAL2
64	XTAL1/REFCLK

7 Package Information

The VSC8601 package is a lead(Pb)-free, 64-pin, plastic low-profile quad flat package (LQFP) with an exposed pad, 10 mm × 10 mm body size, 1.4 mm body thickness, 0.5 mm pin pitch, and 1.6 mm maximum height.

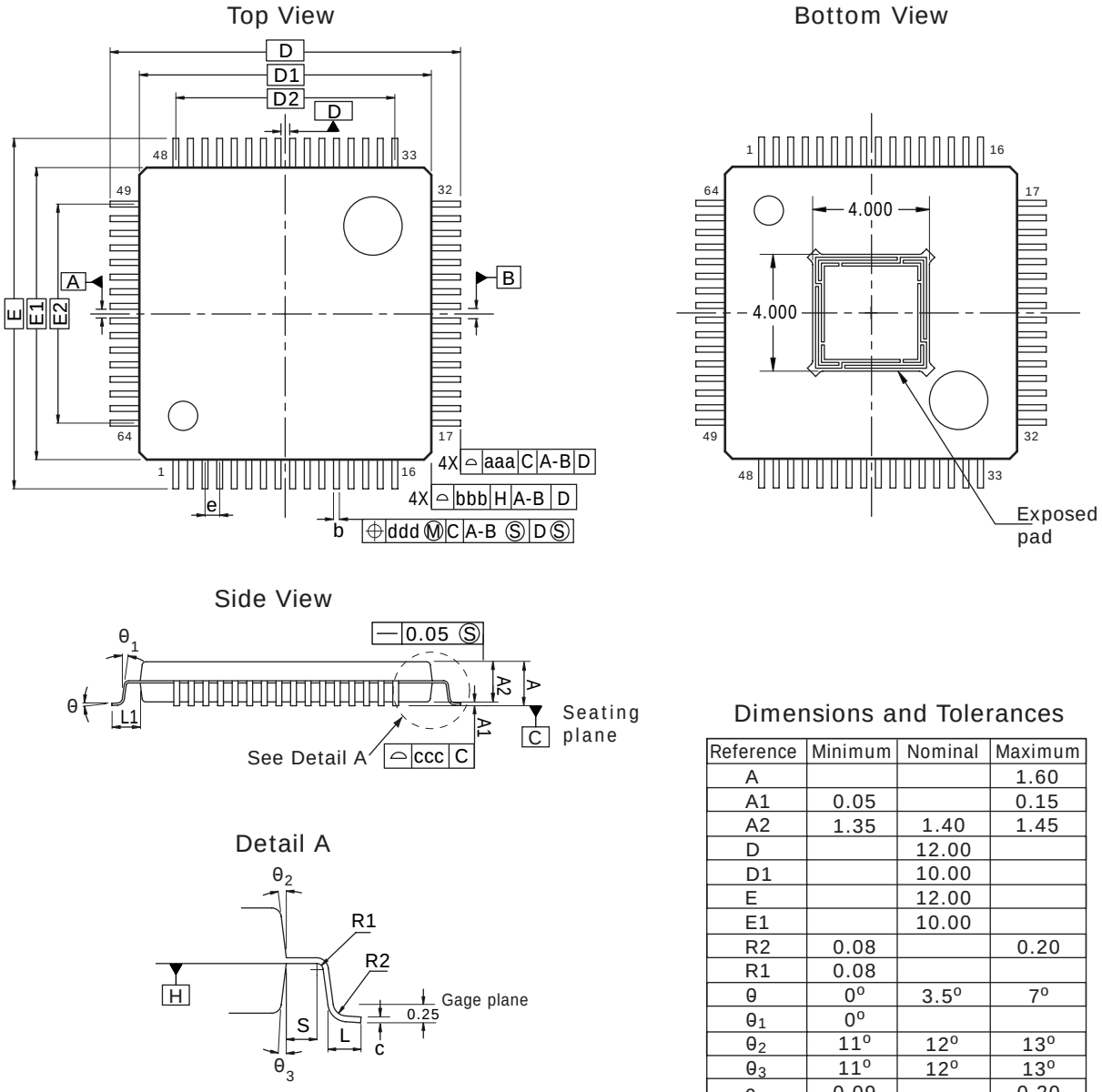
Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

This section provides the package drawing, thermal specifications, and moisture sensitivity rating for the VSC8601 device.

7.1 Package Drawing

The following illustration shows the package drawing for the VSC8601 device. The drawing contains the top view, bottom view, side view, detail views, dimensions, tolerances, and notes.

Figure 24. Package Drawing



Notes

1. All dimensions and tolerances are in millimeters (mm).
2. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25 mm per side. D1 and E1 are maximum plastic body size dimensions including mold mismatch.
3. Dimension b does not include dambar protrusion. Allowable dambar protrusion does not cause the lead width to exceed the maximum b dimension by more than 0.08 mm.

Dimensions and Tolerances

Reference	Minimum	Nominal	Maximum
A			1.60
A1	0.05		0.15
A2	1.35	1.40	1.45
D		12.00	
D1		10.00	
E		12.00	
E1		10.00	
R2	0.08		0.20
R1	0.08		
θ	0°	3.5°	7°
θ_1	0°		
θ_2	11°	12°	13°
θ_3	11°	12°	13°
c	0.09		0.20
L	0.45	0.60	0.75
L1		1.00	
S	0.20		
b	0.17	0.20	0.27
e		0.50	
D2		7.50	
E2		7.50	
aaa		0.20	
bbb		0.20	
ccc		0.08	
ddd		0.08	

7.2 Thermal Specifications

Thermal specifications for this device are based on the JEDEC standard EIA/JESD51-2 and have been modeled using a four-layer test board with two signal layers, a power plane, and a ground plane (2s2p PCB). For more information, see the JEDEC standard.

Table 86. Thermal Resistances

			θ_{JA} (°C/W) vs. Airflow (ft/min)		
Part Order Number	θ_{JC}	θ_{JB}	**0**	**100**	**200**
VSC8601XKN	18.5(1) 6.4(2)	22	33	30	28

1. Simulated on the top of the mold compound with the exposed pad soldered to a ground pad on the PCB.
2. Calculated on the exposed pad soldered to a ground pad on the PCB.

To achieve results similar to the modeled thermal resistance measurements, the guidelines for board design described in the JEDEC standard EIA/JESD51 series must be applied. For information about specific applications, see the following:

EIA/JESD51-5, *Extension of Thermal Test Board Standards for Packages with Direct Thermal Attachment Mechanisms*

EIA/JESD51-7, *High Effective Thermal Conductivity Test Board for Leaded Surface Mount Packages*

EIA/JESD51-9, *Test Boards for Area Array Surface Mount Package Thermal Measurements*

EIA/JESD51-10, *Test Boards for Through-Hole Perimeter Leaded Package Thermal Measurements*

EIA/JESD51-11, *Test Boards for Through-Hole Area Array Leaded Package Thermal Measurements*

7.3 Moisture Sensitivity

This device is rated moisture sensitivity level 3 or better as specified in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

8 Design Considerations

This section explains various issues associated with the VSC8601 device.

8.1 RX_CLK Can Reach as High as 55% Duty Cycle

Issue: When register 23, bit 8 = 0 (no internal clock skew) for RGMII, then the RX_CLK duty cycle has been measured as high as 55%.

Implications: There is a possibility that the duty cycle can go beyond this value, which then violates what is specified in the datasheet. This has only been observed when the skew setting is set to 0.

Workaround: Avoid using an RGMII skew setting of 0.

8.2 First SMI Write Fails after Software Reset

Issue: After applying software reset (using either register 0, bit 15 or the NSRESET pin), the first subsequent SMI write operation into register 4 (auto-negotiation advertisement) or register 9 (1000BASE-T control) does not work. This issue only occurs if the first SMI write after software reset is into register 4 or 9. This issue does not occur if any kind of SMI transaction (either read or write) is applied to any register between the time of the software reset and the SMI write into register 4 or 9.

Implications: The PHY may operate unexpectedly, because settings for registers 4 and 9 remain at the reset value. There are no such implications after either hardware reset or power-down events.

Workaround: Writing “0x0000” into register 31 after every software reset avoids this issue, and subsequent SMI writes into register 4 or 9 succeed.

8.3 Link-Up Issue In Forced 100BASE-TX Mode

Issue: While in the forced 100BASE-TX mode with the automatic crossover detection feature (HP Auto-MDIX) enabled, it can take up to several minutes for the link-up process between the VSC8601 device and a link partner that also has its automatic crossover detection feature enabled. The problem has not been observed in any other operation modes.

Implications: While working against some link partners, such as those by Marvell, it can take up to several minutes for the link-up process to complete.

Workaround: When forcing 100BASE-TX mode, use the following script to alter the internal method that the VSC8601 uses to perform crossover detection. For more information, see PHY API Software and Programmers Guide, which is available on the Vitesse Web site at www.vitesse.com.

```
PhyWrite (PortNo, reg_num(dec), 16_bit_unsigned_data(hex))
PhyWriteMsk (PortNo, reg_num(dec), 16_bit_unsigned_data(hex), mask(hex))
```

```
PhyWrite (PortNo, 31, 0x52B5); // Select internal register page
PhyWrite (PortNo, 16, 0xA7F8); // Request read of internal register
PhyWriteMsk (PortNo, 17, 0x0018, 0x0018); // Set for forced 100BASE-TX
PhyWriteMsk (PortNo, 18, 0, 0); // Necessary read & re-write register 18
PhyWrite (PortNo, 16, 0x87F8); // Write back modified internal register
PhyWrite (PortNo, 31, 0); // Select main register page
```

When returning from forced 100BASE-TX mode to auto-negotiation mode, use the following script to restore the standard method that VSC8601 uses to perform crossover detection:

```
PhyWrite (PortNo, 31, 0x52B5); // Select internal register page
PhyWrite (PortNo, 16, 0xA7F8); // Request read of internal register
PhyWriteMsk (PortNo, 17, 0x0000, 0x0018); // Set for auto-negotiation
PhyWriteMsk (PortNo, 18, 0, 0); // Necessary read & re-write register 18
PhyWrite (PortNo, 16, 0x87F8); // Write-back modified internal register
PhyWrite (PortNo, 31, 0); // Select main register page
```

Note It is not important which order is used for writes to the SMI register with respect to writes to Register 0, which disable and enable the auto-negotiation feature.

8.4 Default 10Base-T Settings Are Marginal and Cause MAU Test Failure

Issue: Default 10Base-T settings are marginal for PHY silicon and magnetic module variations.

Implications: It often causes the output 10Base-T signal to violate the IEEE waveform templates.

Workaround: During device initialization, use the following script. For more information, see *PHY API Software and Programmers Guide*, which is available on the Vitesse Web site at www.vitesse.com.

```
PhyWrite (PortNo, reg_num(dec), 16_bit_unsigned_data(hex))
PhyRead (PortNo, reg_num(dec))
~ -- Logical NOT
& -- Logical AND
| -- Logical OR
= -- Assign value to variable

PhyWrite (PortNo, 31, 0x52b5); // Select internal register page
PhyWrite (PortNo, 18, 0x9e); // Necessary write of internal register
PhyWrite (PortNo, 17, 0xdd39); // Necessary write of internal register
PhyWrite (PortNo, 16, 0x87aa); // Necessary write of internal register
PhyWrite (PortNo, 16, 0xa7b4); // Necessary write of internal register
reg = PhyRead (PortNo, 18); // Read internal reg. and assign it to var.
PhyWrite (PortNo, 18, reg); // Necessary write of internal register

reg = PhyRead (PortNo, 17); // Read internal reg. and assign it to var.
reg = (reg & ~0x003f) | 0x003c;// Modify variable value
PhyWrite (PortNo, 17, reg); // Write back modified internal register
```

```
PhyWrite (PortNo, 16, 0x87b4); // Necessary write of internal register
PhyWrite (PortNo, 16, 0xa794); // Necessary write of internal register
reg = PhyRead (PortNo, 18); // Read internal reg. and assign it to var.
PhyWrite (PortNo, 18, reg); // Necessary write of internal register

reg = PhyRead (PortNo, 17); // Read internal reg. and assign it to var.
reg = (reg & ~0x003f) | 0x003e;// Modify variable value
PhyWrite (PortNo, 17, reg); // Write back modified internal register

PhyWrite (PortNo, 16, 0x8794); // Necessary write of internal register
PhyWrite (PortNo, 18, 0xf7); // Necessary write of internal register
PhyWrite (PortNo, 17, 0xbe36); // Necessary write of internal register
PhyWrite (PortNo, 16, 0x879e); // Necessary write of internal register
PhyWrite (PortNo, 16, 0xa7a0); // Necessary write of internal register
reg = PhyRead (PortNo, 18); // Read internal reg. and assign it to var.
PhyWrite (PortNo, 18, reg); // Necessary write of internal register

reg = PhyRead (PortNo, 17); // Read internal reg. and assign it to var.
reg = (reg & ~0x003f) | 0x0034;// Modify variable value
PhyWrite (PortNo, 17, reg); // Write back modified internal register

PhyWrite (PortNo, 16, 0x87a0); // Necessary write of internal register

PhyWrite (PortNo, 18, 0x3c); // Necessary write of internal register
PhyWrite (PortNo, 17, 0xf3cf); // Necessary write of internal register
PhyWrite (PortNo, 16, 0x87a2); // Necessary write of internal register

PhyWrite (PortNo, 18, 0x3c); // Necessary write of internal register
PhyWrite (PortNo, 17, 0xf3cf); // Necessary write of internal register
PhyWrite (PortNo, 16, 0x87a4); // Necessary write of internal register

PhyWrite (PortNo, 18, 0x3c); // Necessary write of internal register
PhyWrite (PortNo, 17, 0xd287); // Necessary write of internal register
PhyWrite (PortNo, 16, 0x87a6); // Necessary write of internal register

PhyWrite (PortNo, 16, 0xa7a8); // Necessary write of internal register
reg = PhyRead (PortNo, 18); // Read internal reg. and assign it to var.
PhyWrite (PortNo, 18, reg); // Necessary write of internal register

reg = PhyRead (PortNo, 17); // Read internal reg. and assign it to var.
reg = (reg & ~0x0fff) | 0x0125;// Modify variable value
PhyWrite (PortNo, 17, reg); // Write back modified internal register

PhyWrite (PortNo, 16, 0x87a8); // Necessary write of internal register

PhyWrite (PortNo, 31, 0); // Select main register page
```

8.5 On-Chip Pull-up Resistor Violation

Issue: According to the IEEE standard 802.3, the MDIO pin on a slave device should be an open-drain pad type and drive a low value onto the MDIO shared bus. The MDIO shared bus should be pulled high with a pull-up resistor on the PCB or SMI bus master. The VSC8601 device includes a 100 kΩ pull-up on-chip resistor that violates this IEEE specification.

Implication: The VSC8601 device requires an off-chip and on-chip pull-up resistor for the interface to operate correctly. The typical value of the off-chip resistor is relatively small at <1 kΩ, which maintains a short rise time of the MDIO signal. Adding a 100 kΩ pull-up on-chip resistor in parallel with the off-chip pull-up resistor, does not have any practical implications.

Workaround: No workaround is needed.

8.6 Setting the Internal RGMII Timing Compensation Value

Issue: There are two inter-related registers to control the internal RGMII skew timing compensation. The finest level of control is through register 28E.15:12, which has four settings (0 ns, 1.4 ns, 1.7 ns, and 2.0 ns) for either Rx or Tx. Alternatively, register 23.8 provides a simpler level of control (0 ns or 1.7 ns for both Rx and Tx) for compatibility with legacy Vitesse PHY software. A write to either register automatically affects the other so that they are logically consistent. However, this relationship means the legacy control of register 23.8 can potentially overwrite the finer-level controls in register 28E.

Implication: If you intend to use the skew compensation settings in 28E, always write to this register after, not before, a write to register 23. For example, suppose register 23.8 is set to 1 (1.7 ns) and then register 28E.15:12 is set to 0101 (1.4 ns); the resulting delay is 1.4 ns. A subsequent write to register 23, even if bit 8 is kept as 1, automatically changes register 28E to 1010 (1.7 ns).

Workaround: Before performing a write to register 23, first read and store the settings in register 28E. After writing to register 23, write the stored value back to register 28E.

8.7 10BASE-T Harmonics at 30 MHz and 50 MHz Marginally Violate Specification

Issue: The IEEE 802.3 specification states that in 10BASE-T mode, when the DO circuit is driven by an all-ones, Manchester-encoded signal, any harmonic measured on the TD circuit must be at least 27 dB below the fundamental. In VSC8601, this specification is marginally violated at 30 MHz and 50 MHz when this measurement is made under corner conditions. Under nominal conditions, this measurement meets the IEEE specification limits.

Implications: This violation has no practical implication on the performance of the device. 10BASE-T mode has been validated to work without any issues with cables far exceeding the IEEE-specified, worst-case limits.

Workaround: None required.

8.8 Voltage Overshoot When Using On-Chip Switching Regulator

Issue: The device's on-chip switching regulator generates notable voltage overshoot.

Implications: The voltage overshoot from the on-chip switching regulator may lead to device performance issues such as CRC errors, jitter, or both.

Workaround: When using the on-chip regulator, dampen the overshoot by adding a snubber circuit on the output of the regulator pins (REG_OUT). This circuit consists of a 15 Ω resistor and 0.001 µF capacitor connected in series to the REG_OUT pins and ground. For more information about the regulator circuitry connection, see *VSC8601 Design and Layout Guide*, which is available on the Vitesse Web site at www.vitesse.com.

8.9 Long Link-Up Times Caused by Noise on the Twisted Pair Interface

Issue: The VSC8601 may experience longer link-up times during the link-up auto-negotiation process when there is signal noise coming from the link partner.

Implications: Normally, the VSC8601 device successfully links during auto-negotiation when there is signal noise coming from the link partner. However, on rare occasions, the link-up time can be significantly increased for successful auto-negotiation.

Workaround: During device initialization, it is strongly recommended that the following software script is implemented. For more information, see *PHY API Software and Programmers Guide*, which is available on the Vitesse Web site at www.vitesse.com.

```
PhyWrite (PortNo, reg_num(dec), 16_bit_unsigned_data(hex))
PhyRead (PortNo, reg_num(dec))
~ -- Logical NOT
& -- Logical AND
| -- Logical OR
= -- Assign value to variable

PHY_Write (PortNo, 31, 0x52b5);  // Select internal register page
PHY_Write (PortNo, 16, 0xa7fa); // Necessary write of internal register
reg = PHY_Read (PortNo, 18); // Read internal register and assign it to
var.
PHY_Write (PortNo, 18, reg); // Necessary write of internal register
reg = PHY_Read (PortNo, 17); // Read internal register and assign it to
var.
reg = (reg | 0x0008); // Modify variable value
PHY_Write (PortNo, 17, reg); // Write back modified internal register
PHY_Write (PortNo, 16, 0x87fa) // Necessary write of internal register
PHY_Write (PortNo, 31, 0x0000); // Select main register page
```

8.10 High VDD33 and Low VDDIOMAC Supply

Issue: If VDD33 is set to the maximum allowed 3.3 V supply and VDDIOMAC is set to the minimum allowed 3.3 V supply, the VSC8601 device can experience performance issues. These issues generally occur in a lab environment and not in typical applications.

Implications: When VDDIOMAC is set to 3.3 V, VDD33 and VDDIOMAC cannot be sourced by two different 3.3 V supplies.

Workaround: If using VDDIOMAC in 3.3 V mode, use the same 3.3 V source supply as the VDD33, using a proper filtering scheme. For more information, see *VSC8601 Design and Layout Guide*, which is available on the Vitesse Web site at www.vitesse.com.

9 Ordering Information

The VSC8601 package is a lead(Pb)-free, 64-pin, plastic low-profile quad flat package (LQFP) with an exposed pad, 10 mm × 10 mm body size, 1.4 mm body thickness, 0.5 mm pin pitch, and 1.6 mm maximum height.

Lead(Pb)-free products from Vitesse comply with the temperatures and profiles defined in the joint IPC and JEDEC standard IPC/JEDEC J-STD-020. For more information, see the IPC and JEDEC standard.

The following table lists the ordering information for the VSC8601 device.

Table 87. Ordering Information

Part Order Number	Description
VSC8601XKN	Lead(Pb)-free, 64-pin, plastic LQFP with an exposed pad, 10 mm × 10 mm body size, 1.4 mm body thickness, 0.5 mm pin pitch, and 1.6 mm maximum height

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View VSC8601XKN on WIN SOURCE
- Microsemi Corporation Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management