THE DATASHEET OF

ZL2008ALBFT1

ZL2008

Digital DC/DC Controller with Drivers and Pin-Strap Current Sharing

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Rev 4.00
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The ZL2008 is a digital power controller with integrated MOSFET drivers. Current sharing allows multiple devices to be connected in parallel to source loads with very high current demands. Adaptive performance optimization algorithms improve power conversion efficiency. Zilker Labs Digital-DC™ technology enables a blend of power conversion performance and power management features.

The ZL2008 is designed to be a flexible building block for DC power and can be easily adapted to designs ranging from a single-phase power supply operating from a 3.3V input to a multi-phase supply operating from a 12V input. The ZL2008 eliminates the need for complicated power supply managers as well as numerous external discrete components.

Key operating features can be configured by pin-straps, including compensation, current sharing and output voltage. The ZL2008 uses the I^2C/SMBus™ with PMBus™ protocol for communication with a host controller and the Digital-DC bus for communication between Zilker Labs devices.

Applications

- Servers/storage equipment
- Telecom/datacom equipment
- Power supply modules

Features

Power Conversion

- Efficient synchronous buck controller
- Adaptive light load efficiency optimization
- 3V to 14V input range
- 0.54V to 5.5V output range (with margin)
- POLA and DOSA voltage trim modes
- ±1% output voltage accuracy
- Internal 3A MOSFET drivers
- Fast load transient response
- Current sharing and phase interleaving
- *Snapshot™* parameter capture
- RoHS compliant (6mmx6mm) QFN package

Power Management

- Digital soft-start/stop
- Precision delay and ramp-up
- Power good/enable
- Voltage tracking, sequencing and margining
- Voltage, current and temperature monitoring
- I^2C/SMBus interface, PMBus compatible
- Output voltage and current protection
- Internal non-volatile memory (NVM)

Block Diagram

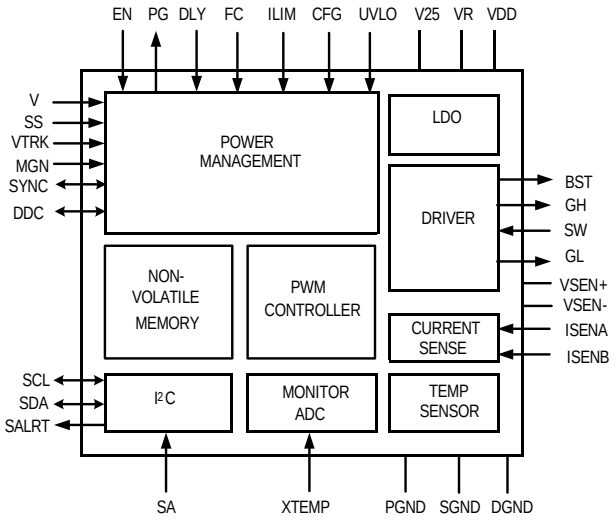

FIGURE 1. BLOCK DIAGRAM

Efficiency vs Load Current

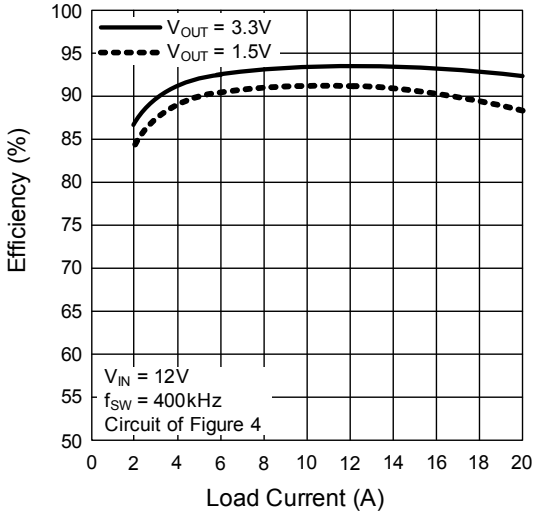

FIGURE 2. EFFICIENCY vs LOAD CURRENT

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Absolute Maximum Ratings

DC Supply Voltage for VDD Pin . . . . . -0.3V to 17V
MOSFET Drive Reference for VR Pin. . . . . -0.3V to 6.5V
2.5V Logic Reference for V25 Pin . . . . . -0.3V to 3V
Logic I/O Voltage for CFG(0, 1 ,2), DDC, EN, FC(0,1), ILIM, MGN, PG, PH_EN, SA(0, 1), SALRT, SCL, SDA, SS, SYNC, UVLO, V(0, 1) Pins . . . . . -0.3V to 6V
Analog Input Voltages for ISENB, VSEN, VTRK, XTEMP Pins . . . . . -0.3V to 6.5V
Analog Input Voltages for ISENA PIn . . . . . -1.5V to 6.5V
High Side Supply Voltage for BST Pin . . . . . -0.3V to 30V
Boost to Switch Voltage for BST -SW Pins . . . . . -0.3V to 8V
High Side Drive Voltage for GH Pin . . . . . (V_{SW}-0.3V) to (V_{BST}+0.3V)
Low Side Drive Voltage for GL Pin . . . . . (PGND-0.3V) to (VR+0.3V)
Switch Node Continuous for SW Pin . . . . . (PGND-0.3V) to 30V
Switch Node Transient (<100ns) for SW Pin . . . . . (PGND-5V) to 30V
Ground Differential for DGND – SGND, PGND - SGND Pins . . . . . -0.3V to 0.3V
ESD Rating
Human Body Model (Note 1, Tested per JESD22-A114E) 2kV
Machine Model (Tested per JESD22-A115-A) 500V
Latch Up (Tested per JESD78) 100mA

Thermal Information

Thermal Resistance (Typical)	θ_{JA} (°C/W)	θ_{JC} (°C/W)
36 Ld QFN (Notes 2, 3)	35	5

Junction Temperature . . . . . -55°C to +150°C
Storage Temperature . . . . . -55°C to +150°C
Pb-Free Reflow Profile . . . . . see link below
http://www.intersil.com/pbfree/Pb-FreeReflow.asp

Recommended Operating Conditions

Input Supply Voltage Range, V_{DD} (See Figure 9)
VDD tied to VR. . . . . 3.0V to 5.5V
VR floating. . . . . 4.5V to 14V
Output Voltage Range, V_{OUT} (Note 4) . . . . . 0.54V to 5.5V
Operating Junction Temperature Range, T_J . . . . . -40°C to +125°C
Input Voltage
V_{IN}, Rise Time . . . . . 5ms minimum
V_{IN} Ramp . . . . . Monotonic

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product reliability and result in failures not covered by warranty.

NOTES:

1. BST, SW pins rated at 1.5kV.
2. θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.
3. For θ_{JC}, the “case temp” location is the center of the exposed metal pad on the package underside.
4. Includes margin limits.

Electrical Specifications

V_{DD} = 12V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C.**

PARAMETER	CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
Input and Supply Characteristics					
I_{DD} Supply Current at f_{SW} = 200kHz	GH, GL no load	–	16	30	mA
I_{DD} Supply Current at f_{SW} = 1.4MHz	MISC_CONFIG[7] = 1	–	25	50	mA
I_{DDS} Shutdown Current	EN = 0V No I^2C/SMBus activity	–	6.5	9	mA
Vr Reference Output Voltage	V_{DD} > 6V, I_{VR} < 20mA	4.5	5.2	5.5	V
V25 Reference Output Voltage	V_R > 3V, I_{V25} < 20mA	2.25	2.5	2.75	V
Output Characteristics					
Output Voltage Adjustment Range (Note 5)	V_{IN} > V_{OUT}	0.6	–	5.0	V
Output Voltage Set-point Resolution	Set using resistors	–	10	–	mV
	Set using I^2C/SMBus	–	±0.025	–	% FS (Note 6)
Output Voltage Accuracy (Note 7)	Includes line, load, temp	-1	–	1	%
Vsen Input Bias Current	VSEN = 5.5V	–	110	200	µA
Current Sense Differential Input Voltage (Ground Referenced)	V_{ISENA} -V_{ISENB}	-100	–	100	mV
Current Sense Differential Input Voltage (V_{out} Referenced, V_{out} < 4.0V)	V_{ISENA} -V_{ISENB}	-50	–	50	mV
Current Sense Input Bias Current	Ground referenced	-100	–	100	µA

Electrical Specifications

V_{DD} = 12V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
Current Sense Input Bias Current (V_{out} Referenced, V_{out} < 4.0V)	ISENA	-1	–	1	µA
	ISENB	-100	–	100	µA
Soft-start Delay Duration Range (Note 8)	Set using SS pin or resistor	2	–	30	ms
	Set using I²C/SMBus	0.002	–	500	s
Soft-start Delay Duration Accuracy	Turn-on delay (precise mode) (Notes 8, 9, 10)	-	±0.25	-	ms
	Turn-on delay (normal mode) (Note 10)	-	-0.25/+4	-	ms
	Turn-off delay (Note 10)	-	-0.25/+4	-	ms
Soft-start Ramp Duration Range	Set using SS pin or resistor	2	–	20	ms
	Set using I²C	0	–	200	ms
Soft-start Ramp Duration Accuracy		–	100	–	µs
Logic Input/Output Characteristics					
Logic Input Leakage Current	EN, PG, SCL, SDA, SALRT pins	-250	–	250	nA
Logic Input Low, V_{IL}		–	–	0.8	V
Logic Input OPEN (N/C)	Multi-mode logic pins	–	1.4	–	V
Logic Input High, V_{IH}		2.0	–	–	V
Logic Output Low, V_{OL}	$I_{OL} \leq$ 4mA	–	–	0.4	V
Logic Output High, V_{OH}	$I_{OH} \geq$ -2mA	2.25	–	–	V
Oscillator and Switching Characteristics					
Switching Frequency Range		200	–	1400	kHz
Switching Frequency Set-point Accuracy	Predefined settings (See Table 11)	-5	–	5	%
Maximum Pwm Duty Cycle	Factory default	95	–	–	%
Minimum Sync Pulse Width		150	–	–	ns
Input Clock Frequency Drift Tolerance	External clock source	-13	–	13	%
Gate Drivers					
High-side driver voltage (V_{BST} -V_{SW})		–	4.5	–	V
High-side Driver Peak Gate Drive Current (Pull-down)	(V_{BST} -V_{SW}) = 4.5V	2	3	–	A
High-side Driver Pull-up Resistance	(V_{BST} -V_{SW}) = 4.5V, (V_{BST} -V_{GH}) = 50mV	–	0.8	2	Ω
High-side Driver Pull-down Resistance	(V_{BST} -V_{SW}) = 4.5V, (V_{GH} -V_{SW}) = 50mV	–	0.5	2	Ω
Low-side Driver Peak Gate Drive Current (Pull-up)	V_R = 5V	–	2.5	–	A
Low-side Driver Peak Gate Drive Current (Pull-down)	V_R = 5V	–	1.8	–	A
Low-side Driver Pull-up Resistance	V_R = 5V, (V_R -V_{GL}) = 50mV	–	1.2	2	Ω
Low-side Driver Pull-down Resistance	V_R = 5V, (V_{GL} -PGND) = 50mV	–	0.5	2	Ω
Switching Timing					
Gh Rise and Fall Time	(V_{BST} -V_{SW}) = 4.5V, C_{LOAD} = 2.2nF	–	5	20	ns
Gl Rise and Fall Time	V_R = 5V, C_{LOAD} = 2.2nF	–	5	20	ns
Tracking					
VTRK Input Bias Current	VTRK = 5.5V	–	110	200	µA
VTRK Tracking Ramp Accuracy	100% Tracking, V_{OUT} -VTRK	-100	–	+ 100	mV
VTRK Regulation Accuracy	100% Tracking, V_{OUT} -VTRK	-1	–	1	%

Electrical Specifications

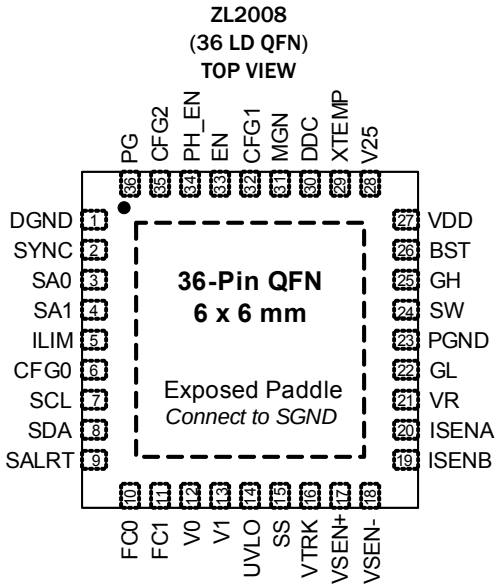
V_{DD} = 12V, T_A = -40°C to +85°C unless otherwise noted. Typical values are at T_A = +25°C. **Boldface limits apply over the operating temperature range, -40°C to +85°C. (Continued)**

PARAMETER	CONDITIONS	MIN (Note 14)	TYP	MAX (Note 14)	UNIT
Fault Protection Characteristics					
UVLO Threshold Range	Configurable via I²C/SMBus	**2.85**	–	**16**	V
UVLO Set-point Accuracy		**-150**	–	**150**	mV
UVLO Hysteresis	Factory default	**–**	3	**–**	%
	Configurable via I²C/SMBus	**0**	–	**100**	%
UVLO Delay		**–**	–	**2.5**	µs
Power Good V_{OUT} Threshold	Factory default	**–**	90	**–**	% V_{OUT}
Power Good V_{OUT} Hysteresis	Factory default	**–**	5	**–**	%
Power Good Delay	Using pin-strap or resistor (Note 11)	**0**	–	**200**	ms
	Configurable via I²C/SMBus	**0**	–	**500**	s
VSEN Undervoltage Threshold	Factory default	**–**	85	**–**	% V_{OUT}
	Configurable via I²C/SMBus	**0**	–	**110**	% V_{OUT}
VSEN Overvoltage Threshold	Factory default	**–**	115	**–**	% V_{OUT}
	Configurable via I²C/SMBus	**0**	–	**115**	% V_{OUT}
VSEN Undervoltage Hysteresis		**–**	5	**–**	% V_{OUT}
VSEN Undervoltage/Overvoltage Fault Response Time	Factory default	**–**	16	**–**	µs
	Configurable via I²C/SMBus	**5**	–	**60**	µs
Current Limit Set-point Accuracy (V_{OUT} Referenced)		**–**	±10	**–**	% FS (Note 12)
Current Limit Set-point Accuracy (Ground Referenced)		**–**	±10	**–**	% FS (Note 12)
Current Limit Protection Delay	Factory default	**–**	5	**–**	t_{SW} (Note 13)
	Configurable via I²C/SMBus	**1**	–	**32**	t_{SW} (Note 13)
Temperature Compensation of Current Limit Protection Threshold	Factory default		4400		ppm/°C
	Configurable via I²C/SMBus	**100**		**12700**	
Thermal Protection Threshold (Junction Temperature)	Factory default	**–**	125	**–**	°C
	Configurable via I²C/SMBus	**-40**	–	**125**	°C
Thermal Protection Hysteresis		**–**	15	**–**	°C

NOTES:

5. Does not include margin limits.
6. Percentage of Full Scale (FS) with temperature compensation applied.
7. V_{OUT} measured at the termination of the VSEN+ and VSEN-sense points.
8. The device requires a delay period following an enable signal and prior to ramping its output. Precise timing mode limits this delay period to approx 2ms, where in normal mode it may vary up to 4ms. Current Share member minimum delay is 5ms. Current share reference must be 10ms greater than member delay.
9. Precise ramp timing mode is only valid when using EN pin to enable the device rather than PMBus enable.
10. The devices may require up to a 4ms delay following the assertion of the enable signal (normal mode) or following the de-assertion of the enable signal.
11. Factory default Power Good delay is set to the same value as the soft-start ramp time.
12. Percentage of Full Scale (FS) with temperature compensation applied
13. $t_{SW} = 1/f_{SW}$, where f_{SW} is the switching frequency.
14. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
15. Nominal capacitance of logic pins is 5pF.

Pin Configuration



Pin Descriptions

Pin	Label	Type (Note 16)	Description
1	DGND	PWR	Digital ground. Common return for digital signals. Connect to low impedance ground plane.
2	SYNC	I/O, M (Note 17)	Clock synchronization input. Used to set switching frequency of internal clock or for synchronization to external frequency reference.
3	SA0	I, M	Serial address select pins. Used to assign unique SMBus address to each IC or to enable certain management features.
4	SA1		
5	ILIM	I, M	Current limit select. Sets the overcurrent threshold voltage for ISENA and ISENB.
6	CFG0	I, M	Configuration pin. Used to setup current sharing and non-linear response.
7	SCL	I/O	Serial clock. Connect to external host and/or to other ZL devices.
8	SDA	I/O	Serial data. Connect to external host and/or to other ZL devices.
9	SALRT	O	Serial alert. Connect to external host if desired.
10	FC0	I	Loop compensation configuration pins.
11	FC1		
12	V0	I	Output voltage selection pins. Used to set V_{OUT} set-point and V_{OUT} max.
13	V1		
14	UVLO	I, M	Undervoltage lockout selection. Sets the minimum value for V_{DD} voltage to enable V_{OUT}.
15	SS	I, M	Soft-start pin. Sets the output voltage ramp time during turn-on and turn-off. Sets the delay from when EN is asserted until the output voltage starts to ramp.
16	VTRK	I	Tracking sense input. Used to track an external voltage source.
17	VSEN+	I	Output voltage feedback. Connect to output regulation point.
18	VSEN-	I	Output voltage feedback. Connect to load return or ground regulation point.
19	ISENB	I	Differential voltage input for current limit.
20	ISENA	I	Differential voltage input for current limit. High voltage tolerant.

Pin Descriptions (Continued)

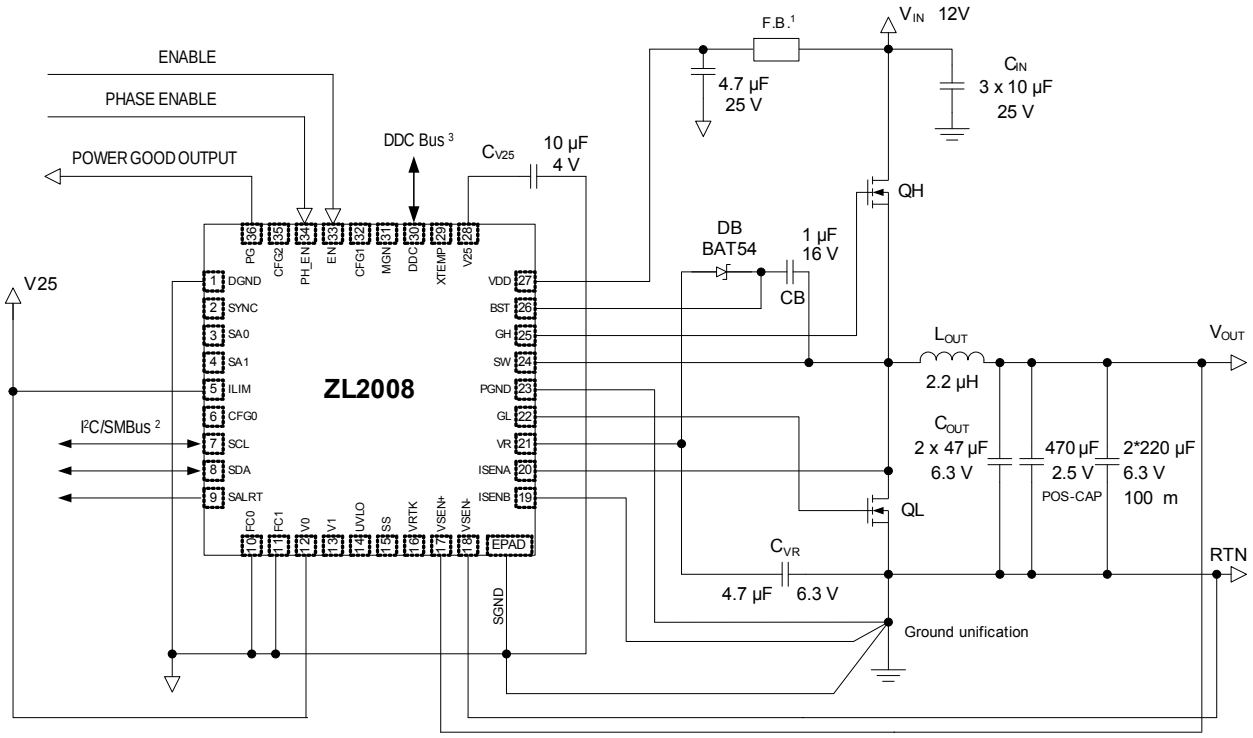
Pin	Label	Type (Note 16)	Description
21	VR	PWR	Internal 5V reference used to power internal drivers.
22	GL	O	Low side FET gate drive.
23	PGND	PWR	Power ground. Connect to low impedance ground plane.
24	SW	PWR	Drive train switch node.
25	GH	O	High-side FET gate drive.
26	BST	PWR	High-side drive boost voltage.
27	VDD (Note 18)	PWR	Supply voltage.
28	V25	PWR	Internal 2.5V reference used to power internal circuitry.
29	XTEMP	I	External temperature sensor input. Connect to external 2N3904 diode connected transistor.
30	DDC	I/O	Digital-DC Bus. (Open Drain) Interoperability between Zilker Labs devices.
31	MGN	I	Signal that enables margining of output voltage.
32	CFG1	I, M	Configuration pin. Used to setup clock synchronization and sequencing.
33	EN	I	Enable input (active high). Pull-up to enable PWM switching and pull-down to disable PWM switching.
34	PH_EN	I	Phase enable input (active high). Pull-up to enable phase and pull-down to disable phase for current sharing.
35	CFG2	I, M	Configuration pin. Sets the phase offset (single-phase) or current sharing group position (multi-phase).
36	PG	O	Power good output.
ePad	SGND	PWR	Exposed thermal pad. Common return for analog signals; internal connection to SGND. Connect to low impedance ground plane.

NOTES:

16. I = Input, O = Output, PWR = Power or Ground. M = Multi-mode pins. Please refer to “Multi-mode Pins” on page 12.
17. The SYNC pin can be used as a logic pin, a clock input or a clock output.
18. V_{DD} is measured internally and the value is used to modify the PWM loop gain.

Typical Application Circuit

The following application circuit represents a typical implementation of the ZL2008. For PMBus operation, it is recommended to tie the enable pin (EN) to SGND.



Notes:
1. Ferrite bead is optional for input noise suppression
2. The I²C/SMBus requires pull-up resistors. Please refer to the I²C/SMBus specifications for more details.
3. The DDC bus requires a pull-up resistor. The resistance will vary based on the capacitive loading of the bus(and on the number of devices connected). The 10 kΩ default value, assuming a maximum of 100 pF per device, provides the necessary 1 µs pull-up rise time. Please refer to the DDC Bus section for more details

FIGURE 3. 12V to 1.8V/16A Application Circuit

ZL2008 Overview

Digital-DC Architecture

The ZL2008 is an innovative mixed-signal power conversion and power management IC based on Zilker Labs patented Digital-DC technology that provides an integrated, high performance step-down converter for a wide variety of power supply applications.

Today's embedded power systems are typically designed for optimal efficiency at maximum load, reducing the peak thermal stress by limiting the total thermal dissipation inside the system. Unfortunately, many of these systems are often operated at load levels far below the peak where the power system has been optimized, resulting in reduced efficiency. While this may not cause thermal stress to occur, it does contribute to higher electricity usage and results in higher overall system operating costs.

Zilker Labs' efficiency-adaptive ZL2008 DC/DC controller helps mitigate this scenario by enabling the power converter to automatically change their operating state to increase efficiency and overall performance with little or no user interaction needed.

Its unique PWM loop utilizes an ideal mix of analog and digital blocks to enable precise control of the entire power conversion process with no software required, resulting in a very flexible device that is also very easy to use. An extensive set of power management functions are fully integrated and can be configured using simple pin connections. The user configuration can be saved in an internal non-volatile memory (NVM). Additionally, all functions can be configured and monitored via the SMBus hardware interface using standard PMBus commands, allowing ultimate flexibility.

Once enabled, the ZL2008 is immediately ready to regulate power and perform power management tasks with no programming required. Advanced configuration options and real-time configuration changes are available via the I^2C/SMBus interface if desired and continuous monitoring of multiple operating parameters is possible with minimal interaction from a host controller. Integrated sub-regulation circuitry enables single supply operation from any supply between 3V and 14V with no secondary bias supplies needed.

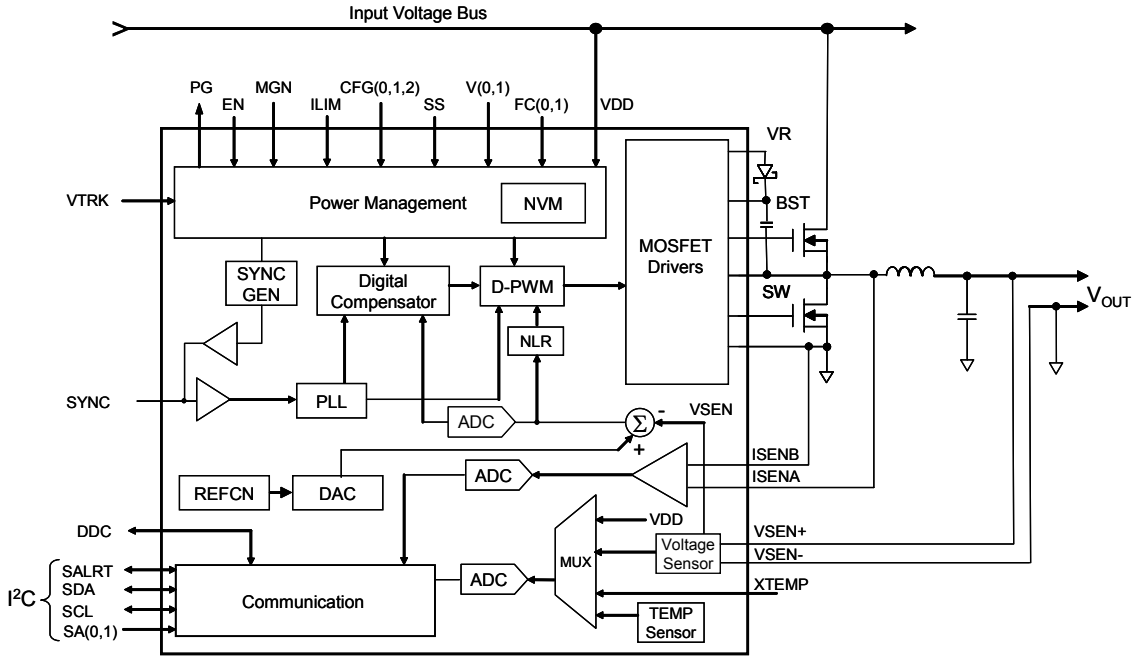


FIGURE 4. ZL2008 Block Diagram

Power Conversion Overview

The ZL2008 operates as a voltage-mode, synchronous buck converter with a selectable constant frequency pulse width modulator (PWM) control scheme that uses external MOSFETs, capacitors, and an inductor to perform power conversion.

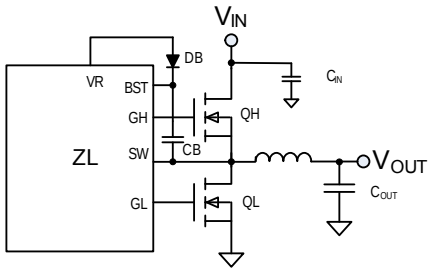


FIGURE 5. Synchronous Buck Converter

Figure 5 illustrates the basic synchronous buck converter topology showing the primary power train components. This converter is also called a step-down converter, as the output voltage must always be lower than the input voltage. In its most simple configuration, the ZL2008 requires two external N-channel power MOSFETs, one for the top control MOSFET (QH) and one for the bottom synchronous MOSFET (QL). The amount of time that QH is on as a fraction of the total switching period is known as the duty cycle *D*, which is described by Equation 1:

$$D \approx \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 1)}$$

During time D, QH is on and $V_{IN} - V_{OUT}$ is applied across the inductor. The current ramps up as shown in Figure 6.

When QH turns off (time 1-D), the current flowing in the inductor must continue to flow from the ground up through QL, during which the current ramps down. Since the output capacitor C_{OUT} exhibits a low impedance at the switching frequency, the AC component of the inductor current is filtered from the output voltage so the load sees nearly a DC voltage.

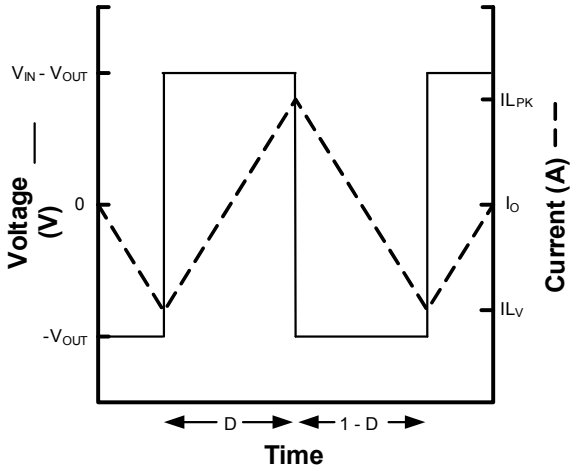


FIGURE 6. Inductor Waveform

Typically, buck converters specify a maximum duty cycle that effectively limits the maximum output voltage that can be realized for a given input voltage. This duty cycle limit ensures that the lowside MOSFET is allowed to turn on for a minimum amount of time during each switching cycle, which enables the bootstrap capacitor (CB in Figure 5) to be charged up and provide adequate gate drive voltage for the high-side MOSFET. See section“High-side Driver Boost Circuit” on page 12 for more details.

In general, the size of components L1 and C_{OUT} as well as the overall efficiency of the circuit are inversely proportional to the switching frequency, f_{SW}. Therefore, the highest efficiency circuit may be realized by switching the MOSFETs at the lowest possible frequency; however, this will result in the largest component size. Conversely, the smallest possible footprint may be realized by switching at the fastest possible frequency but this gives a somewhat lower efficiency. Each user should determine the optimal combination of size and efficiency when determining the switching frequency for each application.

The block diagram for the ZL2008 is illustrated in Figure 4. In this circuit, the target output voltage is regulated by connecting the differential VSEN pins directly to the output regulation point. The VSEN signal is then compared to a reference voltage that has been set to the desired output voltage level by the user. The error signal derived from this comparison is converted to a digital value with a low-resolution, analog to digital (A/D) converter. The digital signal is applied to an adjustable digital compensation filter, and the compensated signal is used to derive the appropriate PWM duty cycle for driving the external MOSFETs in a way that produces the desired output.

The ZL2008 has several features to improve the power conversion efficiency. A non-linear response (NLR) loop improves the response time and reduces the output deviation as a result of a load transient. The ZL2008 monitors the power converter’s operating conditions and continuously adjusts the turn-on and turn-off timing of the high-side and low-side MOSFETs to optimize the overall efficiency of the power supply. Adaptive performance optimization algorithms such as dead-time control, diode emulation, and frequency control are available to provide greater efficiency improvement.

Power Management Overview

The ZL2008 incorporates a wide range of configurable power management features that are simple to implement with no external components. Additionally, the ZL2008 includes circuit protection features that continuously safeguard the device and load from damage due to unexpected system faults. The ZL2008 can continuously monitor input voltage, output voltage/current, internal temperature, and the temperature of an external thermal diode. A Power Good output signal is also included to enable power-on reset functionality for an external processor.

All power management functions can be configured using either pin configuration techniques (see Figure 7) or via the I^2C/SMBus interface. Monitoring parameters can also be pre-configured to provide alerts for specific conditions. See Application Note AN2033 for more details on SMBus monitoring.

Multi-mode Pins

In order to simplify circuit design, the ZL2008 incorporates patented multi-mode pins that allow the user to easily configure many aspects of the device with no programming. Most power management features can be configured using these pins. The multi-mode pins can respond to four different connections as shown in Table 1. These pins are sampled when power is applied or by issuing a PMBus Restore command (See Application Note AN2033).

Pin-strap Settings: This is the simplest implementation method, as no external components are required. Using this method, each pin can take on one of three possible states: LOW, OPEN, or HIGH. These pins can be connected to the V25 pin for logic HIGH settings as this pin provides a regulated voltage higher than 2V. Using a single pin, one of three settings can be selected. Using two pins, one of nine settings can be selected.

TABLE 1. Multi-mode Pin Configuration

Pin Tied To	Value
LOW (Logic LOW)	< 0.8VDC
OPEN (N/C)	No connection
HIGH (Logic HIGH)	> 2.0VDC
Resistor to SGND	Set by resistor value

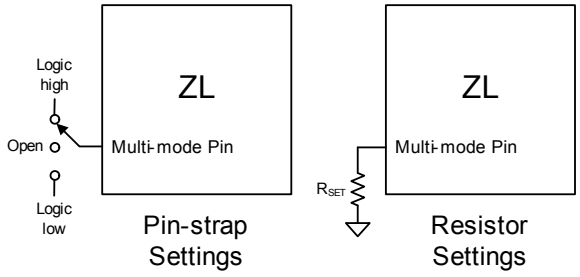


FIGURE 7. Pin-strap and Resistor Setting Examples

Resistor Settings: This method allows a greater range of adjustability when connecting a finite value resistor (in a specified range) between the multi-mode pin and SGND. Standard 1% resistor values are used, and only every fourth E96 resistor value is used so the device can reliably recognize the value of resistance connected to the pin while eliminating the error associated with the resistor accuracy. Up to 31 unique selections are available using a single resistor.

I²C/SMBus Method: Almost any ZL2008 function can be configured via the I²C/SMBus interface using standard PMBus commands. Additionally, any value that has been configured using the pin-strap or resistor setting methods can also be re-configured and/or verified via the I²C/SMBus. See Application Note AN2033 for more details.

The SMBus device address and VOUT_MAX are the only parameters that must be set by external pins. All other device parameters can be set via the I²C/SMBus. The device address is set using the SA0 and SA1 pins. VOUT_MAX is determined as 10% greater than the voltage set by the V0 and V1 pins.

Power Conversion Functional Description

Internal Bias Regulators and Input Supply Connections

The ZL2008 employs two internal low dropout (LDO) regulators to supply bias voltages for internal circuitry, allowing it to operate from a single input supply. The internal bias regulators are as follows:

VR: The VR LDO provides a regulated 5V bias supply for the MOSFET driver circuits. It is powered from the VDD pin. A 4.7µF filter capacitor is required at the VR pin.

V25: The V25 LDO provides a regulated 2.5V bias supply for the main controller circuitry. It is powered from an internal 5V node. A 10µF filter capacitor is required at the V25 pin.

When the input supply (VDD) is higher than 5.5V, the VR pin should not be connected to any other pins. It should only have a filter capacitor attached as shown in Figure 8. Due to the dropout voltage associated with the VR bias regulator, the VDD pin must be connected to the VR pin for designs operating from a supply below 5.5V. Figure 8 illustrates the required connections for both cases.

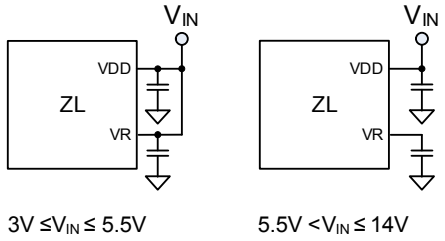


FIGURE 8. Input Supply Connections

Note: the internal bias regulators are not designed to be outputs for powering other circuitry. Do not attach external loads to any of these pins. The multi-mode pins may be connected to the V25 pin for logic HIGH settings.

High-side Driver Boost Circuit

The gate drive voltage for the high-side MOSFET driver is generated by a floating bootstrap capacitor, CB (see Figure 5). When the lower MOSFET (QL) is turned on, the SW node is pulled to ground and the capacitor is charged from the internal VR bias regulator through diode DB. When QL turns off and the upper MOSFET (QH) turns on, the SW node is pulled up to V_{DD} and the voltage on the bootstrap capacitor is boosted approximately 5V above V_{DD} to provide the necessary voltage to power the high-side driver. A Schottky diode should be used for DB to help maximize the high-side drive supply voltage.

Output Voltage Selection

STANDARD MODE

The output voltage may be set to any voltage between 0.6V and 5.0V provided that the input voltage is higher than the desired output voltage by an amount sufficient to prevent the device from exceeding its maximum duty cycle specification. Using the pin-strap method, V_{OUT} can be set to any of nine standard voltages as shown in Table 2.

TABLE 2. Output Voltage Pin-strap Settings

		V0		
		LOW (V)	OPEN (V)	HIGH (V)
V1	LOW	0.6	0.8	1.0
	OPEN	1.2	1.5	1.8
	HIGH	2.5	3.3	5.0

The resistor setting method can be used to set the output voltage to levels not available in Table 2. Resistors R0 and R1 are selected to produce a specific voltage between 0.6V and 5.0V in 10mV steps. Resistor R1 provides a coarse setting and resistor R0 provides a fine adjustment, thus eliminating the additional errors associated with using two 1% resistors (this typically adds approx 1.4% error).

To set V_{OUT} using resistors, follow the steps below to calculate an index value and then use Table 3 to select the resistor that corresponds to the calculated index value as follows:

1. Calculate Index1:
   Index1 = 4 x V_{OUT} (V_{OUT} in 10mV steps)
2. Round the result down to the nearest whole number.
3. Select the value of R1 from Table 3 using the Index1 rounded value from step 2.
4. Calculate Index0:
5. Index0 = 100 x V_{OUT} – (25 x Index1)
6. Select the value of R0 from Table 3 using the Index0 value from Step 4.

TABLE 3. Output Voltage Resistors Settings

Index	R0 or R1 (kΩ)
0	10
1	11
2	12.1
3	13.3
4	14.7
5	16.2
6	17.8
7	19.6
8	21.5
9	23.7
10	26.1
11	28.7
12	31.6
13	34.8
14	38.3
15	42.2
16	46.4
17	51.1
18	56.2
19	61.9
20	68.1
21	75
22	82.5
23	90.9
24	100

Example from Figure 9: For V_{OUT} = 1.33V,

Index1 = 4 x 1.33V = 5.32;

From Table 3, R1 = 16.2kΩ

Index0 = (100 x 1.33V) – (25 x 5) = 8;

From Table 3, R0 = 21.5kΩ

SMBUS MODE

The output voltage may be set to any value between 0.6V and 5.0V using a PMBus command over the I^2C/SMBus interface. See Application Note AN2033 for details.

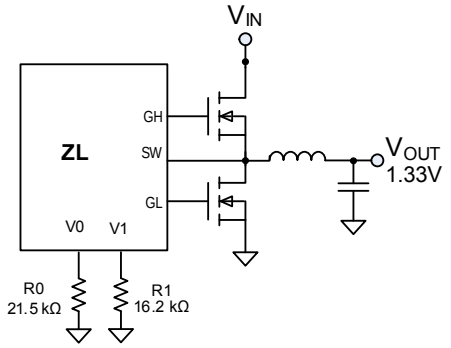


FIGURE 9. Output Voltage Resistor Setting Example

POLA VOLTAGE TRIM MODE

The output voltage mapping can be changed to match the voltage setting equations for POLA and DOSA standard modules.

The standard method for adjusting the output voltage for a POLA module is defined by Equation 2:

$$R_{SET} = 10k\Omega \times \frac{0.69V}{V_{OUT} - 0.69V} - 1.43k\Omega \quad \text{(EQ. 2)}$$

The resistor, R_{SET}, is external to the POLA module. See Figure 10.

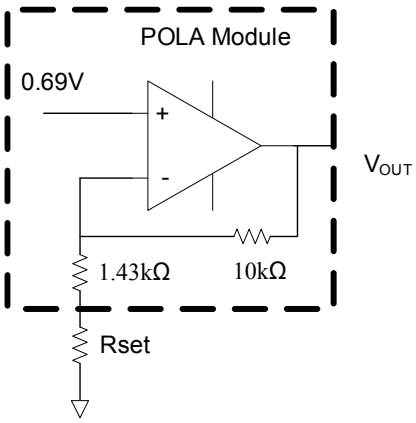


FIGURE 10. Output Voltage Setting on POLA Module

To stay compatible with this existing method for adjusting the output voltage and to keep the same external R_{SET} resistor when using the ZL2008, the module manufacturer should add a 10kΩ resistor on the module as shown in Figure 11. Now, the same R_{SET} used for an analog POLA module will provide the same output voltage when using a digital POLA module based on the ZL2008.

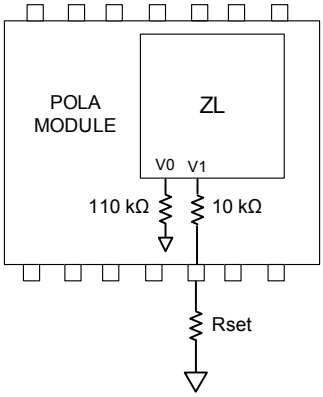


FIGURE 11. R_{SET} on a POLA Module

The POLA mode is activated through pin-strap by connecting a 110kΩ resistor on V0 to SGND. The V1 pin is then used to adjust the output voltage as shown in Table 4.

The POLA mode can also be activated through PMBus commands. See Application Note AN2033 for more details.

TABLE 4. POLA Mode V_{OUT} Settings

V_{OUT} (V)	R_{SET} (kΩ) In series with 10kΩ resistor
0.700	162
0.752	110
0.758	100
0.765	90.9
0.772	82.5
0.790	75.0
0.800	56.2
0.821	51.1
0.834	46.4
0.848	42.2
0.880	34.8
0.899	31.6
0.919	28.7
0.965	23.7
0.991	21.5
1.000	19.6
1.100	16.2
1.158	13.3
1.200	12.1
1.250	9.09
1.500	7.50
1.669	5.62
1.800	4.64
2.295	2.87
2.506	2.37
3.300	1.21
5.000	0.162

NOTE: (R0 = 110kΩ, R1 = R_{SET} + 10kΩ)

DOSA VOLTAGE TRIM MODE

On a DOSA module, the V_{OUT} setting follows Equation 3:

$$R_{SET} = \frac{6900}{V_{OUT} - 0.69V} \quad \text{(EQ. 3)}$$

To maintain DOSA compatibility, the same scheme is used as with a POLA module except the 10kΩ resistor is replaced with a 8.66kΩ resistor as shown in Figure 12.

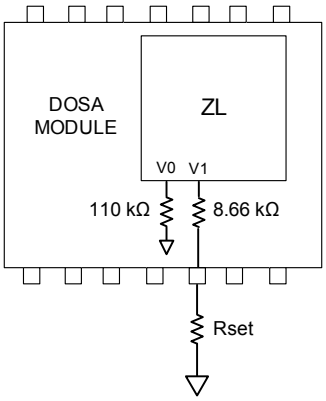


FIGURE 12. R_{SET} on a DOSA Module

The DOSA mode V_{OUT} settings are listed in Table 5.

TABLE 5. DOSA Mode V_{OUT} Settings

V_{OUT} (V)	R_{SET} (kΩ) In series with 8.660kΩ resistor
0.700	162
0.752	113
0.758	100
0.765	90.9
0.772	82.5
0.790	75.0
0.800	57.6
0.821	52.3
0.834	47.5
0.848	43.2
0.880	36.5
0.899	33.2
0.919	30.1
0.965	25.5
0.991	22.6
1.000	21.0
1.100	17.8
1.158	14.7
1.200	13.3
1.250	10.5
1.500	8.87
1.669	6.98
1.800	6.04
2.295	4.32
2.506	3.74
3.300	2.61
5.000	1.50

NOTE: (R0 = 110kΩ, R1 = R_{SET} + 8.66kΩ)

Start-up Procedure

The ZL2008 follows a specific internal start-up procedure after power is applied to the VDD pin. Table 6 describes the start-up sequence.

If the device is to be synchronized to an external clock source, the clock frequency must be stable prior to asserting the EN pin. The device requires approximately 5ms to 10ms to check for specific values stored in its internal memory. If the user has stored values in memory, those values will be loaded. The device will then check the status of all multi-mode pins and load the values associated with the pin settings.

Once this process is completed, the device is ready to accept commands via the I^2C/SMBus interface and the device is ready to be enabled. Once enabled, the device requires approximately 2ms before its output voltage may be allowed to start its ramp-up process. If a soft-start delay period less than 2ms has been configured (using PMBus commands), the device will default to a 2ms delay period. If a delay period greater than 2ms is configured, the device will wait for the configured delay period prior to starting to ramp its output.

After the delay period has expired, the output will begin to ramp towards its target voltage according to the pre-configured soft-start ramp time that has been set using the SS pin. It should be noted that if the EN pin is tied to VDD, the device will still require approx 5ms to 10ms before the output can begin its ramp-up as described in Table 6.

Soft-start Delay and Ramp Times

It may be necessary to set a delay from when an enable signal is received until the output voltage starts to ramp to its target value. In addition, the designer may wish to precisely set the time required for V_{OUT} to ramp to its target value after the delay period has expired. These features may be used as part of an overall inrush current management strategy or to precisely control how fast a load IC is turned on. The ZL2008 gives the system designer several options for precisely and independently controlling both the delay and ramp time periods.

The soft-start delay period begins when the EN pin is asserted and ends when the delay time expires. The soft-start delay period is set using the SS pin. Precise ramp delay timing reduces the delay time variations but is only available when the appropriate bit in the MISC_CONFIG register has been set. Please refer to Application Note AN2033 for details.

The soft-start ramp timer enables a precisely controlled ramp to the nominal V_{OUT} value that begins once the delay period has expired. The ramp-up is guaranteed monotonic and its slope may be precisely set using the SS pin.

The soft-start delay and ramp times can be set to standard values according to Table 7.

TABLE 6. ZL2106 START-UP SEQUENCE

STEP #	STEP NAME	DESCRIPTION	TIME DURATION
1	Power Applied	Input voltage is applied to the ZL2008's VDD pin	Depends on input supply ramp time
2	Internal Memory Check	The device will check for values stored in its internal memory. This step is also performed after a Restore command.	Approx 5ms to 10ms (device will ignore an enable signal or PMBus traffic during this period)
3	Multi-mode Pin Check	The device loads values configured by the multi-mode pins.	
4	Device Ready	The device is ready to accept an enable signal.	-
5	Pre-ramp Delay	The device requires approximately 2ms following an enable signal and prior to ramping its output. Additional pre-ramp delay may be configured using the SS pin.	Approximately 2ms

TABLE 7. Soft-start Pin-strap Settings

SS Pin	Delay Time (ms)	Ramp Time (ms)
LOW	2	2
OPEN	5	5
HIGH	10	10

If the desired soft-start delay and ramp times are not one of the values listed in Table 7, the times can be set to a custom value by connecting a resistor from the SS pin to SGND using the appropriate resistor value from Table 8. The value of this resistor is measured upon start-up or Restore and will not change if the resistor is varied after power has been applied to the ZL2008. See Figure 13 for typical connections using resistors.

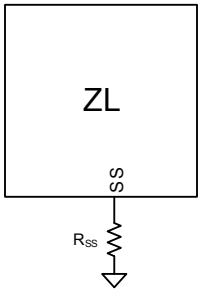


FIGURE 13. SS Pin Resistor Connections

The soft-start delay and ramp times can also be set to custom values via the I²C/SMBus interface. When the SS delay time is set to 0ms, the device will begin its ramp-up after the internal circuitry has initialized (approx. 2ms). When the soft-start ramp period is set to 0ms, the output will ramp up as quickly as the output load capacitance and loop settings will allow. It is generally recommended to set the soft-start ramp to a value greater than 500µs to prevent inadvertent fault conditions due to excessive inrush current.

Power Good

The ZL2008 provides a Power Good (PG) signal that indicates the output voltage is within a specified tolerance of its target level and no fault condition exists. By default, the PG pin will assert if the output is within
-10% of the target voltage. These limits and the polarity of the pin may be changed via the I²C/SMBus interface. See Application Note AN2033 for details.

A PG delay period is defined as the time from when all conditions within the ZL2008 for asserting PG are met to when the PG pin is actually asserted. This feature is commonly used instead of using an external reset controller to control external digital logic. By default, the ZL2008 PG delay is set equal to the soft-start ramp time setting. Therefore, if the soft-start ramp time is set to 10ms, the PG delay will be set to 10ms. The PG delay may be set independently of the soft-start ramp using the I²C/SMBus as described in Application Note AN2033.

TABLE 8. SS Resistor Settings

R_{SS} (kΩ)	Delay Time (ms)	Ramp Time (ms)
10	2	5
11		10
12.1		20
13.3	5	2
14.7		5
16.2		10
17.8		20
19.6	10	2
21.5		5
23.7		10
26.1		20
28.7	15	2
31.6		5
34.8		10
38.3		20
42.2	20	2
46.4		5
51.1		10
56.2		20
61.9	30	2
68.1		5
75		10
82.5		20

Switching Frequency and PLL

The ZL2008 incorporates an internal phase-locked loop (PLL) to clock the internal circuitry. The PLL can be driven by an external clock source connected to the SYNC pin. When using the internal oscillator, the SYNC pin can be configured as a clock source for other Zilker Labs devices.

The SYNC pin is a unique pin that can perform multiple functions depending on how it is configured. The CFG1 pin is used to select the operating mode of the SYNC pin as shown in Table 9. Figure 14 illustrates the typical connections for each mode.

TABLE 9. SYNC Pin Function Selection

CFG1 Pin	SYNC Pin Function
LOW	SYNC is configured as an input
OPEN	Auto Detect mode
HIGH	SYNC is configured as an output f_{SW} = 400kHz

Configuration A: SYNC OUTPUT

When the SYNC pin is configured as an output (CFG1 pin is tied HIGH), the device will run from its internal oscillator and will drive the resulting internal oscillator signal (preset to 400kHz) onto the SYNC pin so other devices can be synchronized to it. The SYNC pin will not be checked for an incoming clock signal while in this mode.

Configuration B: SYNC INPUT

When the SYNC pin is configured as an input (CFG1 pin is tied LOW), the device will automatically check for a clock signal on the SYNC pin each time EN is asserted. The ZL2008's oscillator will then synchronize with the rising edge of the external clock.

The incoming clock signal must be in the range of 200kHz to 1.4MHz and must be stable when the enable pin is asserted. The clock signal must also exhibit the necessary performance requirements (see "Electrical Specifications" on page 4). In the event of a loss of the external clock signal, the output voltage may show transient over/undershoot.

If this happens, the ZL2008 will automatically switch to its internal oscillator and switch at a frequency close to the previous incoming frequency.

Configuration C: SYNC AUTO DETECT

When the SYNC pin is configured in auto detect mode (CFG1 pin is left OPEN), the device will automatically check for a clock signal on the SYNC pin after enable is asserted.

If a clock signal is present, The ZL2008's oscillator will then synchronize the rising edge of the external clock. Refer to SYNC INPUT description.

If no incoming clock signal is present, the ZL2008 will configure the switching frequency according to the state of the SYNC pin as listed in Table 10. In this mode, the ZL2008 will only read the SYNC pin connection during the start-up sequence. Changes to SYNC pin connections will not affect f_{SW} until the power (VDD) is cycled off and on.

TABLE 10. Switching Frequency Pin-strap Setting

SYNC Pin	Frequency
LOW	200kHz
OPEN	400kHz
HIGH	1MHz
Resistor	See Table 11

If the user wishes to run the ZL2008 at a frequency not listed in Table 10, the switching frequency can be set using an external resistor, R_{SYNC}, connected between SYNC and SGND using Table 11.

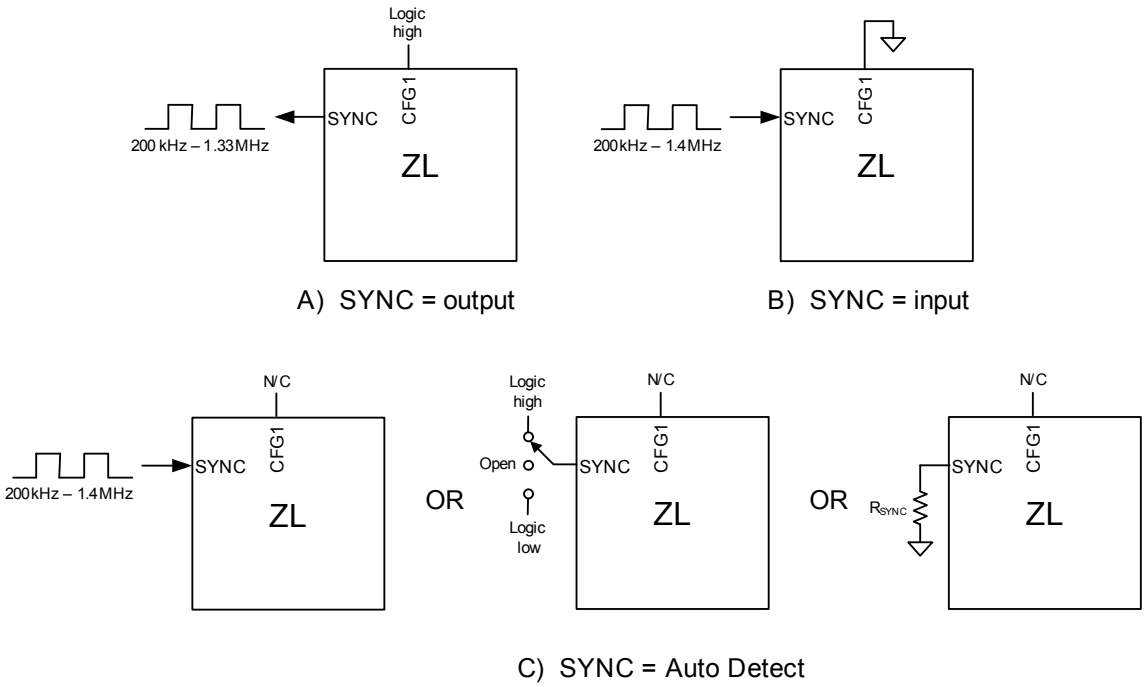


FIGURE 14. Sync Pin Configurations

TABLE 11. Switching Frequency Resistor Settings

R_{SYNC} (kΩ)	f_{SW} (kHz)
10	200
11	222
12.1	242
13.3	267
14.7	296
16.2	320
17.8	364
19.6	400
21.5	421
23.7	471
26.1	533
28.7	571
31.6	615
34.8	727
38.3	800
46.4	889
51.1	1000
56.2	1143
68.1	1333

The switching frequency can also be set to any value between 200kHz and 1.33MHz using the I^2C/SMBus interface. The available frequencies below 1.4MHz are defined by f_{SW} = 8MHz/N, where the whole number N is $6 \leq N \leq 40$. See Application Note AN2033 for details.

If a value other than f_{SW} = 8MHz/N is entered using a PMBus command, the internal circuitry will select the valid switching frequency value that is closest to the entered value. For example, if 810kHz is entered, the device will select 800kHz (N=10).

When multiple Zilker Labs devices are used together, connecting the SYNC pins together will force all devices to synchronize with each other. The CFG1 pin of one device must set its SYNC pin as an output and the remaining devices must have their SYNC pins set as Auto Detect.

Note: The switching frequency read back using the appropriate PMBus command will differ slightly from the selected values in Table 11. The difference is due to hardware quantization.

Power Train Component Selection

The ZL2008 is a synchronous buck converter that uses external MOSFETs, inductor and capacitors to perform the power conversion process. The proper selection of the external components is critical for optimized performance.

To select the appropriate external components for the desired performance goals, the power supply requirements listed in Table 12 must be known.

TABLE 12. Power Supply Requirements

Parameter	Range	Example Value
Input voltage (V_{IN})	3.0V to 14.0V	12V
Output voltage (V_{OUT})	0.6V to 5.0V	1.2V
Output current (I_{OUT})	0A to ~25A	20A
Output voltage ripple (V_{orip})	< 3% of V_{OUT}	1% of V_{OUT}
Output load step (I_{ostep})	< Io	50% of I_o
Output load step rate	—	10A/µs
Output deviation due to load step	—	± 50mV
Maximum PCB temp.	+120°C	+85°C
Desired efficiency	—	85%
Other considerations	Various	Optimize for small size

DESIGN GOAL TRADE-OFFS

The design of the buck power stage requires several compromises among size, efficiency, and cost. The inductor core loss increases with frequency, so there is a trade-off between a small output filter made possible by a higher switching frequency and getting better power supply efficiency. Size can be decreased by increasing the switching frequency at the expense of efficiency. Cost can be minimized by using through-hole inductors and capacitors; however these components are physically large.

To start the design, select a switching frequency based on Table 13. This frequency is a starting point and may be adjusted as the design progresses.

TABLE 13. Circuit Design Consideration

Frequency Range	Efficiency	Circuit Size
200kHz to 400kHz	Highest	Larger
400kHz to 800kHz	Moderate	Smaller
800kHz to 1.4MHz	Lower	Smallest

INDUCTOR SELECTION

The output inductor selection process must include several trade-offs. A high inductance value will result in a low ripple current (I_{opp}), which will reduce output capacitance and produce a low output ripple voltage, but may also compromise output transient load performance. Therefore, a balance must be struck between output ripple and optimal load transient performance. A good starting point is to select the output inductor ripple equal to the expected load transient step magnitude (I_{ostep}):

$$I_{opp} = I_{ostep} \quad \text{(EQ. 4)}$$

Now the output inductance can be calculated using Equation 5, where V_{INM} is the maximum input voltage:

$$L_{OUT} = \frac{V_{OUT} \times \left(1 - \frac{V_{OUT}}{V_{INM}}\right)}{fsw \times I_{opp}} \quad \text{(EQ. 5)}$$

The average inductor current is equal to the maximum output current. The peak inductor current (I_{Lpk}) is calculated using Equation 6 where I_{OUT} is the maximum output current:

$$I_{Lpk} = I_{OUT} + \frac{I_{opp}}{2} \quad \text{(EQ. 6)}$$

Select an inductor rated for the average DC current with a peak current rating above the peak current computed above.

In overcurrent or short-circuit conditions, the inductor may have currents greater than 2X the normal maximum rated output current. It is desirable to use an inductor that still provides some inductance to protect the load and the MOSFETs from damaging currents in this situation.

Once an inductor is selected, the DCR and core losses in the inductor are calculated. Use the DCR specified in the inductor manufacturer's datasheet.

$$P_{LDCR} = DCR \times I_{Lrms}^{2} \quad \text{(EQ. 7)}$$

I_{Lrms} is given by Equation 8:

$$I_{Lrms} = \sqrt{I_{OUT}^{2} + \frac{(I_{opp})^2}{12}} \quad \text{(EQ. 8)}$$

where I_{OUT} is the maximum output current. Next, calculate the core loss of the selected inductor. Since this calculation is specific to each inductor and manufacturer, refer to the chosen inductor datasheet. Add the core loss and the ESR loss and compare the total loss to the maximum power dissipation recommendation in the inductor datasheet.

OUTPUT CAPACITOR SELECTION

Several trade-offs must also be considered when selecting an output capacitor. Low ESR values are needed to have a small output deviation during transient load steps (V_{osag}) and low output voltage ripple (V_{orip}). However, capacitors with low ESR, such as semi-stable (X5R and X7R) dielectric ceramic capacitors, also have relatively low capacitance values. Many designs can use a combination of high capacitance devices and low ESR devices in parallel.

For high ripple currents, a low capacitance value can cause a significant amount of output voltage ripple. Likewise, in high transient load steps, a relatively large amount of capacitance is needed to minimize the output voltage deviation while the inductor current ramps up or down to the new steady state output current value.

As a starting point, apportion one-half of the output ripple voltage to the capacitor ESR and the other half to capacitance, as shown in Equations 9 and 10:

$$C_{OUT} = \frac{I_{opp}}{8 \times f_{sw} \times \frac{V_{orip}}{2}} \quad \text{(EQ. 9)}$$

$$ESR = \frac{V_{orip}}{2 \times I_{opp}} \quad \text{(EQ. 10)}$$

Use these values to make an initial capacitor selection, using a single capacitor or several capacitors in parallel.

After a capacitor has been selected, the resulting output voltage ripple can be calculated using Equation 11:

$$V_{orip} = I_{opp} \times ESR + \frac{I_{opp}}{8 \times f_{sw} \times C_{OUT}} \quad \text{(EQ. 11)}$$

Because each part of this equation was made to be less than or equal to half of the allowed output ripple voltage, the V_{orip} should be less than the desired maximum output ripple.

INPUT CAPACITOR

It is highly recommended that dedicated input capacitors be used in any point-of-load design, even when the supply is powered from a heavily filtered 5V or 12V "bulk" supply from an off-line power supply. This is because of the high RMS ripple current that is drawn by the buck converter topology. This ripple (I_{CINrms}) can be determined from Equation 12:

$$I_{CINrms} = I_{OUT} \times \sqrt{D \times (1 - D)} \quad \text{(EQ. 12)}$$

Without capacitive filtering near the power supply circuit, this current would flow through the supply bus and return planes, coupling noise into other system circuitry. The input capacitors should be rated at 1.2X the ripple current calculated above to avoid overheating of the capacitors due to the high ripple current, which can cause premature failure. Ceramic capacitors with X7R or X5R dielectric with low ESR and 1.1X the maximum expected input voltage are recommended.

BOOTSTRAP CAPACITOR SELECTION

The high-side driver boost circuit utilizes an external Schottky diode (D_B) and an external bootstrap capacitor (C_B) to supply sufficient gate drive for the high-side MOSFET driver. D_B should be a 20mA, 30V Schottky diode or equivalent device and C_B should be a 1µF ceramic type rated for at least 6.3V.

QL SELECTION

The bottom MOSFET should be selected primarily based on the device's $R_{DS(ON)}$ and secondarily based on its gate charge. To choose QL, use the following equation and allow 2% to 5% of the output power to be dissipated in the $R_{DS(ON)}$ of QL (lower output voltages and higher step-down ratios will be closer to 5%):

Calculate the RMS current in QL as follows:

$$P_{QL} = 0.05 \times V_{OUT} \times I_{OUT} \quad \text{(EQ. 13)}$$

$$I_{botrms} = I_{Lrms} \times \sqrt{1-D} \quad \text{(EQ. 14)}$$

Calculate the desired maximum $R_{DS(ON)}$ as follows:

$$R_{DS(ON)} = \frac{P_{QL}}{(I_{botrms})^2} \quad \text{(EQ. 15)}$$

Note that the $R_{DS(ON)}$ given in the manufacturer's datasheet is measured at +25°C. The actual $R_{DS(ON)}$ in the end-use application will be much higher. For example, a Vishay Si7114 MOSFET with a junction temperature of +125°C has an $R_{DS(ON)}$ that is 1.4 times higher than the value at +25°C. Select a candidate MOSFET, and calculate the required gate drive current as follows:

$$I_g = f_{SW} \times Q_g \quad \text{(EQ. 16)}$$

Keep in mind that the total allowed gate drive current for both QH and QL is 80mA.

MOSFETs with lower $R_{DS(ON)}$ tend to have higher gate charge requirements, which increases the current and resulting power required to turn them on and off. Since the MOSFET gate drive circuits are integrated in the ZL2008, this power is dissipated in the ZL2008 according to Equation 17:

$$P_{QL} = f_{sw} \times Q_g \times V_{INM} \quad \text{(EQ. 17)}$$

QH SELECTION

In addition to the $R_{DS(ON)}$ loss and gate charge loss, QH also has switching loss. The procedure to select QH is similar to the procedure for QL. First, assign 2% to 5% of the output power to be dissipated in the $R_{DS(ON)}$ of QH using the equation for QL above. As was done with QL, calculate the RMS current as follows:

$$I_{toprms} = I_{Lrms} \times \sqrt{D} \quad \text{(EQ. 18)}$$

Calculate a starting $R_{DS(ON)}$ as follows, in this example using 5%:

$$P_{QH} = 0.05 \times V_{OUT} \times I_{OUT} \quad \text{(EQ. 19)}$$

$$R_{DS(ON)} = \frac{P_{QH}}{(I_{toprms})^2} \quad \text{(EQ. 20)}$$

Select a MOSFET and calculate the resulting gate drive current. Verify that the combined gate drive current from QL and QH does not exceed 80mA.

Next, calculate the switching time using:

$$t_{SW} = \frac{Q_g}{I_{gdr}} \quad \text{(EQ. 21)}$$

where Q_g is the gate charge of the selected QH and I_{gdr} is the peak gate drive current available from the ZL2008.

Although the ZL2008 has a typical gate drive current of 3A, use the minimum guaranteed current of 2A for a conservative design. Using the calculated switching time, calculate the switching power loss in QH using:

$$P_{swtop} = V_{INM} \times t_{sw} \times I_{OUT} \times f_{sw} \quad \text{(EQ. 22)}$$

The total power dissipated by QH is given by Equation 23:

$$P_{QHtot} = P_{QH} + P_{swtop} \quad \text{(EQ. 23)}$$

MOSFET THERMAL CHECK

Once the power dissipations for QH and QL have been calculated, the MOSFETs junction temperature can be estimated. Using the junction-to-case thermal resistance (R_{th}) given in the MOSFET manufacturer's datasheet and the expected maximum printed circuit board temperature, calculate the junction temperature as follows:

$$T_{j\max} = T_{pcb} + (P_Q \times R_{th}) \quad \text{(EQ. 24)}$$

CURRENT SENSING COMPONENTS

Once the current sense method has been selected (refer to section "Current Limit Threshold Selection" on page 21), the components are selected as follows.

When using the inductor DCR sensing method, the user must also select an R/C network comprised of R1 and CL (see Figure 15).

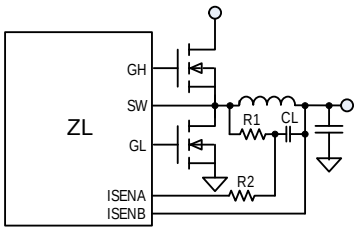


FIGURE 15. DCR Current Sensing

For the voltage across C_L to reflect the voltage across the DCR of the inductor, the time constant of the inductor must match the time constant of the RC network. That is:

$$\tau_{RC} = \tau_{L/DCR}$$
$$R_1 \cdot C_L = \frac{L}{DCR} \quad \text{(EQ. 25)}$$

For *L*, use the average of the nominal value and the minimum value. Include the effects of tolerance, DC Bias and switching frequency on the inductance when determining the minimum value of *L*. Use the typical value for *DCR*.

The value of R_1 should be as small as feasible and no greater than 5kΩ for best signal-to-noise ratio. The designer should make sure the resistor package size is appropriate for the power dissipated and include this loss in efficiency calculations. In calculating the minimum value of R_1, the average voltage across

C_L (which is the average $I_{OUT}DCR$ product) is small and can be neglected. Therefore, the minimum value of R_1 may be approximated Equation 26:,

$$R_{1-\min} = \frac{D\left(V_{IN-\max} - V_{OUT}\right)^2 + \left(1-D\right)\cdot V_{OUT}{}^2}{P_{R1\,pkg-\max}\cdot \delta_P} \quad \text{(EQ. 26)}$$

where $P_{R1pkg\text{-}max}$ is the maximum power dissipation specification for the resistor package and $_P$ is the derating factor for the same parameter (eg.: $P_{R1pkg\text{-}max}$ = 0.0625W for 0603 package, $_P$ = 50% @ 85°C). Once $R_{1\text{-}min}$ has been calculated, solve for the maximum value of C_L from Equation 27:

$$C_{L-\max} = \frac{L}{R_{1-\min}\cdot DCR} \quad \text{(EQ. 27)}$$

and choose the next-lowest readily available value (e.g.: For $C_{L\text{-}max}$ = 1.86µF, C_L = 1.5µF is a good choice). Then substitute the chosen value into the same equation and re-calculate the value of R_1. Choose the 1% resistor standard value closest to this re-calculated value of R_1. The error due to the mismatch of the two time constants is expressed in Equation 28:

$$\varepsilon_\tau = \left(1 - \frac{R_1\cdot C_L\cdot DCR}{L_{avg}}\right)\cdot 100\% \quad \text{(EQ. 28)}$$

The value of R_2 should be simply five times that of R_1:

$$R_2 = 5\cdot R_1 \quad \text{(EQ. 29)}$$

For the $R_{DS(ON)}$ current sensing method, the external low side MOSFET will act as the sensing element as indicated in Figure 16.

Current Limit Threshold Selection

It is recommended that the user include a current limiting mechanism in their design to protect the power supply from damage and prevent excessive current from being drawn from the input supply in the event that the output is shorted to ground or an overload condition is imposed on the output. Current limiting is accomplished by sensing the current through the circuit during a portion of the duty cycle.

Output current sensing can be accomplished by measuring the voltage across a series resistive sensing element according to Equation 30:

$$V_{LIM} = I_{LIM}\times R_{SENSE} \quad \text{(EQ. 30)}$$

Where:

I_{LIM} is the desired maximum current that should flow in the circuit.

R_{SENSE} is the resistance of the sensing element.

V_{LIM} is the voltage across the sensing element at the point the circuit should start limiting the output current.

The ZL2008 supports “lossless” current sensing by measuring the voltage across a resistive element that is already present in the circuit. This eliminates additional efficiency losses incurred by devices that must use an additional series resistance in the circuit.

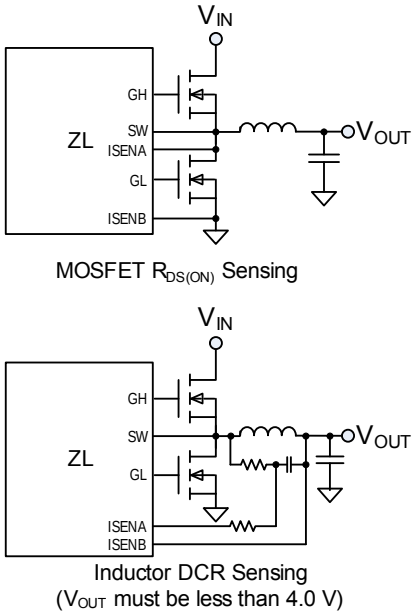


FIGURE 16. Current Sensing Methods

To set the current limit threshold, the user must first select a current sensing method. The ZL2008 incorporates two methods for current sensing, synchronous MOSFET $R_{DS(ON)}$ sensing and inductor DC resistance (DCR) sensing; Figure 16 shows a simplified schematic for each method. The current sensing method can be selected using the CFG2 pin, as shown in Tables 26 and 28, or via the I^2C/SMBus interface. Please refer to Application Note AN2033 for details.

In addition to selecting the current sensing method, the ZL2008 gives the power supply designer several choices for the fault response during over or under current condition. The user can select the number of violations allowed before declaring fault, a blanking time and the action taken when a fault is detected.

The blanking time represents the time when no current measurement is taken. This is to avoid taking a reading just after a switching transition (less accurate due to potential ringing). It is a configurable parameter.

Once the sensing method has been selected, the user must select the voltage threshold (VLIM), the desired current limit threshold, and the resistance of the sensing element.

The current limit threshold voltage can be selected by simply connecting the ILIM pin as shown in Table 14. The ground-referenced sensing method is being used in this mode. By default, the IOUT_CAL_GAIN is set to 1mΩ for DCR mode and 2mΩ for RDS mode.

TABLE 14. Current Limit Threshold Voltage Pin-strap Settings

ILIM Pin	R_{DS} V_{LIM} (mV)	DCR V_{LIM} (mV)
LOW	50	25
OPEN	60	30
HIGH	70	35

TABLE 15. Current Limit Threshold Voltage Resistor Settings

R_{LIM} (kΩ)	R_{DS} V_{LIM} (mV)	DCR V_{LIM} (mV)
10	0	0
11	5	2.5
12.1	10	5
13.3	15	7.5
14.7	20	10
16.2	25	12.5
17.8	30	15
19.6	35	17.5
21.5	40	20
23.7	45	22.5
26.1	50	25
28.7	55	27.5
31.6	60	30
34.8	65	32.5
38.3	70	35
42.2	75	37.5
46.4	80	40
51.1	85	42.5
56.2	90	45
61.9	95	47.5
68.1	100	50
75	105	52.5
82.5	110	55
90.9	115	57.5
100	120	60

The threshold voltage can also be selected in 5mV increments by connecting a resistor, R_{LIM}, between the ILIM pin and ground according to Table 15. This method is preferred if the user does not desire to use or does not have access to the I²C/SMBus interface and the desired threshold value is contained in Table 15.

The current limit threshold can also be set to a custom value via the I²C/SMBus interface. Please refer to Application Note AN2033 for further details.

Loop Compensation

The ZL2008 operates as a voltage-mode synchronous buck controller with a fixed frequency PWM scheme. Although the ZL2008 uses a digital control loop, it operates much like a traditional analog PWM controller. Figure 17 is a simplified block diagram of the ZL2008 control loop, which differs from an analog control loop only by the constants in the PWM and compensation blocks. As in the analog controller case, the compensation block compares the output voltage to the desired voltage reference and compensation zeroes are added to keep the loop stable. The resulting integrated error signal is used to drive the PWM logic, converting the error signal to a duty cycle to drive the external MOSFETs.

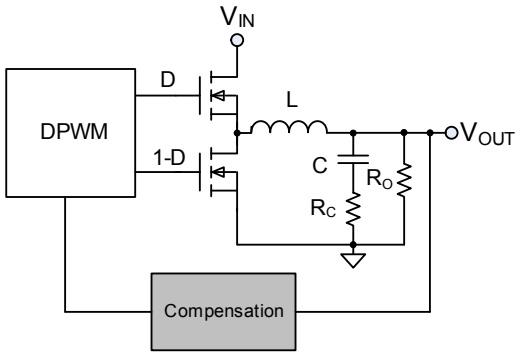


FIGURE 17. Control Loop Block Diagram

In the ZL2008, the compensation zeros and gain are set by configuring the FC0 and FC1 pins or via the I²C/SMBus interface once the user has calculated the required settings. This method eliminates the inaccuracies due to the component tolerances associated with using external resistors and capacitors required with traditional analog controllers.

The compensation is configured using a baseline set of PID taps which are scaled on the factors of Gain, Q and Fn as shown in Tables 16, 17 and 18. The parameters Gain, Q and Fn are defined in AN2035 and are parameters of the compensator (not the power stage being compensated).

The selection of these scaling factors is based on compensation required for additional output capacitance used in an application.

TABLE 16. FC0 Pin-strap Settings

FC0 Pin	Gain Scale (dB)	Q-new/Q-base
LOW	-12	1
OPEN	0	
HIGH	6	

TABLE 17. FC1 Pin-strap Settings

FC1 Pin	Fn-new/Fn-base
LOW	1
OPEN	
HIGH	

The scaling factors are applied to the baseline set of taps to achieve the desired compensation results. These baseline taps correspond to zeroes of the form:

$$G_{base}\left[1+\frac{s}{(Q_{base}*2\pi f_{nbase})}+\left(\frac{s}{(Q_{base}*2\pi f_{nbase})}\right)^2\right] \quad \text{(EQ. 31)}$$

Where G_{base} = 20dB

Q_{base} = 2

$f_{nbase} = f_{SW}/10$

Both the baseline taps and the calculated taps determined by the FC0 and FC1 resistors can be read via the I²C/SMBus interface. Please refer to Application Note AN2033 for further details.

TABLE 18. Loop Compensation Resistor Settings

R_{FC0} (kΩ)	Gain Scale (dB)	Q-new/Q-base	R_{FC1} (kΩ)	Fn-new/Fn-base
10	12	0.6813	10	1.0000
11		0.4642	11	0.9050
12.1		0.3162	12.1	0.8190
13.3		0.2154	13.3	0.7411
14.7		0.1468	14.7	0.6707
16.2		0.1000	16.2	0.6070
17.8	6	0.6813	17.8	0.5493
19.6		0.4642	19.6	0.4971
21.5		0.3162	21.5	0.4498
23.7		0.2154	23.7	0.4071
26.1		0.1468	26.1	0.3684
28.7		0.1000	28.7	0.3334
31.6	0	0.6813	31.6	0.3017
34.8		0.4642	34.8	0.2730
38.3		0.3162	38.3	0.2471
42.2		0.2154	42.2	0.2236
46.4		0.1468	46.4	0.2024
51.1		0.1000	51.1	0.1831
56.2	-6	1.0000	56.2	0.1657
61.9		0.6813	61.9	0.1500
68.1		0.4642	68.1	0.1357
75		0.3162	75	0.1228
82.5		0.2154	82.5	0.1112
90.9		0.1468	90.9	0.1006
100		0.1000	100	0.0910
110	-12	0.6813	110	0.0824
121		0.4642	121	0.0745
133		0.3162	133	0.0675
147		0.2154	147	0.0611
162		0.1468	162	0.0553
178		0.1000	178	0.0500

Non-linear Response (NLR) Settings

The ZL2008 incorporates a non-linear response (NLR) loop that decreases the response time and the output voltage deviation in the event of a sudden output load current step. The NLR loop incorporates a secondary error signal processing path that bypasses the primary error loop when the output begins to transition outside of the standard regulation limits. This scheme results in a higher equivalent loop bandwidth than what is possible using a traditional linear loop.

When a load current step function imposed on the output causes the output voltage to drop below the lower regulation limit, the NLR circuitry will force a positive correction signal that will turn on the upper MOSFET and quickly force the output to increase. Conversely, a negative load step (i.e. removing a large load current) will cause the NLR circuitry to force a negative correction signal that will turn on the lower MOSFET and quickly force the output to decrease.

NLR can be configured using resistor pin-straps as follows:

CFG0 disables NLR or enables NLR inner thresholds to 1.5%, 2% or 3% (see Table 30).

CFG1 sets NLR inner thresholds timeout and blanking to 1 and 4 or 2 and 8 (see Table 27).

Please refer to Application Note AN2032 for more details regarding NLR settings.

Efficiency Optimized Driver Dead-time Control

The ZL2008 utilizes a closed loop algorithm to optimize the dead-time applied between the gate drive signals for the top and bottom FETs. In a synchronous buck converter, the MOSFET drive circuitry must be designed such that the top and bottom MOSFETs are never in the conducting state at the same time. Potentially damaging currents flow in the circuit if both top and bottom MOSFETs are simultaneously on for periods of time exceeding a few nanoseconds. Conversely, long periods of time in which both MOSFETs are off reduce overall circuit efficiency by allowing current to flow in their parasitic body diodes.

It is therefore advantageous to minimize this dead-time to provide optimum circuit efficiency. In the first order model of a buck converter, the duty cycle is determined by Equation 32:

$$D \approx \frac{V_{OUT}}{V_{IN}} \quad \text{(EQ. 32)}$$

However, non-idealities exist that cause the real duty cycle to extend beyond the ideal. Dead-time is one of those non-idealities that can be manipulated to improve efficiency. The ZL2008 has an internal algorithm that constantly adjusts dead-time non-overlap to minimize duty cycle, thus maximizing efficiency. This circuit will null out dead-time differences due to component variation, temperature, and loading effects.

This algorithm is independent of application circuit parameters such as MOSFET type, gate driver delays, rise and fall times and circuit layout. In addition, it does not require drive or MOSFET voltage or current waveform measurements.

Adaptive Diode Emulation

Most power converters use synchronous rectification to optimize efficiency over a wide range of input and output conditions. However, at light loads the synchronous MOSFET will typically sink current and introduce additional energy losses associated with higher peak inductor currents, resulting in reduced efficiency. Adaptive diode emulation mode turns off the low-side FET gate drive at low load currents to prevent the inductor current from going negative, reducing the energy losses and increasing overall efficiency. Diode emulation is available to single-phase devices only.

Note: the overall bandwidth of the device may be reduced when in diode emulation mode. It is recommended that diode emulation is disabled prior to applying significant load steps.

Adaptive Frequency Control

Since switching losses contribute to the efficiency of the power converter, reducing the switching frequency will reduce the switching losses and increase efficiency. The ZL2008 includes Adaptive Frequency Control mode, which effectively reduces the observed switching frequency as the load decreases.

Adaptive frequency mode is enabled by setting bit 0 of MISC_CONFIG to 1 and is only available while the device is operating within Adaptive Diode Emulation Mode. As the load current is decreased, diode emulation mode decreases the GL on-time to prevent negative inductor current from flowing. As the load is decreased further, the GH pulse width will begin to decrease while maintaining the programmed frequency, f_{PROG} (set by the FREQ_SWITCH command).

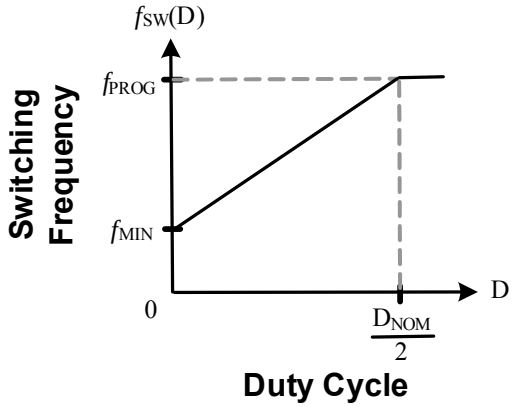


FIGURE 18. Adaptive Frequency

Once the GH pulse width (D) reaches 50% of the nominal duty cycle, D_{NOM} (determined by Vin and Vout), the switching frequency will start to decrease according to Equation 33:

If

$$\frac{D_{NOM}}{2}$$

then,

$$\left(\frac{2(f_{SW} - f_{MIN})}{D_{NOM}}\right)D + f_{MIN} \quad \text{(EQ. 33)}$$

Otherwise $f_{SW}(D) = f_{PROG}$

This is illustrated in Figure 18. Due to quantizing effects inside the IC, the ZL2008 will decrease its frequency in steps between f_{SW} and f_{MIN}. The quantity and magnitude of the steps will depend on the difference between f_{SW} and f_{MIN} as well as the frequency range.

Adaptive frequency mode is not available for current sharing groups when using an external clock, or if the device is outputting a clock signal on its SYNC pin.

Power Management Functional Description

Input Undervoltage Lockout

The input undervoltage lockout (UVLO) prevents the ZL2008 from operating when the input falls below a preset threshold, indicating the input supply is out of its specified range. The UVLO threshold (V_{UVLO}) can be set between 2.85V and 16V using the UVLO pin. The simplest implementation is to connect the UVLO pin as shown in Table 19. If the UVLO pin is left unconnected, the UVLO threshold will default to 4.5V.

TABLE 19. UVLO Threshold Pin-strap Settings

UVLO Pin	UVLO Threshold (V)
LOW	3
OPEN	4.5
HIGH	10.8

If the desired UVLO threshold is not one of the listed choices, the user can configure a threshold between 2.85V and 16V by connecting a resistor between the UVLO pin and SGND by selecting the appropriate resistor from Table 20.

TABLE 20. UVLO Threshold Resistor Settings

R_{UVLO} (kΩ)	UVLO (V)
17.8	2.85
19.6	3.14
21.5	3.44
23.7	3.79
26.1	4.18
28.7	4.59
31.6	5.06
34.8	5.57
38.3	6.13
42.2	6.75
46.4	7.42
51.1	8.18
56.2	8.99
61.9	9.9
68.1	10.9
75	12
82.5	13.2
90.9	14.54
100	16

The UVLO voltage can also be set to any value between 2.85V and 16V via the I^2C/SMBus interface.

Once an input undervoltage fault condition occurs, the device can respond in a number of ways as follows:

1. Continue operating without interruption.
2. Continue operating for a given delay period, followed by shutdown if the fault still exists. The device will remain in shutdown until instructed to restart.
3. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.

The default response from a UVLO fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition. If the fault condition is no longer present, the ZL2008 will be re-enabled.

Please refer to Application Note AN2033 for details on how to configure the UVLO threshold or to select specific UVLO fault response options via the I^2C/SMBus interface.

Output Overvoltage Protection

The ZL2008 offers an internal output overvoltage protection circuit that can be used to protect sensitive load circuitry from being subjected to a voltage higher than its prescribed limits. A hardware comparator is used to compare the actual output voltage (seen at the VSEN pin) to a threshold set to 15% higher than the target output voltage (the default setting). If the VSEN voltage exceeds this threshold, the PG pin will de-assert and the device can then respond in a number of ways as follows:

1. Initiate an immediate shutdown until the fault has been cleared. The user can select a specific number of retry attempts.
2. Turn off the high-side MOSFET and turn on the low-side MOSFET. The low-side MOSFET remains ON until the device attempts a restart.

The default response from an overvoltage fault is to immediately shut down. The device will continuously check for the presence of the fault condition, and when the fault condition no longer exists the device will be re-enabled.

For continuous overvoltage protection when operating from an external clock, the only allowed response is an immediate shutdown.

Please refer to Application Note AN2033 for details on how to select specific overvoltage fault response options via I^2C/SMBus.

Output Pre-Bias Protection

An output pre-bias condition exists when an externally applied voltage is present on a power supply's output before the power supply's control IC is enabled. Certain applications require that the converter not be allowed to sink current during start up if a pre-bias condition exists at the output. The ZL2008 provides pre-bias protection by sampling the output voltage prior to initiating an output ramp.

If a pre-bias voltage lower than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled. The output voltage is then ramped to the final regulation value at the ramp rate set by the SS pin.

The actual time the output will take to ramp from the pre-bias voltage to the target voltage will vary depending on the pre-bias voltage but the total time elapsed from when the delay period expires and when the output reaches its target value will match the pre-configured ramp time. See Figure 19.

If a pre-bias voltage higher than the target voltage exists after the pre-configured delay period has expired, the target voltage is set to match the existing pre-bias voltage and both drivers are enabled with a PWM duty cycle that would ideally create the pre-bias voltage.

Once the pre-configured soft-start ramp period has expired, the PG pin will be asserted (assuming the pre-bias voltage is not higher than the overvoltage limit). The PWM will then adjust its duty cycle to match the original target voltage and the output will ramp down to the pre-configured output voltage.

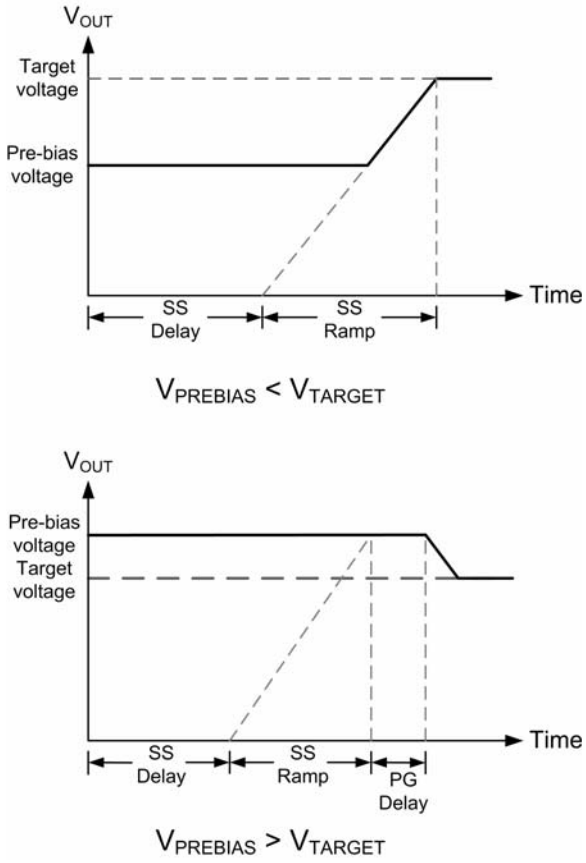


FIGURE 19. Output Responses to Pre-bias Voltages

If a pre-bias voltage higher than the overvoltage limit exists, the device will not initiate a turn-on sequence and will declare an overvoltage fault condition to exist. In this case, the device will respond based on the output overvoltage fault response method that has been selected. See "Output Overvoltage Protection" on page 26 for response options due to an overvoltage condition.

Pre-bias protection is not offered for current sharing groups that also have tracking enabled.

Output Overcurrent Protection

The ZL2008 can protect the power supply from damage if the output is shorted to ground or if an overload condition is imposed on the output. Once the current limit threshold has been selected (see "Current Limit Threshold Selection" on page 21), the user may determine the desired course of action in response to the fault condition. The following overcurrent protection response options are available:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.

4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

The default response from an overcurrent fault is an immediate shutdown of the device. The device will continuously check for the presence of the fault condition, and if the fault condition no longer exists the device will be re-enabled.

Please refer to Application Note AN2033 for details on how to select specific overcurrent fault response options via I^2C/SMBus.

Thermal Overload Protection

The ZL2008 includes an on-chip thermal sensor that continuously measures the internal temperature of the die and shuts down the device when the temperature exceeds the preset limit. The default temperature limit is set to +125°C in the factory, but the user may set the limit to a different value if desired. See Application Note AN2033 for details. Note that setting a higher thermal limit via the I^2C/SMBus interface may result in permanent damage to the device. Once the device has been disabled due to an internal temperature fault, the user may select one of several fault response options as follows:

1. Initiate a shutdown and attempt to restart an infinite number of times with a preset delay period between attempts.
2. Initiate a shutdown and attempt to restart a preset number of times with a preset delay period between attempts.
3. Continue operating for a given delay period, followed by shutdown if the fault still exists.
4. Continue operating through the fault (this could result in permanent damage to the power supply).
5. Initiate an immediate shutdown.

If the user has configured the device to restart, the device will wait the preset delay period (if configured to do so) and will then check the device temperature. If the temperature has dropped below a threshold that is approx +15°C lower than the selected temperature fault limit, the device will attempt to re-start. If the temperature still exceeds the fault limit the device will wait the preset delay period and retry again.

The default response from a temperature fault is an immediate shutdown of the device. The device will continuously check for the fault condition, and once the fault has cleared the ZL2008 will be re-enabled.

Please refer to Application Note AN2033 for details on how to select specific temperature fault response options via I^2C/SMBus.

Voltage Tracking

Numerous high performance systems place stringent demands on the order in which the power supply voltages are turned on. This is particularly true when powering FPGAs, ASICs, and other advanced processor devices that require multiple supply voltages to power a single die. In most cases, the I/O interface operates at a higher voltage than the core and therefore the core supply voltage must not exceed the I/O supply voltage according to the manufacturers' specifications.

Voltage tracking protects these sensitive ICs by limiting the differential voltage between multiple power supplies during the power-up and power down sequence. The ZL2008 integrates a lossless tracking scheme that allows its output to track a voltage that is applied to the VTRK pin with no external components required. The VTRK pin is an analog input that, when tracking mode is enabled, configures the voltage applied to the VTRK pin to act as a reference for the device's output regulation.

The ZL2008 offers two mode of tracking as follows:

1. *Coincident*. This mode configures the ZL2008 to ramp its output voltage at the same rate as the voltage applied to the VTRK pin.
2. *Ratiometric*. This mode configures the ZL2008 to ramp its output voltage at a rate that is a percentage of the voltage applied to the VTRK pin. The default setting is 50%, but an external resistor string may be used to configure a different tracking ratio.

Figure 20 illustrates the typical connection and the two tracking modes.

The master ZL2008 device in a tracking group is defined as the device that has the highest target output voltage within the group. This master device will control the ramp rate of all tracking devices and is not configured for tracking mode. A delay of at least 10ms must be configured into the master device using the SS pin, and the user may also configure a specific ramp rate using the SS pin. Any device that is configured for tracking mode will ignore its soft-start delay and ramp time settings (SS pin) and its output will take on the turn-on/turn-off characteristics of the reference voltage present at the VTRK pin. All of the ENABLE pins in the tracking group must be connected together and driven by a single logic source. Tracking is configured via the I^2C/SMBus interface by using the TRACK_CONFIG PMBus command. Please refer to Application Note AN2033 for more information on configuring tracking mode using PMBus.

TABLE 21. Tracking Resistor Settings

R_{SS} (kΩ)	Track Ratio (%)	Upper Track Limit	Ramp-up/down Behavior
90.9	100	Limited by target	Output does not decrease before PG
100			Output always follows VTRK
110		Limited by VTRK	Output does not decrease before PG
121			Output always follows VTRK
133	50	Limited by target	Output does not decrease before PG
147			Output always follows VTRK
162		Limited by VTRK	Output does not decrease before PG
178			Output always follows VTRK

It should be noted that current sharing groups that are also configured to track another voltage do not offer pre-bias protection; a minimum load should therefore be enforced to avoid the output voltage from being held up by an outside force. Additionally, a device set up for tracking must have both Alternate Ramp Control and Precise Ramp-Up Delay disabled.

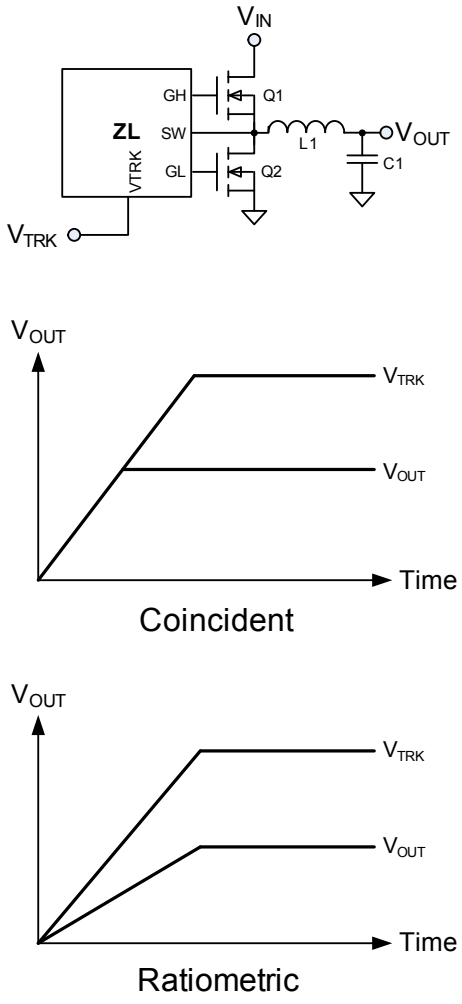


FIGURE 20. Tracking Modes

Voltage Margining

The ZL2008 offers a simple means to vary its output higher or lower than its nominal voltage setting in order to determine whether the load device is capable of operating over its specified supply voltage range. The MGN command is set by driving the MGN pin or through the I²C/SMBus interface. The MGN pin is a tri-level input that is continuously monitored and can be driven directly by a processor I/O pin or other logic-level output.

The ZL2008's output will be forced higher than its nominal set point when the MGN command is set HIGH, and the output will be forced lower than its nominal set point when the MGN command is set LOW. Default margin limits of V_{NOM} ±5% are pre-loaded in the factory, but the margin limits can be modified through the I²C/SMBus interface to as high as V_{NOM} + 10% or as low as 0V, where V_{NOM} is the nominal output voltage set point determined by the V0 and V1 pins. A safety feature prevents the user from configuring the output voltage to exceed V_{NOM} + 10% under any conditions.

The margin limits and the MGN command can both be set individually through the I²C/SMBus interface. Additionally, the transition rate between the nominal output voltage and either margin limit can be configured through the I²C interface. Please refer to Application Note AN2033 for detailed instructions on modifying the margining configurations.

I²C/SMBus Communications

The ZL2008 provides an I²C/SMBus digital interface that enables the user to configure all aspects of the device operation as well as monitor the input and output parameters. The ZL2008 can be used with any standard 2-wire I²C host device. In addition, the device is compatible with SMBus version 2.0 and includes an SALRT line to help mitigate bandwidth limitations related to continuous fault monitoring. Pull-up resistors are required on the I²C/SMBus as specified in the SMBus 2.0 specification. The ZL2008 accepts most standard PMBus commands. When controlling the device with PMBus commands, it is recommended that the enable pin is tied to SGND.

I²C/SMBus Device Address Selection

When communicating with multiple SMBus devices using the I²C/SMBus interface, each device must have its own unique address so the host can distinguish between the devices. The device address can be set according to the pin-strap options listed in Table 22. Address values are right-justified.

TABLE 22. SMBus Address Pin-strap Selection

		SA0		
		LOW	OPEN	HIGH
SA1	LOW	0x20	0x21	0x22
	OPEN	0x23	0x24	0x25
	HIGH	0x26	0x27	Reserved

If additional device addresses are required, a resistor can be connected to the SA0 pin according to Table 23 to provide up to 25 unique device addresses. In this case, the SA1 pin should be tied to SGND.

TABLE 23. SMBus Address Resistor Selection

R_{SA0} (kΩ)	SMBus Address
10	0x00
11	0x01
12.1	0x02
13.3	0x03
14.7	0x04
16.2	0x05
17.8	0x06
19.6	0x07
21.5	0x08
23.7	0x09
26.1	0x0A
28.7	0x0B
31.6	0x0C
34.8	0x0D
38.3	0x0E
42.2	0x0F
46.4	0x10
51.1	0x11
56.2	0x12
61.9	0x13
68.1	0x14
75	0x15
82.5	0x16
90.9	0x17
100	0x18

If more than 25 unique device addresses are required or if other SMBus address values are desired, both the SA0 and SA1 pins can be configured with a resistor to SGND according to Equation 34 and Table 24.

$$SMBus\ address = 25 \times (SA1\ index) + (SA0\ index)\ (in\ decimal) \quad \text{(EQ. 34)}$$

TABLE 24. SMBus Address Index Values

R_{SA} (kΩ)	SA0 or SA1 Index
10	0
11	1
12.1	2
13.3	3
14.7	4
16.2	5
17.8	6
19.6	7
21.5	8
23.7	9
26.1	10
28.7	11
31.6	12
34.8	13
38.3	14
42.2	15
46.4	16
51.1	17
56.2	18
61.9	19
68.1	20
75	21
82.5	22
90.9	23
100	24

Using this method, the user can theoretically configure up to 625 unique SMBus addresses, however the SMBus is inherently limited to 128 devices so attempting to configure an address higher than 128 (0x80) will cause the device address to repeat (i.e., attempting to configure a device address of 129 (0x81) would result in a device address of 1). Therefore, the user should use index values 0-4 on the SA1 pin and the full range of index values on the SA0 pin, which will provide 125 device address combinations.

Note that the SMBus address 0x4B is reserved for device test and cannot be used in the system.

Digital-DC Bus

The Digital-DC Communications (DDC) bus is used to communicate between Zilker Labs Digital-DC devices. This dedicated bus provides the communication channel between devices for features such as sequencing, fault spreading, and current sharing. The DDC pin on all Digital-DC devices in an application should be connected together. A pull-up resistor is required on the DDC bus in order to guarantee the rise time as follows:

$$Rise\ time = R_{PU} * C_{LOAD}\ \ 1\mu s \qquad \text{(EQ. 35)}$$

where R_{PU} is the DDC bus pull-up resistance and C_{LOAD} is the bus loading. The pull-up resistor may be tied to VR or to an external 3.3V or 5V supply as long as this voltage is present prior to or during device power-up. As rules of thumb, each device connected to the DDC bus presents approx 10pF of capacitive loading, and each inch of FR4 PCB trace introduces approx 2pF. The ideal design will use a central pull-up resistor that is well-matched to the total load capacitance. In power module applications, the user should consider whether to place the pull-up resistor on the module or on the PCB of the end application. The minimum pull-up resistance should be limited to a value that enables any device to assert the bus to a voltage that will ensure a logic 0 (typically 0.8V at the device monitoring point) given the pull-up voltage (5V if tied to VR) and the pull-down current capability of the ZL2008 (nominally 4mA).

Phase Spreading

When multiple point of load converters share a common DC input supply, it is desirable to adjust the clock phase offset of each device such that not all devices start to switch simultaneously. Setting each converter to start its switching cycle at a different point in time can dramatically reduce input capacitance requirements and efficiency losses. Since the peak current drawn from the input supply is effectively spread out over a period of time, the peak current drawn at any given moment is reduced and the power losses proportional to the I_{RMS}^2 are reduced dramatically.

In order to enable phase spreading, all converters must be synchronized to the same switching clock. The CFG1 pin is used to set the configuration of the SYNC pin for each device as described in section “Switching Frequency and PLL” on page 17 .

The phase offset of each single-phase device may be set to any value between 0° and 337.5° in 22.5° increments using the CFG2 pin as shown in Tables 25 and 26.

TABLE 25. Phase Offset Pin-strap Settings

R_{CFG2}	Phase Offset (°)	Current Sense
LOW	90	DCR
OPEN	0	
HIGH	180	

TABLE 26. Phase Offset Resistor Settings

R_{CFG2} (kΩ)	Phase Offset (°)	Current Sense
10	22.5	DCR
11	45	
12.1	67.5	
13.3	90	
14.7	112.5	
16.2	135	
17.8	157.5	
19.6	180	
21.5	202.5	
23.7	225	
26.1	247.5	
28.7	270	
31.6	292.5	
34.8	315	
38.3	337.5	
42.2	22.5	RDS
46.4	45	
51.1	67.5	
56.2	90	
61.9	112.5	
68.1	135	
75	157.5	
82.5	180	
90.9	202.5	
100	225	
110	247.5	
121	270	
133	292.5	
147	315	
162	337.5	

The phase offset of (multi-phase) current sharing devices is automatically set to a value between 0° and 337.5° in 22.5° increments as described in “Active Current Sharing” on page 31.

The phase offset of each device may also be set to any value between 0° and 360° in 22.5° increments via the I^2C/SMBus interface. Refer to Application Note AN2033 for further details.

Output Sequencing

A group of Digital-DC devices may be configured to power up in a predetermined sequence. This feature is especially useful when powering advanced processors, FPGAs, and ASICs that require one supply to reach its operating voltage prior to another supply reaching its operating voltage in order to avoid latch-up from occurring. Multi-device sequencing can be achieved by configuring each device through the I^2C/SMBus interface or by using Zilker Labs patented autonomous sequencing mode.

Autonomous sequencing mode configures sequencing by using events transmitted between devices over the DDC bus. This mode is not available on current sharing rails.

The sequencing order is determined using each device's SMBus address. Using autonomous sequencing mode (configured using the CFG1 pin), the devices must be assigned sequential SMBus addresses with no missing addresses in the chain. This mode will also constrain each device to have a phase offset according to its SMBus address as described "Phase Spreading" on page 30.

The sequencing group will turn on in order starting with the device with the lowest SMBus address and will continue through to turn on each device in the address chain until all devices connected have been turned on. When turning off, the device with the highest SMBus address will turn off first followed in reverse order by the other devices in the group.

Sequencing is configured by connecting a resistor from the CFG1 pin to ground as described in Table 27. The CFG1 pin is also used to set the configuration of the SYNC pin as well as to determine the sequencing method and order. Please refer to "Switching Frequency and PLL" on page 17 for more details on the operating parameters of the SYNC pin.

Multiple device sequencing may also be achieved by issuing PMBus commands to assign the preceding device in the sequencing chain as well as the device that will follow in the sequencing chain. This method places fewer restrictions on SMBus address (no need of sequential address) and also allows the user to assign any phase offset to any device irrespective of its SMBus device address.

The Enable pins of all devices in a sequencing group must be tied together and driven high to initiate a sequenced turn-on of the group. Enable must be driven low to initiate a sequenced turnoff of the group.

Refer to Application Note AN2033 for details on sequencing via the I^2C/SMBus interface.

Fault Spreading

Digital DC devices can be configured to broadcast a fault event over the DDC bus to the other devices in the group. When a non-destructive fault occurs and the device is configured to shut down on a fault, the device will shut down and broadcast the fault event over the DDC bus. The other devices on the DDC bus will shut down together or in sequencing order, if configured to do so, and will attempt to re-start in their prescribed order if configured to do so.

Temperature Monitoring Using the XTEMP Pin

The ZL2008 supports measurement of an external device temperature using either a thermal diode integrated in a processor, FPGA or ASIC, or using a discrete diode-connected 2N3904 NPN transistor. Figure 21 illustrates the typical connections required.

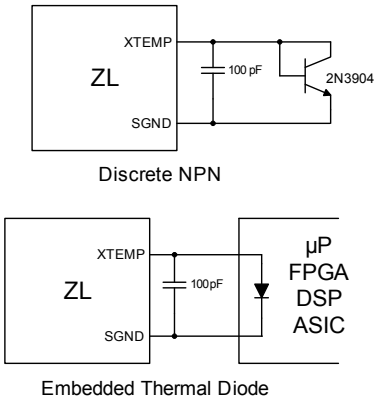


FIGURE 21. External Temperature Monitoring

Active Current Sharing

Paralleling multiple ZL2008 devices can be used to increase the output current capability of a single power rail. By connecting the DDC pins of each device together and configuring the devices as a current sharing rail, the units will share the current equally within a few percent.

Figure 22 illustrates a typical connection for three devices.

The ZL2008 uses a low-bandwidth, first-order digital current sharing technique to balance the unequal device output loading by aligning the load lines of member devices to a reference device.

Droop resistance is used to add artificial resistance in the output voltage path to control the slope of the load line curve, calibrating out the physical parasitic mismatches due to power train components and PCB layout.

TABLE 27. Sequencing Pin-strap and Resistor Settings

R_{CFG1}	SYNC Pin Config	Sequencing Configuration	NLR Timeout and Blanking
LOW	Input	Sequencing is disabled.	1 and 4
OPEN	Auto detect		
HIGH	Output		
10kΩ	Input	Sequencing is disabled.	1 and 4
11kΩ	Auto detect		
12.1kΩ	Output		
14.7kΩ	Input	The ZL2008 is configured as the first device in a nested sequencing group. Turn on order is based on the device SMBus address.	
16.2kΩ	Auto detect		
17.8kΩ	Output		
21.5kΩ	Input	The ZL2008 is configured as a last device in a nested sequencing group. Turn on order is based on the device SMBus address.	
23.7kΩ	Auto detect		
26.1kΩ	Output		
31.6kΩ	Input	The ZL2008 is configured as the middle device in a nested sequencing group. Turn on order is based on the device SMBus address.	
34.8kΩ	Auto detect		
38.3kΩ	Output		
46.4kΩ	Input	Sequencing is disabled.	2 and 8
51.1kΩ	Auto detect		
56.2kΩ	Output		
68.1kΩ	Input	The ZL2008 is configured as the first device in a nested sequencing group. Turn on order is based on the device SMBus address.	
75kΩ	Auto detect		
82.5kΩ	Output		
100kΩ	Input	The ZL2008 is configured as a last device in a nested sequencing group. Turn on order is based on the device SMBus address.	
110kΩ	Auto detect		
121kΩ	Output		
147kΩ	Input	The ZL2008 is configured as the middle device in a nested sequencing group. Turn on order is based on the device SMBus address.	
162kΩ	Auto detect		
178kΩ	Output		

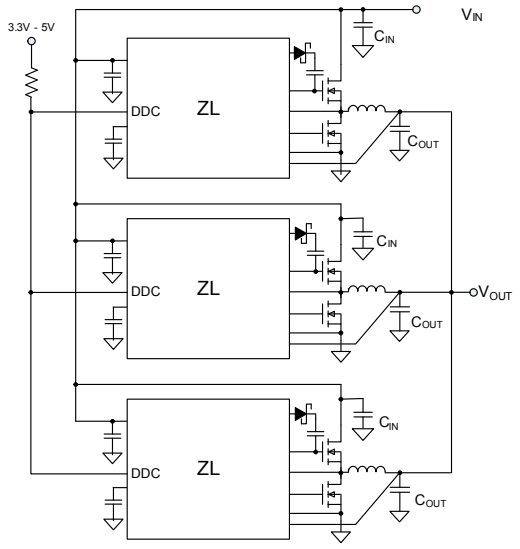


FIGURE 22. Current Sharing Group

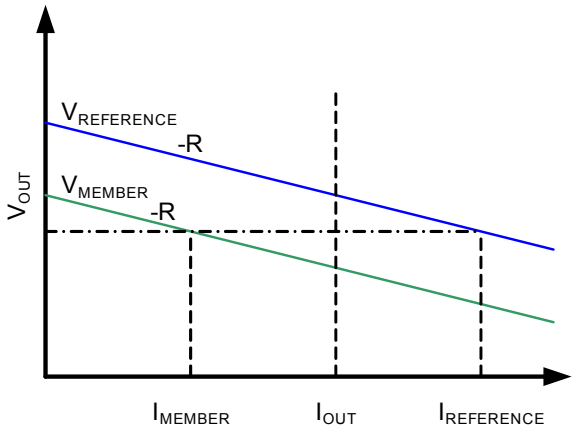


FIGURE 23. Active Current Sharing

Upon system start-up, the device with the lowest member position as selected in ISHARE_CONFIG is defined as the reference device. The remaining devices are members. The reference device broadcasts its current over the DDC bus. The members use the reference current information to trim their voltages (V_{MEMBER}) to balance the current loading of each device in the system.

Figure 23 shows that, for load lines with identical slopes, the member voltage is increased towards the reference voltage which closes the gap between the inductor currents.

The relation between reference and member current and voltage is given by Equation 36:

$$V_{MEMBER} = V_{OUT} + R \times \left(I_{REFERENCE} - I_{MEMBER} \right) \quad \text{(EQ. 36)}$$

where *R* is the value of the droop resistance.

The ISHARE_CONFIG command is used to configure the device for active current sharing. The default setting is a stand-alone non-current sharing device. A current sharing rail can be part of a system sequencing group.

For fault configuration, the current share rail is configured in a quasi-redundant mode. In this mode, when a member device fails, the remaining members will continue to operate and attempt to maintain regulation. Of the remaining devices, the device with the lowest member position will become the reference. If fault spreading is enabled, the current share rail failure is not broadcast until the entire current share rail fails.

Up to eight (8) devices can be configured in a given current sharing rail.

TABLE 28. Current Share Position Settings

R_{CFG2} (kΩ)	Current Share Position	Current Sense
10	0	DCR
11	1	
12.1	2	
13.3	3	
14.7	4	
16.2	5	
17.8	6	
19.6	7	
42.2	0	RDS
46.4	1	
51.1	2	
56.2	3	
61.9	4	
68.1	5	
75	6	
82.5	7	

TABLE 29. Current Share Pin-strap Settings

CFG0 Pin	NLR	Current Share # of Members	Current Sharing
LOW	1.5%	0	Disabled
OPEN	Disabled		
HIGH	2%		

TABLE 30. Current Share Resistor Settings

R_{CFG0} (kΩ)	NLR	Current Share # of Members	Current Sharing
10	Disabled	2	Enabled
11		3	
12.1		4	
13.3		5	
14.7		6	
16.2		7	
17.8		8	
19.6	3%	0	Disabled
21.5		2	Enabled
23.7		3	
26.1		4	
28.7		5	
31.6		6	
34.8		7	
38.3		8	
42.2	2%	0	Disabled
46.4		2	Enabled
51.1		3	
56.2		4	
61.9		5	
68.1		6	
75		7	
82.5		8	
90.9	1.5%	0	Disabled
100		2	Enabled
110		3	
121		4	
133		5	
147		6	
162		7	
178		8	

The phase offset of a current sharing group is automatically set to a value between 0° and 337.5° in 22.5° increments as follows:

$$Phase\ Offset = (SMBus\ Address[4:0] - Current\ Share\ Position) * 22.5° \quad \text{(EQ. 37)}$$

The phase of the individual members in a group are spread evenly from the phase offset of the group.

Please refer to Application Note AN2034 for additional details on current sharing.

Phase Adding/Dropping

The ZL2008 allows multiple power converters to be connected in parallel to supply higher load currents than can be addressed using a single-phase design. In doing so, the power converter is optimized at a load current range that requires all phases to be operational. During periods of light loading, it may be beneficial to disable one or more phases in order to eliminate the current drain and switching losses associated with those phases, resulting in higher efficiency.

The ZL2008 offers the ability to add and drop phases using a the phase enable pin or a PMBus command in response to an observed load current change. All phases in a current share rail are considered active prior to the current sharing rail ramp to power-good.

Phases can be dropped after power-good is reached. The phase enable pin can be used to drop and add phases:

- Set PH_EN = 0 to drop a phase
- Set PH_EN = 1 to add a phase

The time to detect a change of state of the phase enable pin is between 0ms and 3ms (max).

Any member of the current sharing rail can be dropped. If the reference device is dropped, the remaining active device with the lowest member position will become the new reference.

Additionally, any change to the number of members of a current sharing rail will precipitate autonomous phase distribution within the rail where all active phases realign their phase position based on their order within the number of active members.

If the members of a current sharing rail are forced to shut down due to an observed fault, all members of the rail will attempt to re-start simultaneously after the fault has cleared.

For single phase operation, that is, not current sharing, the PH_EN pin is ignored and can be left open.

Monitoring via I²C/SMBus

A system controller can monitor a wide variety of different ZL2008 system parameters through the I²C/SMBus interface. The device can monitor for fault conditions by monitoring the SALRT pin, which will be pulled low when any number of pre-configured fault conditions occur.

The device can also be monitored continuously for any number of power conversion parameters including but not limited to the following:

- Input voltage/Output voltage
- Output current
- Internal and external temperature
- Switching frequency
- Duty cycle

The PMBus Host should respond to SALRT as follows:

1. ZL device pulls SALRT Low
2. PMBus Host detects that SALRT is now low, performs transmission with Alert Response Address to find which ZL device is pulling SALRT low.
3. PMBus Host talks to the ZL device that has pulled SALRT low. The actions that the host performs are up to the System Designer.

If multiple devices are faulting, SALRT will still be low after doing the above steps and will require transmission with the Alert Response Address repeatedly until all faults are cleared.

Please refer to Application Note AN2033 for details on how to monitor specific parameters via the I²C/SMBus interface.

Snapshot Parameter Capture

The ZL2008 offers a special feature that enables the user to capture parametric data during normal operation or following a fault. The Snapshot functionality is enabled by setting bit 1 of MISC_CONFIG to 1.

See AN2033 for details on using the Snapshot in addition to the parameters supported. The Snapshot feature enables the user to read status and parameters via a block read transfer through the SMBus. This can be done during normal operation, although it should be noted that reading the 22 bytes will occupy the SMBus for some time.

The SNAPSHOT_CONTROL command enables the user to store the snapshot parameters to Flash memory in response to a pending fault as well as to read the stored data from Flash memory after a fault has occurred. Table 31 describes the usage of this command. Automatic writes to Flash memory following a fault are triggered when any fault threshold level is exceeded, provided that the specific fault's response is to shut down (writing to Flash memory is not allowed if the device is configured to re-try following the specific fault condition). It should also be noted that the device's V_{DD} voltage must be maintained during the time when the device is writing the data to Flash memory; a process that requires between 700µs to 1400µs depending on whether the data is set up for a block write. Undesirable results may be observed if the device's V_{DD} supply drops below 3.0V during this process.

TABLE 31. SNAPSHOT_CONTROL Command

Data Value	Description
1	Copies current SNAPSHOT values from Flash memory to RAM for immediate access using SNAPSHOT command.
2	Writes current SNAPSHOT values to Flash memory. Only available when device is disabled.

In the event that the device experiences a fault and power is lost, the user can extract the last SNAPSHOT parameters stored during the fault by writing a 1 to SNAPSHOT_CONTROL (transfers data from Flash memory to RAM) and then issuing a SNAPSHOT command (reads data from RAM via SMBus).

Non-Volatile Memory and Device Security Features

The ZL2008 has internal non-volatile memory where user configurations are stored. Integrated security measures ensure that the user can only restore the device to a level that has been made available to them. Refer to "Start-up Procedure" on page 15 for details on how the device loads stored values from internal memory during start-up.

During the initialization process, the ZL2008 checks for stored values contained in its internal non-volatile memory. The ZL2008 offers two internal memory storage units that are accessible by the user as follows:

1. *Default Store*: A power supply module manufacturer may want to protect the module from damage by preventing the user from being able to modify certain values that are related to the physical construction of the module. In this case, the module manufacturer would use the Default Store and would allow the user to restore the device to its default setting but would restrict the user from restoring the device to the factory settings.
2. *User Store*: The manufacturer of a piece of equipment may want to provide the ability to modify certain power supply settings while still protecting the equipment from modifying values that can lead to a system level fault. The equipment manufacturer would use the User Store to achieve this goal.

Please refer to Application Note AN2033 for details on how to set specific security measures via the I²C/SMBus interface.

Pin-strap Current Sharing Configuration

A 3-phase current sharing group example is shown in Figure 24. Each ZL2008 device in the group is connected to the same DDC bus and SMBus. Also, the enable pins are connected together to allow all devices in the current sharing group to enable simultaneously.

The device with the lowest position number becomes the reference device. The reference device provides the load current information to each member device. If the reference device is

dropped or faults then the device with the next lowest position number will become the new reference device.

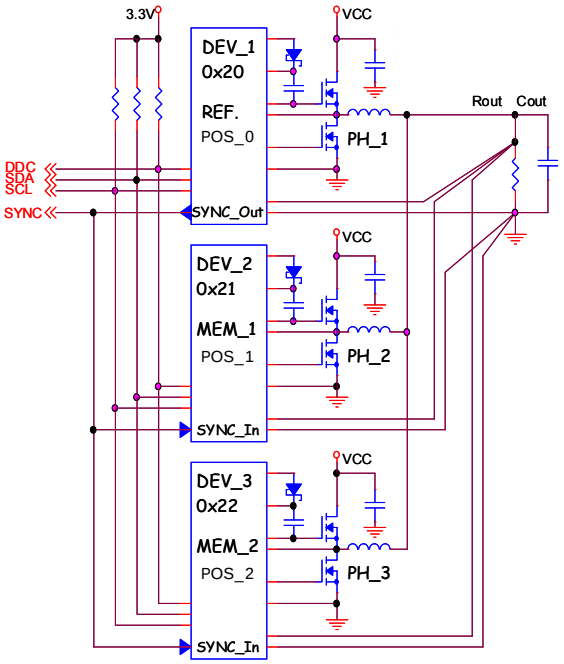


FIGURE 24. 3-phase Current Sharing Group

SMBus Address (SA0, SA1 Pins)

Assign sequential SMBus addresses to each device in the current sharing group. If other non-current sharing devices are connected to the same SMBus then assign addresses to these devices that are before or after the current sharing group.

Current Share Pin-Straps (CFG0, CFG2 Pins)

Resistor pin-strap the CFG0 pin to set the following parameters:

a. **Current Share # of Members** – Number of devices or phases in a current sharing group (2 minimum and 8 maximum).

b. **Current Share Control** – Current sharing is automatically enabled when the number of members is 2 (and disabled when members is = 0).

Resistor pin-strap the CFG2 pin to set the current share position:

c. **Current Share Position** – Sequential numbering from 0 to 7 (max) of N number of members starting with the reference device in position 0 and ending with the last member device in position N-1.

For the 3-phase group the parameters for each device are shown in Table 32.

TABLE 32. Current Share Parameters

Device	SMBus Address	# of Members	Position	Control
Reference	0x20	3	0	Enabled
Member_1	0x21	3	1	Enabled
Member_2	0x22	3	2	Enabled

SYNC Clock (CFG1 Pin)

Typically the reference device sources the SYNC clock. However, any device internal or external to the current sharing group can source the SYNC clock. If the reference device is sourcing the SYNC clock, then resistor pin-strap the CFG1 pin to configure the SYNC pin as an output. Otherwise configure the reference device's SYNC pin as an input. For member devices, resistor pin-strap the CFG1 pin to configure the SYNC pin as an input.

Soft-start (SS Pin)

Current sharing groups require proper synchronization prior to ramp events. Resistor pin-strap the SS pin to set the following parameters:

a. **Delay Time** – The reference device's soft-start delay time must be at least 10ms greater than any member device to ramp up/down current sharing. The reference device requires this additional time to coordinate a synchronization signal to all member devices.

b. **Ramp Time** – A minimum soft-start ramp time of 5ms is required for both reference and member devices to ramp up/down current sharing.

Phase Enable (PH_EN Pin)

Phase enable is used to dynamically add or drop a current sharing phase during operation. Set the PH_EN pin high to enable a phase and low to disable a phase (open is an invalid state). The PH_EN pin replaces the PHASE_CONTROL command.

For proper operation, the pin must be externally driven high or low without switching glitches. Also, ensure phase enable is high for the reference and member devices of a current sharing group prior to ramp-up.

MFR_CONFIG Command

Application specific values are set by the MFR_CONFIG command. The following parameters must be set to properly configure current sharing.

a. **Current Sense Blanking Delay** (bits 15:11) – The current sense delay parameter controls the blanking time when no current measurement is taken. This allows the filtering of noise from the current measurement circuit when the FETs are switching. The actual value selected depends on f_{SW}, sensing method and ring-out duration. The same delay is used for both reference and member devices.

b. **Current Sense Control** (bits 5:4) – Three modes of current sensing are available depending on duty cycle and switching frequency as listed in Table 33 (also refer to "Current Limit Threshold Selection" on page 21). The same sensing is used for both reference and member devices.

Note, the following parameters are automatically set when current sharing is enabled.

Alternate Ramp Control (bit 2) – Automatically set to "1" (enabled) for both reference and member devices when current sharing is enabled.

SYNC Pin Output Control (bit 0) – Automatically set to push-pull for a SYNC clock output and open-drain for a SYNC clock input.

TABLE 33. Current Sense Options

Current Sense Configuration	Usage
Ground referenced, down slope ($R_{DS(ON)}$ sensing)	Low duty cycle and low f_{SW}
V_{out} referenced, down slope (Inductor DCR sensing)	Low duty cycle and high f_{SW}
V_{out} referenced, up slope (Inductor DCR sensing)	High duty cycle

VOUT_DROOP Command

The droop or load-line resistance is used as part of the current sharing algorithm. When current sharing is enabled, VOUT_DROOP is automatically set to a value of 0xBA80 (1.25mΩ). The same droop value is used for both reference and member devices.

Current Sharing Example

Example pin-strap resistor values for the current sharing group in Figure 24 are shown in Table 34. Sequential SMBus addresses are used with the reference device at the lowest address. The reference device outputs the SYNC clock to the member devices SYNC clock input. The devices are configured for 3-phase current sharing with all phases enabled. The reference device soft-start ramp time is at least 5ms and soft-start delay time is at least 10ms greater than the member devices for proper synchronization and output voltage ramp.

TABLE 34. Pin-Strap Current Sharing Resistor Values

Pin	Reference	Member_1	Member_2	Description
SA0, SA1	Low, Low	Open, Low	High, Low	SMBus Address = 0x20 for Reference SMBus Address = 0x21 for Member_1 SMBus Address = 0x22 for Member_2
CFG0	23.7kΩ	23.7kΩ	23.7kΩ	Current Share # of Members = 3 Current Share Control = Enabled
CFG1	High	Low	Low	SYNC = Output for Reference SYNC = Input for Member_1 and Member_2
CFG2	42.2kΩ	46.4kΩ	51.1kΩ	Current Share Position = 0 for Reference Current Share Position = 1 for Member_1 Current Share Position = 2 for Member_2
SS	31.6kΩ	14.7kΩ	14.7kΩ	Delay = 15ms, Ramp = 5ms for Reference Delay = 5ms, Ramp = 5ms for Member_1 Delay = 5ms, Ramp = 5ms for Member_2
PH_EN	High	High	High	All Phases Enabled

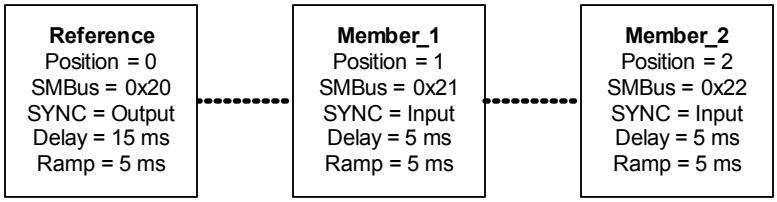


FIGURE 25.

Ordering Information

PART NUMBER (Notes 19, 20, 21)	PART MARKING	TEMP RANGE (°C)	PACKAGE	PKG. DWG. #
ZL2008ALBFT	2008	-40 to +85	36 Ld 6mmx6mm QFN	L36.6x6A
ZL2008ALBFT1	2008	-40 to +85	36 Ld 6mmx6mm QFN	L36.6x6A

NOTES:

19. Please refer to TB347 for details on reel specifications.
20. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
21. For Moisture Sensitivity Level (MSL), please see device information page for ZL2008. For more information on MSL please see techbrief TB363.

Related Tools and Documentation

The following application support documents and tools are available to help simplify your design.

Item	Description
AN2010	Application Note: Thermal and Layout Guidelines
AN2032	Application Note: NLR Configuration
AN2033	Application Note: PMBus Command Set
AN2034	Application Note: Current Sharing
AN2035	Application Note: Compensation Using CompZL

Revision History

Rev. #	Description	Date
1.0	Initial release	January 2009
FN6859.0	Assigned file number FN6859 to datasheet as this will be the first release with an Intersil file number. Replaced header and footer with Intersil header and footer. Updated disclaimer information to read “Intersil and it’s subsidiaries including Zilker Labs, Inc.” No changes to datasheet content	February 2009
FN6859.1	Updated to new format. Updates include: a) Putting Abs Max, Recommended Operating Conditions and Electrical Specs tables into Intersil format - Adding Pb-free reflow link to Thermal info - Adding Intersil's caution statement, per legal b) Put Ordering Info table into Intersil format - Adding Moisture Sensitivity Level note, TB347 tape and reel spec note and Pb-free note (corresponding to lead finish). c) Updated sales disclaimer on last page to Intersil's verbiage d) Replaced Zilker POD with Intersil equivalent POD (L36.6x6A) e) Updated graphics to Intersil standards (font change) f) Updated cross references to tables (since table #s were removed from Electrical Specs, Abs Max, Recommended Operating Conditions and Pin Descriptions tables) g) Updated cross references to figures (since figure #s was removed from Pinout) h) Added equation #s to all equations i) Added Intersil standard over temp notes to Electrical Specs table as follows: - Added Note 14: "Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested." to MIN MAX columns of Electrical Specs table. -Added "Boldface limits apply over the operating temperature range, -40°C to +85°C" to common conditions of Electrical Specs table. Bolded all MIN and MAX specs in table. “Absolute Maximum Ratings” on page 4: Removed “MOSFET Drive Reference for VR Pin.....120mA”. Removed “2.5V Logic Reference for V25 Pin .....120mA” “Electrical Specifications” table, page 4 to page 6: Changed Max for I_{DDS} Shutdown Current from 8mA to 9mA. Changed conditions for “Vr Reference Output Voltage” from <50mA to <20mA Changed conditions for “V25 Reference Output Voltage” from <50mA to <20mA Added the following sentence to Note 8: “Current Share member minimum delay is 5ms. Current share reference must be 10ms greater than member delay” Added Note 15: “Limits established by characterization and are not production tested.” Added Note 15 callout to the following parameters: Soft start delay duration range for test condt using I^2C Minimum Sync Pulse Width High-side Driver Peak Gate Drive Current (Pull-down) High-side Driver Pull-up Resistance High-side Driver Pull-down Resistance Low-side Driver Pull-up Resistance Low-side Driver Pull-down Resistance Switching timing (for both conditions) VTRK Tracking Ramp Accuracy UVLO Delay UVLO Hysteresis for I^2C/SMBus conditions Power Good Delay for I^2C/SMBus conditions VSEN Undervoltage Threshold for I^2C/SMBus conditions VSEN Overvoltage Threshold for I^2C/SMBus conditions VSEN Undervoltage/Overvoltage Fault Response Time for I^2C/SMBus conditions Current Limit Protection Delay for I^2C/SMBus conditions Temperature Compensation of Current Limit Protection Threshold for I^2C/SMBus conditions Thermal Protection Threshold (Junction Temperature) for I^2C/SMBus conditions	October 2009

Revision History (Continued)

Rev. #	Description	Date
FN6859.1	Added Note 15: “Nominal capacitance of logic pins is 5pF”. Added Note 15 callouts to Logic Output Low, V_{OL} and Logic Output High, V_{OH} parameters. Changed “Logic Input Bias Current” parameter to “Logic Input Leakage Current”. Changed Logic Input Leakage Current Min from -10µA to -250nA and Max from 10µA to 250nA. Removed “MGN Input Bias Current” line from table. Changed “Power Good V_{OUT} Low Threshold” parameter to “Power Good V_{OUT} Threshold” and removed “Power Good V_{OUT} High Threshold” line from table. Page 10: Removed 2 paragraphs as follows: “The ZL2008 can be configured by simply connecting its pins according to the tables provided in the following sections... I^2C/SMBus interface using an available computer and the included USB cable.” “Application notes and ... local Zilker Labs sales office to order an evaluation kit” Throughout: Changed all referenced Zilker App note numbers to newly assigned Intersil numbers (e.g. AN33 -> AN2033) “Current Limit Threshold Selection” on page 21. In paragraph below Figure 16, changed “The current sensing method can be selected via the I^2C/SMBus interface.” to “The current sensing method can be selected using the CFG2 pin as shown in Tables 26 and 28 or via the I^2C/SMBus interface.” In 3rd paragraph below Figure 16, changed “This is to avoid taking a reading just after a current load step” to “This is to avoid taking a reading just after a switching transition”. Added “Note that IOUT_CAL_GAIN is set to 2mΩ by default.” to end of last paragraph. Added “(Voltage seen on 2mΩ)” to Tables 14 and 15 captions on page 21. Replaced Table 25. Phase Offset Pin-strap Settings on page 30 (changed “CFG2 Pin” column to “R_{CFG2}” and added “Current Sense” column). Table 26. Phase Offset Resistor Settings on page 30. Added “Current Sense” column and R_{CFG2} rows from 42.2kΩ through 162kΩ and corresponding Phase Offset rows. On page 30: 2nd column, 1st paragraph, changed “The phase offset of (multi-phase) current sharing devices is automatically set to a value between 0° and 337.5° in 22.5° increments as follows: Phase Offset = SMBus Address[4:0] –Current Share Position * 22.5°” to “The phase offset of a current sharing group is automatically set to a value between 0° and 337.5° in 22.5° increments as follows: Phase Offset = (SMBus Address[4:0] –Current Share Position) * 22.5°” Added “The phase of the individual members in a group are spread evenly from the phase offset of the group.” Table 28. Current Share Position Settings on page 33. Added “Current Sense” column. Added R_{CFG2} rows from 42.2kΩ through 82.5kΩ and corresponding Current Share Position rows. Removed former Table 35. Snapshot Parameters “Snapshot Parameter Capture” on page 35. Added “See AN2033 for details on using the Snapshot in addition to the parameters supported.” to 2nd paragraph On page 4, corrected: “Analog Input Voltages for ISENA Pin. . . . . .1.5V to 30V” to: “Analog Input Voltages for ISENA Pin. . . . . .-1.5V to 6.5V” On page 21, Table 14, added “DCR V_{LIM} (mV)” column. Renamed “Threshold Voltage” column to “R_{DS} V_{LIM}” On page 22, Table 15, added “DCR V_{LIM} (mV)” column. Renamed “V_{LIM}” column to “R_{DS} V_{LIM}” On page 21, in second column, first paragraph, changed “Note that IOUT_CAL_GAIN is set to 2mΩ by default.” to “By default, the IOUT_CAL_GAIN is set to 1mΩ for DCR mode and 2mΩ for RDS mode.” In Table 14 on page 21, removed “ (Voltage seen on 2mΩ)” from caption In Table 15 on page 22, removed “(Voltage seen on 2mΩ)” from caption	October 2009
	“Power Good” on page 16, changed 2nd sentence from “...if the output is within -10%/+15% of the target voltage.” to “...if the output is within -10% of the target voltage.” Replaced last paragraph in “Power Good” section. “Fault Spreading” on page 31, added “or in sequencing order” to last sentence. Change marketing part number to ZL2008ALBFT to note firmware revision.	November 2009

Revision History (Continued)

Rev. #	Description	Date
FN6859.2	Added “ESD Rating” on page 4. Added Note 1 to “ESD Rating” on page 4 Added “Latch Up (Tested per JESD78) 100mA” on page 4 Table 26 “Phase Offset Resistor Settings” on page 30, in third column titled "Current Sense", swapped RDS and DCR so DCR is in the top part of the table and RDS in the bottom. Added “About Intersil” on page 42 Corrected Note 2 in “Thermal Information” on page 4 from: “θ_{JA} is measured with the component mounted on a high effective thermal conductivity test board in free air. See Tech Brief TB379 for details.” To: “θ_{JA} is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech Brief TB379.” In Table 28 on page 33, in the third column, swapped DCR and RDS so that RDS is on the bottom. “Active Current Sharing” on page 31, second paragraph changed from "Figure 21 illustrates a typical ..." to "Figure 22 illustrates a typical ..." On page 36, second column, changed from “Resistor pin-strap the CFG2 pin to set the following parameter:” change this to say “Resistor pin-strap the CFG2 pin to set the current share position.”	April 2010
FN6859.3	Added following statement to disclaimer on page 42: “This product is subject to a license from Power One, Inc. related to digital power technology as set forth in U.S. Patent No. 7,000,125 and other related patents owned by Power One, Inc. These license rights do not extend to stand-alone POL regulators unless a royalty is paid to Power One, Inc.”	December 2010
FN6859.4	Updated to new template. Removed Electrical specs notes 14 and 15: 14. Parameters with MIN and/or MAX limits are 100% tested at +25°C, unless otherwise specified. Temperature limits established by characterization and are not production tested. 15. Limits established by characterization and are not production tested. and replaced with new Note 14: “Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.” Page 1, 1st sentence, changed “The ZL2008 is a digital DC/DC controller with ...” to “ZL20081 is a digital power controller with...” Page 4, Abs Max Ratings, the entry for Logic I/O pins, changed from "-0.3V to 6.5V" to "-0.3 to 6V" Page 29, 2nd column, added sentence “Note that the SMBus address 0x4B is reserved for device test and cannot be used in the system.” at the end of column two.	December 2010
	Add the following lines to the“Recommended Operating Conditions” on page 4: Input Voltage V_{IN}, Rise Time .. . . . . .5ms minimum V_{IN} Ramp . . . . .Monotonic	

About Intersil

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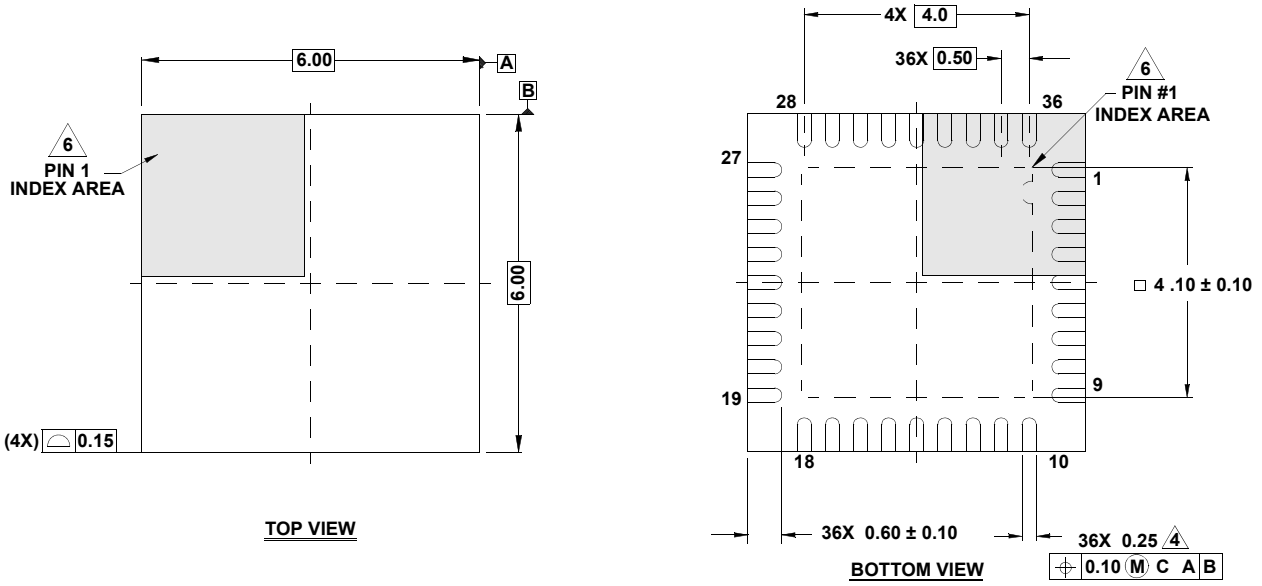
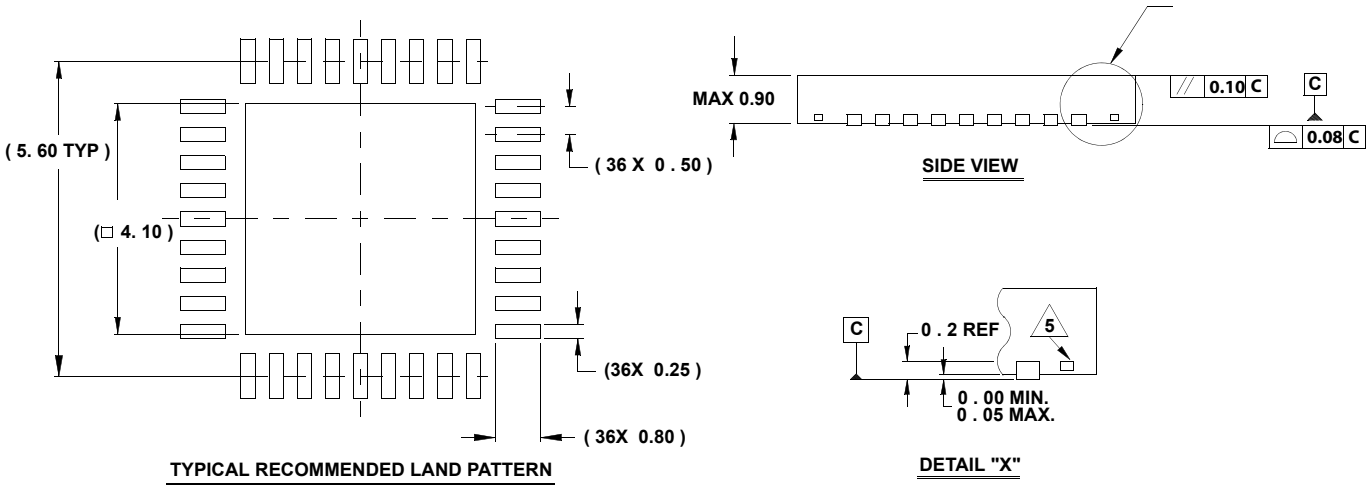
Package Outline Drawing

L36.6x6A

36 LEAD QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 1, 9/09





NOTES:

1. Dimensions are in millimeters.
   Dimensions in ( ) for Reference Only.
2. Dimensioning and tolerancing conform to AMSE Y14.5m-1994.
3. Unless otherwise specified, tolerance : Decimal ± 0.05
4. Dimension b applies to the metallized terminal and is measured between 0.15mm and 0.30mm from the terminal tip.
5. Tiebar shown (if present) is a non-functional feature.
6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 indentifier may be either a mold or mark feature.
7. Compliant to JEDEC MO-220VJJD.

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