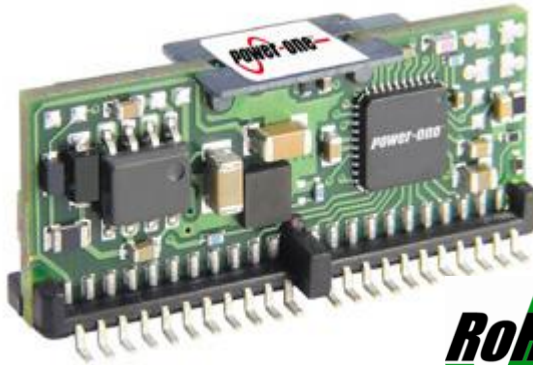




**THE DATASHEET OF  
ZY7115LG-T3**





### Applications

- Low voltage, high density systems with Intermediate Bus Architectures (IBA)
- Point-of-load regulators for high performance DSP, FPGA, ASIC, and microprocessor applications
- Desktops, servers, and portable computing
- Broadband, networking, optical, and communications systems
- Active memory bus terminators

### Benefits

- Integrates digital power conversion with intelligent power management
- Eliminates the need for external power management components
- Completely programmable via industry-standard I<sup>2</sup>C communication bus
- One part that covers all applications
- Reduces board space, system cost and complexity, and time to market

### Description

Power-One's point-of-load converters are recommended for use with regulated bus converters in an Intermediate Bus Architecture (IBA). The ZY7115 is an intelligent, fully programmable step-down point-of-load DC-DC module integrating digital power conversion and intelligent power management. When used with ZM7300 Series Digital Power Managers, the ZY7115 completely eliminates the need for external components for sequencing, tracking, protection, monitoring, and reporting. All parameters of the ZY7115 are programmable via the industry-standard I<sup>2</sup>C communication bus and can be changed by a user at any time during product development and service.

### Features

- RoHS lead free and lead-solder-exempt products are available
- Wide input voltage range: 3V–13.2V
- High continuous output current: 15A
- Wide programmable output voltage range: 0.5V–5.5V
- Active digital current share
- Single-wire serial communication bus for frequency synchronization, programming, and monitoring
- Optimal voltage positioning with programmable slope of the VI line
- Overcurrent, overvoltage, undervoltage, and overtemperature protections with programmable thresholds and types
- Programmable fixed switching frequency 0.5-1.0MHz
- Programmable turn-on and turn-off delays
- Programmable turn-on and turn-off voltage slew rates with tracking protection
- Programmable feedback loop compensation
- Power Good signal with programmable limits
- Programmable fault management
- Start up into the load pre-biased up to 100%
- Full rated current sink
- Real time voltage, current, and temperature measurements, monitoring, and reporting
- Small footprint SMT package: 8x32mm
- Low profile of 14mm
- Compatible with conventional pick-and-place equipment
- Wide operating temperature range
- UL 60950-1/CSA 22.2 No. 60950-1-07 Second Edition, IEC 60950-1: 2005, and EN 60950-1:2006

# ZY7115 15A DC-DC Intelligent POL Data Sheet

## 3V to 13.2V Input • 0.5V to 5.5V Output



### Reference Documents:

- ZM7300 Digital Power Manager Data Sheet
- ZM7300 Digital Power Manager Programming Manual
- Power-One I2C Graphical User Interface
- ZM00056-KIT USB to I<sup>2</sup>C Adapter Kit User Manual

### 1. Ordering Information

| ZY  | 71  | 15                            | x  | y   | -           | zz   |
|---|---|-------------------------------|--|---|-------------|--|
| <b>Product family:</b><br>Z-One<br>Module | <b>Series:</b><br>Intelligent<br>POL<br>Converter | <b>Output Current:</b><br>15A | <b>Output voltage setpoint accuracy:</b><br>L – 1.2% or 20mV,<br>whichever is greater.<br>H <sup>1</sup> – 1.0% or 10mV,<br>whichever is greater | <b>RoHS compliance:</b><br>No suffix - RoHS<br>compliant with Pb<br>solder exemption <sup>2</sup><br>G - RoHS compliant<br>for all six substances | <b>Dash</b> | <b>Packaging Option<sup>3</sup>:</b><br>T1 – 500pcs T&R<br>T2 – 100pcs T&R<br>T3 – 50pcs T&R<br>Q1 – 1pc sample for<br>evaluation only |

<sup>1</sup> Contact factory for availability.

<sup>2</sup> The solder exemption refers to all the restricted materials except lead in solder. These materials are Cadmium (Cd), Hexavalent chromium (Cr6+), Mercury (Hg), Polybrominated biphenyls (PBB), Polybrominated diphenylethers (PBDE), and Lead (Pb) used anywhere except in solder.

<sup>3</sup> Packaging option is used only for ordering and not included in the part number printed on the POL converter label.

<sup>4</sup> The evaluation board is available in only one configuration: ZM7300-KIT-HKS.

Example: **ZY7115HG-T2**: A 100-piece reel of RoHS compliant POL converters with the output voltage setpoint of 1.0% or 10mV, whichever is greater. Each POL converter is labeled ZY7115HG.

### 2. Absolute Maximum Ratings

Stresses in excess of the absolute maximum ratings may cause performance degradation, adversely affect long-term reliability, and cause permanent damage to the converter.

| Parameter             | Conditions/Description               | Min | Max | Units |
|-----------------------|--------------------------------------|-----|-----|-------|
| Operating Temperature | Controller case temperature          | -40 | 105 | °C    |
| Input Voltage         | 250ms Transient                      |     | 15  | VDC   |
| Output Current        | (See Output Current Derating Curves) | -15 | 15  | ADC   |

### 3. Environmental and Mechanical Specifications

| Parameter                  | Conditions/Description                       | Min            | Nom | Max        | Units    |
|----------------------------|--|----------------|-----|------------|----------|
| Ambient Temperature Range  |  | -40            |     | 85         | °C       |
| Storage Temperature (Ts)   |  | -55            |     | 125        | °C       |
| Weight                     |  |                |     | 15         | grams    |
| MTBF                       | Calculated Per Telcordia Technologies SR-332 | 4.82           |     |            | MHrs     |
| Peak Reflow Temperature    | ZY7115<br>ZY7115G                            |                | 245 | 220<br>260 | °C<br>°C |
| Lead Plating               | ZY7115 and ZY7115G                           | 100% Matte Tin |     |            |          |
| Moisture Sensitivity Level | ZY7115 and ZY7115G                           | 3              |     |            |          |



### 4. Electrical Specifications

Specifications apply at the input voltage from 3V to 13.2V, output load from 0 to 15A, ambient temperature from -40°C to 85°C, 100µF output capacitance, and default performance parameters settings unless otherwise noted.

#### 4.1 Input Specifications

| Parameter  | Conditions/Description   | Min  | Nom         | Max  | Units      |
|--|--|------|-------------|------|------------|
| Input voltage ( $V_{IN}$ )                             | At $V_{IN}<4.75V$ , VLDO pin needs to be connected to an external voltage source higher than 4.75V | 3    |             | 13.2 | VDC        |
| Input Current (at no load)                             | $V_{IN}\geq 4.75V$ , VLDO pin connected to $V_{IN}$  |      | 50          |      | mADC       |
| Undervoltage Lockout (VLDO connected to $V_{IN}$ )     | Ramping Up<br>Ramping Down   |      | 4.2<br>3.75 |      | VDC<br>VDC |
| Undervoltage Lockout (VLDO connected to $V_{AUX}=5V$ ) | Ramping Up<br>Ramping Down   |      | 3.0<br>2.5  |      | VDC<br>VDC |
| External Low Voltage Supply                            | Connect to VLDO pin when $V_{IN}<4.75V$  | 4.75 |             | 13.2 | VDC        |
| VLDO Input Current                                     | Current drawn from the external low voltage supply at $V_{LDO}=5V$                                 |      | 50          |      | mADC       |

#### 4.2 Output Specifications

| Parameter  | Conditions/Description  | Min                        | Nom                        | Max   | Units                      |
|--|---|----------------------------|----------------------------|-------|----------------------------|
| Output Voltage Range ( $V_{OUT}$ )                                       | Programmable <sup>1</sup><br>Default (no programming)   | 0.5                        | 0.5                        | 5.5   | VDC<br>VDC                 |
| Output Voltage Setpoint Accuracy   | $V_{IN}=12V$ , $I_{OUT}=0.5*I_{OUT\ MAX}$ ,<br>$F_{SW}=500kHz$ , room temperature   | (See Ordering Information) |                            |       |                            |
| Output Current ( $I_{OUT}$ )   | $V_{IN\ MIN}$ to $V_{IN\ MAX}$  | -15 <sup>2</sup>           |                            | 15    | ADC                        |
| Line Regulation  | $V_{IN\ MIN}$ to $V_{IN\ MAX}$  |                            | ±0.3                       |       | % $V_{OUT}$                |
| Load Regulation  | 0 to $I_{OUT\ MAX}$   |                            | ±0.2                       |       | % $V_{OUT}$                |
| Dynamic Regulation<br>Peak Deviation<br>Settling Time                    | Slew rate 2.5A/µs, 50 - 100% load step<br>$C_{OUT}=300\mu F$ , $F_{SW}=1MHz$<br>to 10% of peak deviation  |                            | 100<br>50                  |       | mV<br>µs                   |
| Output Voltage Peak-to-Peak<br>Ripple and Noise<br>BW=20MHz<br>Full Load | $V_{IN}=5.0V$ , $V_{OUT}=0.5V$ , $F_{SW}=500kHz$<br>$V_{IN}=13.2V$ , $V_{OUT}=0.5V$ , $F_{SW}=500kHz$<br>$V_{IN}=5.0V$ , $V_{OUT}=2.5V$ , $F_{SW}=500kHz$<br>$V_{IN}=13.2V$ , $V_{OUT}=2.5V$ , $F_{SW}=500kHz$<br>$V_{IN}=13.2V$ , $V_{OUT}=5.0V$ , $F_{SW}=500kHz$ |                            | 10<br>15<br>10<br>25<br>35 |       | mV<br>mV<br>mV<br>mV<br>mV |
| Temperature Coefficient  | $V_{IN}=12V$ , $I_{OUT}=0.5*I_{OUT\ MAX}$   |                            | 20                         |       | ppm/°C                     |
| Switching Frequency  | Default<br>Programmable, 250kHz steps   | 500                        | 500                        | 1,000 | kHz<br>kHz                 |
| Duty Cycle Limit   | Default<br>Programmable, 1.56% steps  | 0                          | 90.5                       | 95    | %<br>%                     |

<sup>1</sup> ZY7115 is a step-down converter, thus the output voltage is always lower than the input voltage as show in Figure 1.

<sup>2</sup> At the negative output current (bus terminator mode) efficiency of the ZY7115 degrades resulting in increased internal power dissipation. Therefore maximum allowable negative current under specific conditions is 20% lower than the current determined from the derating curves shown in paragraph 5.5.

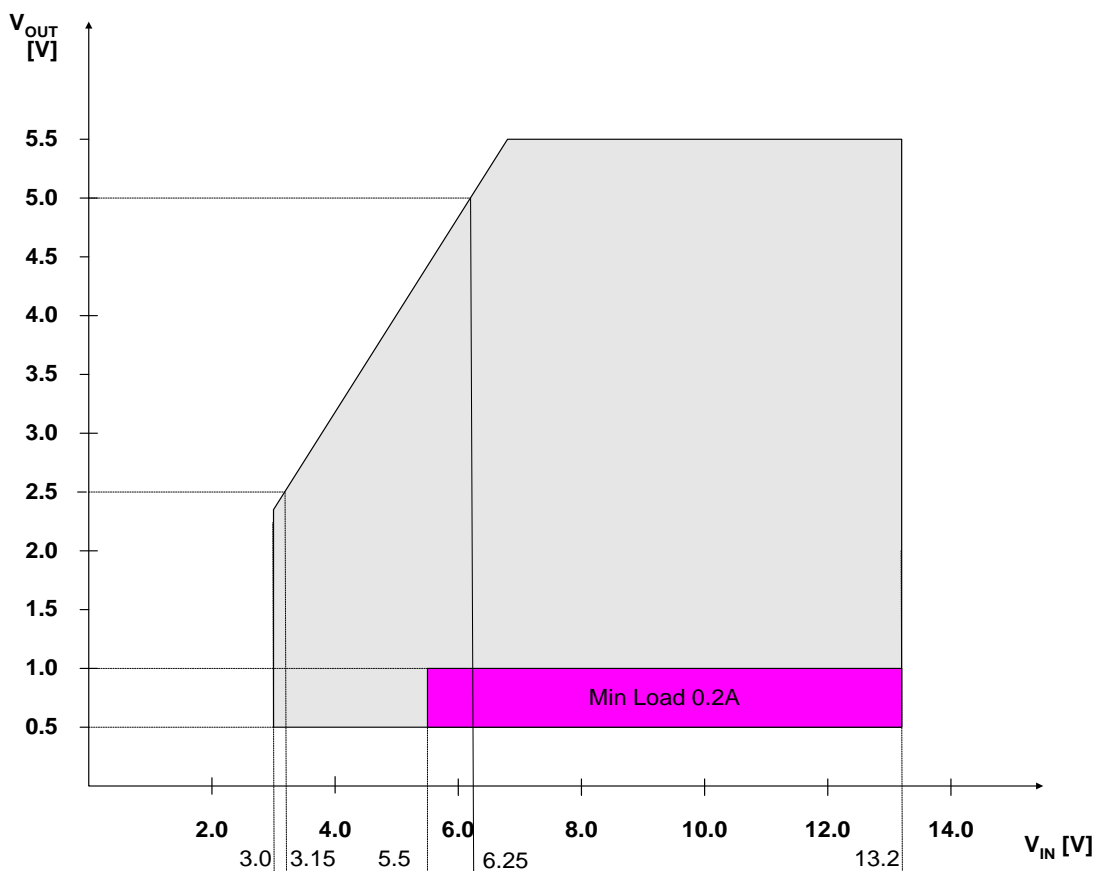


Figure 1. Output Voltage as a Function of Input Voltage and Output Current

### 4.3 Protection Specifications

| Parameter                            | Conditions/Description  | Min   | Nom | Max | Units                                      |
|--------------------------------------|---|---|-----|-----|--|
| <b>Output Overcurrent Protection</b> |   |   |     |     |  |
| Type                                 | Default<br>Programmable   | Non-Latching, 130ms period<br>Latching/Non-Latching |     |     |  |
| Threshold                            | Default<br>Programmable in 11 steps   | 60  | 170 | 170 | %I <sub>OUT</sub><br>%I <sub>OUT</sub>     |
| Threshold Accuracy                   |   | -25   |     | 25  | %I <sub>OCP.SET</sub>                      |
| <b>Output Overvoltage Protection</b> |   |   |     |     |  |
| Type                                 | Default<br>Programmable   | Non-Latching, 130ms period<br>Latching/Non-Latching |     |     |  |
| Threshold                            | Default<br>Programmable in 10% steps  | 110 <sup>1</sup>                                    | 130 | 130 | %V <sub>O.SET</sub><br>%V <sub>O.SET</sub> |
| Threshold Accuracy                   | Measured at V <sub>O.SET</sub> =2.5V  | -2  |     | 2   | %V <sub>OVP.SET</sub>                      |
| Delay                                | From instant when threshold is exceeded until the turn-off command is generated |   | 6   |     | μs   |

| <b>Output Undervoltage Protection</b>     |   |  |             |      |  |
|---|---|--|-------------|------|--|
| Type                                      | Default Programmable  | Non-Latching, 130ms period Latching/Non-Latching |             |      |  |
| Threshold                                 | Default Programmable in 5% steps  | 75   | 75          | 85   | %V <sub>O.SET</sub><br>%V <sub>O.SET</sub> |
| Threshold Accuracy                        | Measured at V <sub>O.SET</sub> =2.5V  | -2   |             | 2    | %V <sub>UVP.SET</sub>                      |
| Delay                                     | From instant when threshold is exceeded until the turn-off command is generated       |  | 6           |      | µs   |
| <b>Overtemperature Protection</b>         |   |  |             |      |  |
| Type                                      | Default Programmable  | Non-Latching, 130ms period Latching/Non-Latching |             |      |  |
| Turn Off Threshold                        | Temperature is increasing   |  | 130         |      | °C   |
| Turn On Threshold                         | Temperature is decreasing after the module was shut down by OTP                       |  | 120         |      | °C   |
| Threshold Accuracy                        |   | -5   |             | 5    | °C   |
| Delay                                     | From instant when threshold is exceeded until the turn-off command is generated       |  | 6           |      | µs   |
| <b>Tracking Protection (when Enabled)</b> |   |  |             |      |  |
| Type                                      | Default Programmable  | Disabled Latching/Non-Latching, 130ms period     |             |      |  |
| Threshold                                 | Enabled during output voltage ramping up  |  |             | ±250 | mVDC                                       |
| Threshold Accuracy                        |   | -50  |             | 50   | mVDC                                       |
| Delay                                     | From instant when threshold is exceeded until the turn-off command is generated       |  | 6           |      | µs   |
| <b>Overtemperature Warning</b>            |   |  |             |      |  |
| Threshold                                 | Always enabled, reported in Status register   |  | 120         |      | °C   |
| Threshold Accuracy                        |   | -5   |             | 5    | °C   |
| Hysteresis                                |   |  | 3           |      | °C   |
| Delay                                     | From instant when threshold is exceeded until the warning signal is generated         |  | 6           |      | µs   |
| <b>Power Good Signal (PGOOD pin)</b>      |   |  |             |      |  |
| Logic                                     | V <sub>OUT</sub> is inside the PG window<br>V <sub>OUT</sub> is outside the PG window |  | High<br>Low |      | N/A  |
| Lower Threshold                           | Default Programmable in 5% steps  | 90   | 90          | 95   | %V <sub>O.SET</sub><br>%V <sub>O.SET</sub> |
| Upper Threshold                           |   |  | 110         |      | %V <sub>O.SET</sub>                        |
| Delay                                     | From instant when threshold is exceeded until status of PG signal changes             |  | 6           |      | µs   |
| Threshold Accuracy                        | Measured at V <sub>O.SET</sub> =2.5V  | -2   |             | 2    | %V <sub>O.SET</sub>                        |

<sup>1</sup> Minimum OVP threshold is 1.0V

# ZY7115 15A DC-DC Intelligent POL Data Sheet

## 3V to 13.2V Input • 0.5V to 5.5V Output



### 4.4 Feature Specifications

| Parameter  | Conditions/Description                         | Min                      | Nom  | Max                     | Units            |
|--|--|--------------------------|------|-------------------------|------------------|
| <b>Current Share</b>                                       |  |                          |      |                         |                  |
| Type   |  | Active, Single Line      |      |                         |                  |
| Maximum Number of Modules Connected in Parallel            | $I_{OUT\ MIN} \geq 20\% * I_{OUT\ NOM}$        | 10                       |      |                         |                  |
| Maximum Number of Modules Connected in Parallel            | $I_{OUT\ MIN} = 0$                             | 4                        |      |                         |                  |
| Current Share Accuracy                                     | $I_{OUT\ MIN} \geq 20\% * I_{OUT\ NOM}$        |                          |      | ±20                     | % $I_{OUT}$      |
| <b>Interleave</b>  |  |                          |      |                         |                  |
| Interleave (Phase Shift)                                   | Default<br>Programmable in 11.25° steps        | 0                        | 0    | 348.75                  | Degree<br>degree |
| <b>Sequencing</b>  |  |                          |      |                         |                  |
| Turn ON Delay  | Default<br>Programmable in 1ms steps           | 0                        | 0    | 255                     | ms<br>ms         |
| Turn OFF Delay   | Default<br>Programmable in 1ms steps           | 0                        | 0    | 63                      | ms<br>ms         |
| <b>Tracking</b>  |  |                          |      |                         |                  |
| Turn ON Slew Rate  | Default<br>Programmable in 7 steps             | 0.1                      | 0.1  | 8.33 <sup>1</sup>       | V/ms<br>V/ms     |
| Turn OFF Slew Rate   | Default<br>Programmable in 7 steps             | -0.1                     | -0.1 | -8.33 <sup>1</sup>      | V/ms<br>V/ms     |
| <b>Optimal Voltage Positioning</b>                         |  |                          |      |                         |                  |
| Load Regulation  | Default<br>Programmable in 7 steps             | 0                        | 0    | 6.27                    | mV/A<br>mV/A     |
| <b>Feedback Loop Compensation</b>                          |  |                          |      |                         |                  |
| Zero 1 (Effects phase lead and increases gain in mid-band) | Programmable                                   | 0.05                     |      | 50                      | kHz              |
| Zero 2 (Effects phase lead and increases gain in mid-band) | Programmable                                   | 0.05                     |      | 50                      | kHz              |
| Pole 1 (Integrator Pole, effects loop gain)                | Programmable                                   | 0.05                     |      | 50                      | kHz              |
| Pole 2 (Effects phase lag and limits gain in mid-band)     | Programmable                                   | 1                        |      | 1000                    | kHz              |
| Pole 3 (High frequency low-pass filter to limit PWM noise) | Programmable                                   | 1                        |      | 1000                    | kHz              |
| <b>Monitoring</b>  |  |                          |      |                         |                  |
| Voltage Monitoring Accuracy                                | 1 LSB=22mV                                     | -2% $V_{OUT}$<br>- 1 LSB |      | 2% $V_{OUT}$<br>+ 1 LSB | mV               |
| Current Monitoring Accuracy                                | $20\% * I_{OUT\ NOM} < I_{OUT} < I_{OUT\ NOM}$ | -20                      |      | +20                     | % $I_{OUT}$      |
| Temperature Monitoring Accuracy                            | Junction temperature of POL controller         | -5                       |      | +5                      | °C               |
| <b>Remote Voltage Sense (+VS and -VS pins)</b>             |  |                          |      |                         |                  |
| Voltage Drop Compensation                                  | Between +VS and $V_{OUT}$                      |                          |      | 300                     | mV               |
| Voltage Drop Compensation                                  | Between -VS and PGND                           |                          |      | 100                     | mV               |

<sup>1</sup> Achieving fast slew rates under specific line and load conditions may require feedback loop adjustment

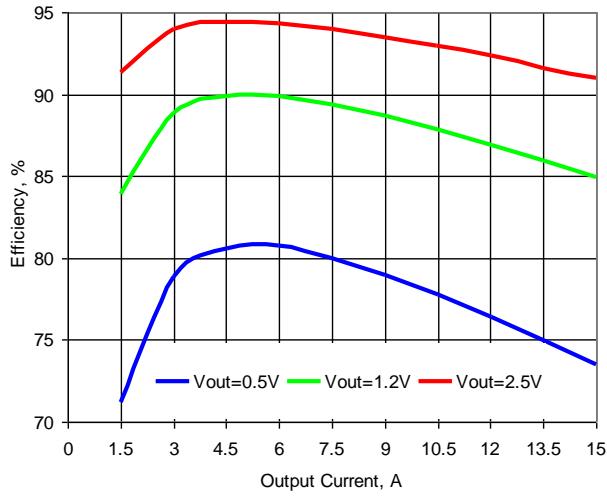


#### 4.5 Signal Specifications

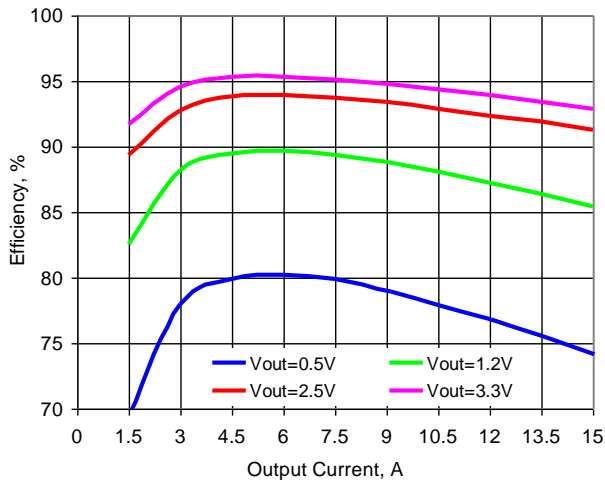
| Parameter                               | Conditions/Description                            | Min        | Nom | Max        | Units            |
|---|---|------------|-----|------------|------------------|
| VDD                                     | Internal supply voltage                           | 3.15       | 3.3 | 3.45       | V                |
| <b>SYNC/DATA Line (SD pin)</b>          |   |            |     |            |                  |
| ViL_sd                                  | LOW level input voltage                           | -0.5       |     | 0.3 x VDD  | V                |
| ViH_sd                                  | HIGH level input voltage                          | 0.75 x VDD |     | VDD + 0.5  | V                |
| Vhyst_sd                                | Hysteresis of input Schmitt trigger               | 0.25 x VDD |     | 0.45 x VDD | V                |
| VoL                                     | LOW level sink current @ 0.5V                     | 14         |     | 60         | mA               |
| Tr_sd                                   | Maximum allowed rise time 10/90%VDD               |            |     | 300        | ns               |
| Cnode_sd                                | Added node capacitance                            |            | 5   | 10         | pF               |
| Ipu_sd                                  | Pull-up current source at Vsd=0V                  | 0.3        |     | 1.0        | mA               |
| Freq_sd                                 | Clock frequency of external SD line               | 475        |     | 525        | kHz              |
| Tsynq                                   | Sync pulse duration                               | 22         |     | 28         | % of clock cycle |
| T0                                      | Data=0 pulse duration                             | 72         |     | 78         | % of clock cycle |
| <b>Inputs: ADDR0...ADDR4, EN, IM</b>    |   |            |     |            |                  |
| ViL_x                                   | LOW level input voltage                           | -0.5       |     | 0.3 x VDD  | V                |
| ViH_x                                   | HIGH level input voltage                          | 0.7 x VDD  |     | VDD+0.5    | V                |
| Vhyst_x                                 | Hysteresis of input Schmitt trigger               | 0.1 x VDD  |     | 0.3 x VDD  | V                |
| RdnL_ADDR                               | External pull down resistance<br>ADDRX forced low |            |     | 10         | kOhm             |
| <b>Power Good and OK Inputs/Outputs</b> |   |            |     |            |                  |
| Iup_PG                                  | Pull-up current source input forced low PG        | 25         |     | 110        | μA               |
| Iup_OK                                  | Pull-up current source input forced low OK        | 175        |     | 725        | μA               |
| ViL_x                                   | LOW level input voltage                           | -0.5       |     | 0.3 x VDD  | V                |
| ViH_x                                   | HIGH level input voltage                          | 0.7 x VDD  |     | VDD+0.5    | V                |
| Vhyst_x                                 | Hysteresis of input Schmitt trigger               | 0.1 x VDD  |     | 0.3 x VDD  | V                |
| IoL                                     | LOW level sink current at 0.5V                    | 4          |     | 20         | mA               |
| <b>Current Share Bus (CS pin)</b>       |   |            |     |            |                  |
| Iup_CS                                  | Pull-up current source at VCS = 0V                | 0.84       |     | 3.1        | mA               |
| ViL_CS                                  | LOW level input voltage                           | -0.5       |     | 0.3 x VDD  | V                |
| ViH_CS                                  | HIGH level input voltage                          | 0.75 x VDD |     | VDD+0.5    | V                |
| Vhyst_CS                                | Hysteresis of input Schmitt trigger               | 0.25 x VDD |     | 0.45 x VDD | V                |
| IoL                                     | LOW level sink current at 0.5V                    | 14         |     | 60         | mA               |
| Tr_CS                                   | Maximum allowed rise time 10/90% VDD              |            |     | 100        | ns               |

**5. Typical Performance Characteristics**

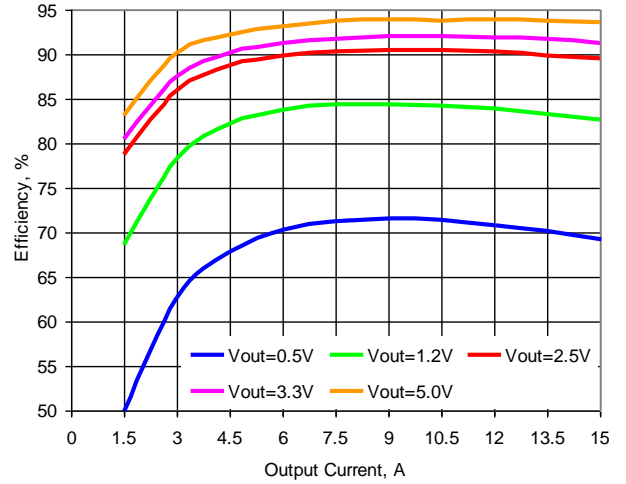
**5.1 Efficiency Curves**



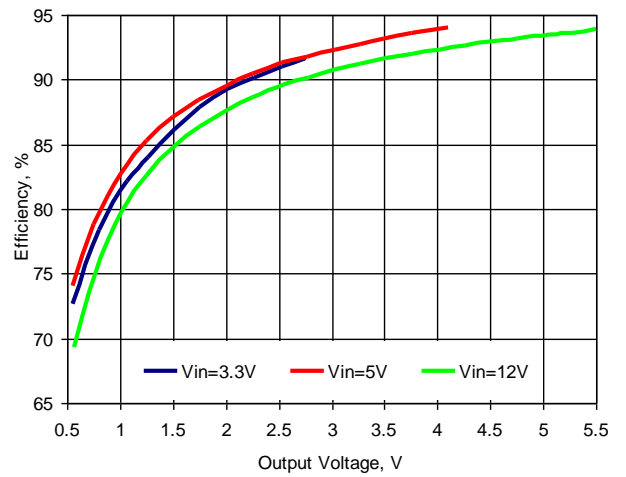
**Figure 2. Efficiency vs. Load. Vin=3.3V, Fsw=500kHz**



**Figure 3. Efficiency vs. Load. Vin=5V, Fsw=500kHz**



**Figure 4. Efficiency vs. Load. Vin=12V, Fsw=500kHz**



**Figure 5. Efficiency vs. Output Voltage, Iout=15A, Fsw=500kHz**

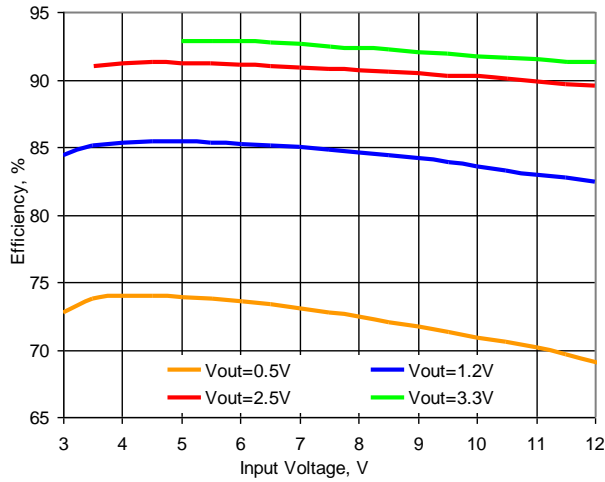


Figure 6. Efficiency vs. Input Voltage. Iout=15A, Fsw=500kHz

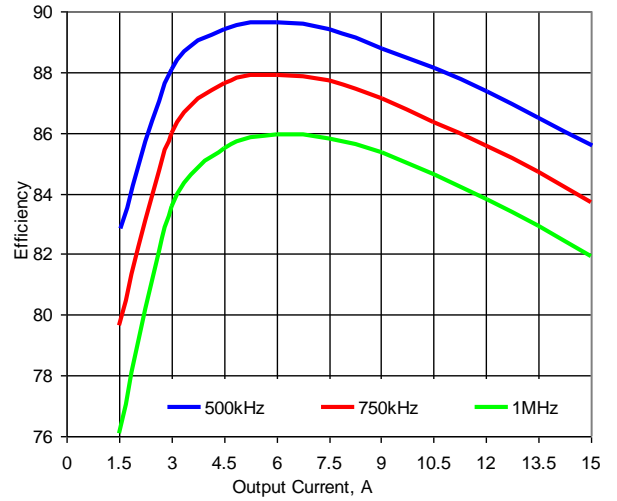


Figure 8. Efficiency vs. Load. Vin=5V, Vout=1.2V

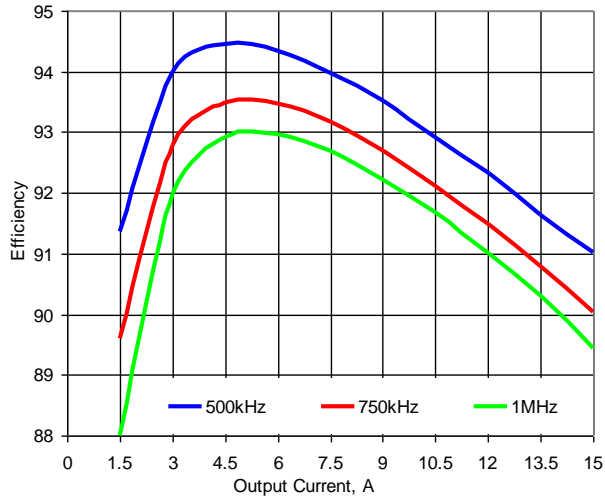


Figure 7. Efficiency vs. Load. Vin=3.3V, Vout=2.5V

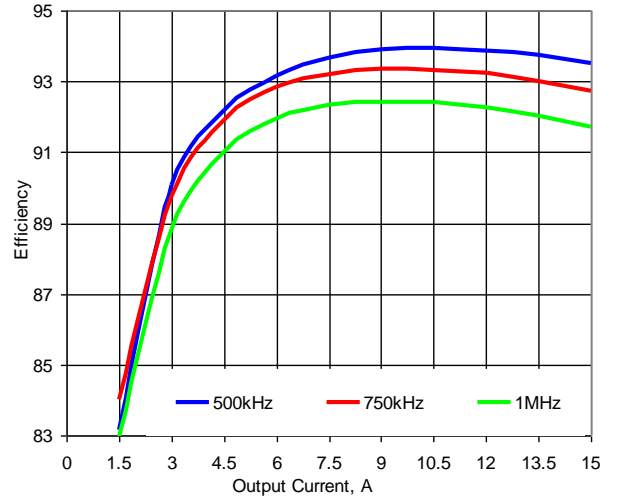


Figure 9. Efficiency vs. Load. Vin=12V, Vout=5V



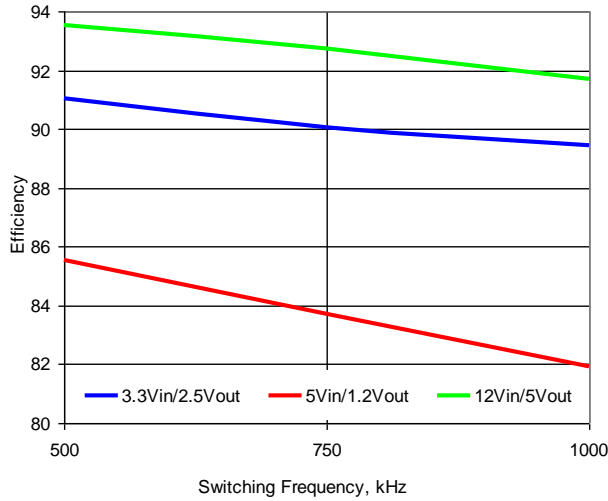


Figure 10. Efficiency vs. Switching Frequency. Iout=15A

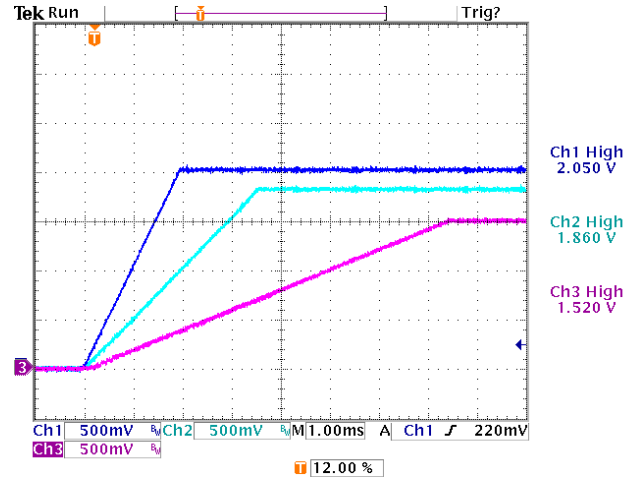


Figure 12. Turn-On with Different Rising Slew Rates. Rising Slew Rates are Programmed as follows: V1-1V/ms, V2-0.5V/ms, V3-0.2V/ms. Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

## 5.2 Turn-On Characteristics

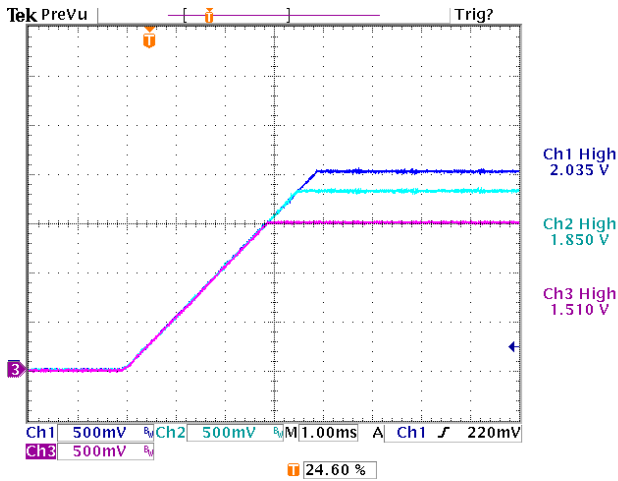


Figure 11. Tracking Turn-On. Rising Slew Rate is Programmed at 0.5V/ms. Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

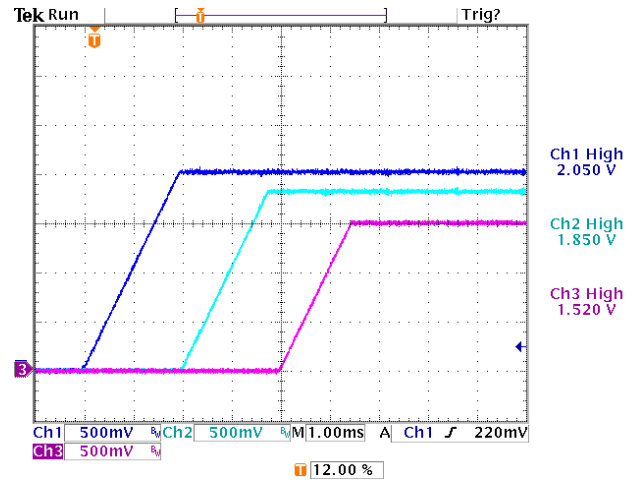


Figure 13. Sequenced Turn-On. Rising Slew Rate is Programmed at 1V/ms. V2 Delay is 2ms, V3 delay is 4ms. Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3



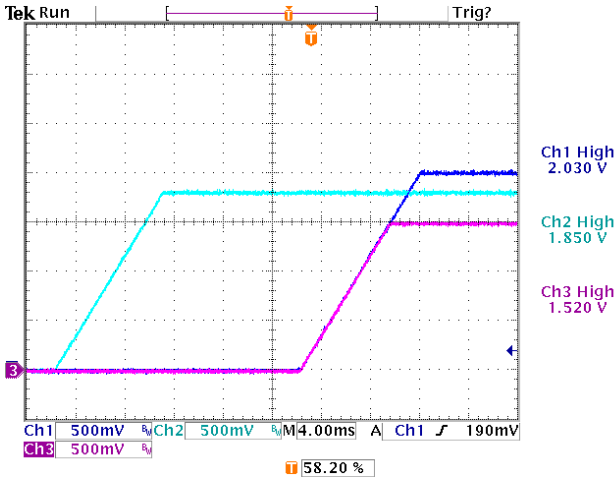


Figure 14. Turn On with Sequencing and Tracking. Rising Slew Rate Programmed at 0.2V/ms, V1 and V3 delays are programmed at 20ms. Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

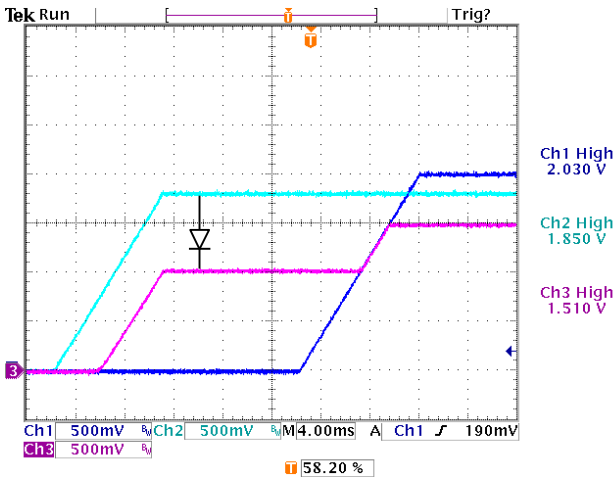


Figure 15. Turn On into Prebiased Load. V3 is Prebiased by V2 via a Diode. Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

### 5.3 Turn-Off Characteristics

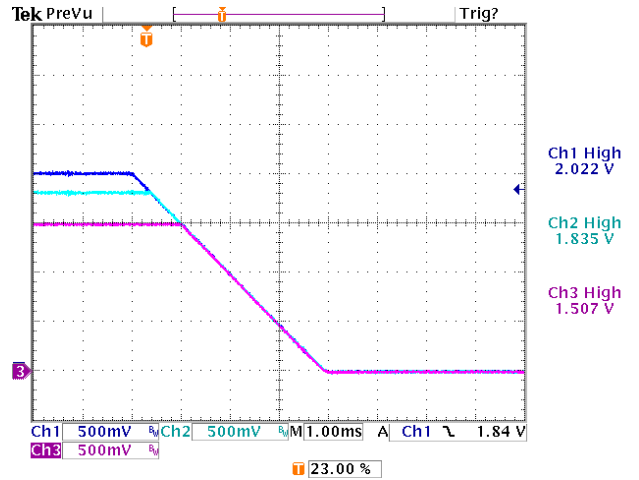


Figure 16. Tracking Turn-Off. Falling Slew Rate is Programmed at 0.5V/ms. Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3

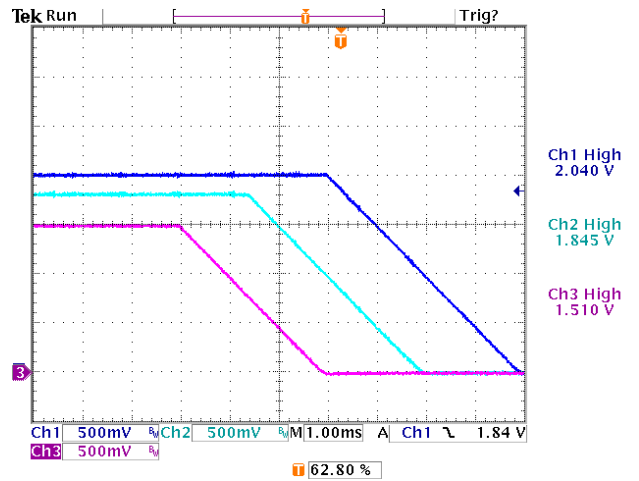


Figure 17. Turn-Off with Tracking and Sequencing. Falling Slew Rate is Programmed at 0.5V/ms. Vin=12V, Ch1 – V1, Ch2 – V2, Ch3 – V3





5.4 Transient Response

The pictures below show the deviation of the output voltage in response to the 50-100-50% step load at 2.5A/μs. In all tests the POL converters were operating at 1MHz and had 6x47μF ceramic capacitors connected across the output pins. Bandwidth of the feedback loop was programmed for faster transient response.

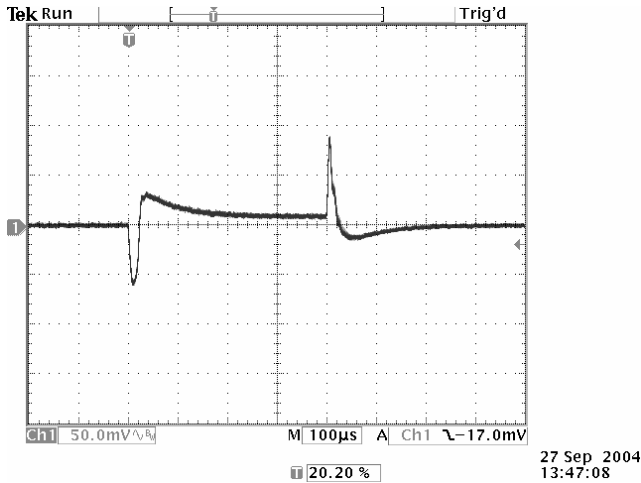


Figure 18. Vin=12V, Vout=1V. Bandwidth is 40kHz

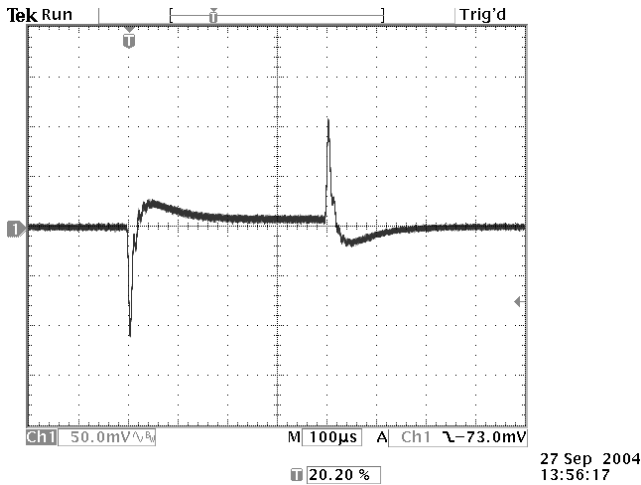


Figure 19. Vin=12V, Vout=5V. Bandwidth is 40kHz

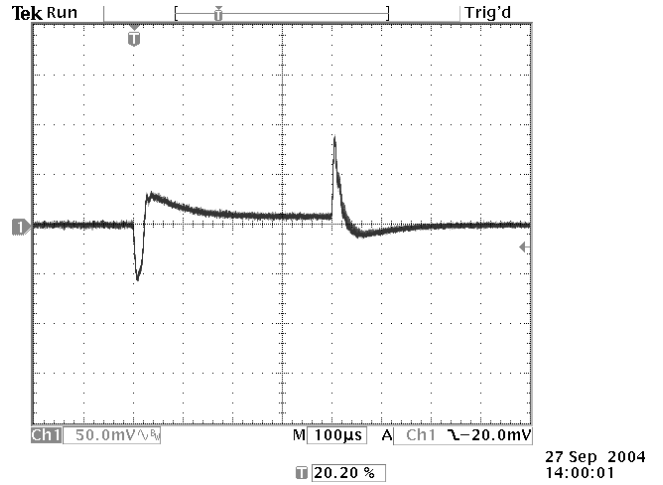


Figure 20. Vin=5V, Vout=1V. Bandwidth is 40kHz

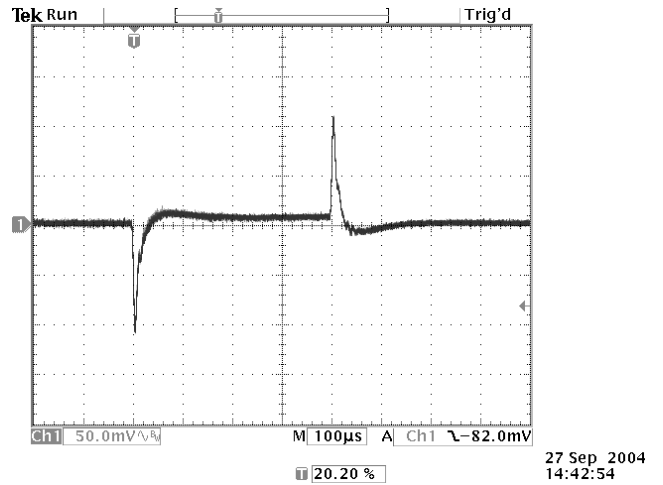


Figure 21. Vin=5V, Vout=2.5V. Bandwidth is 40kHz

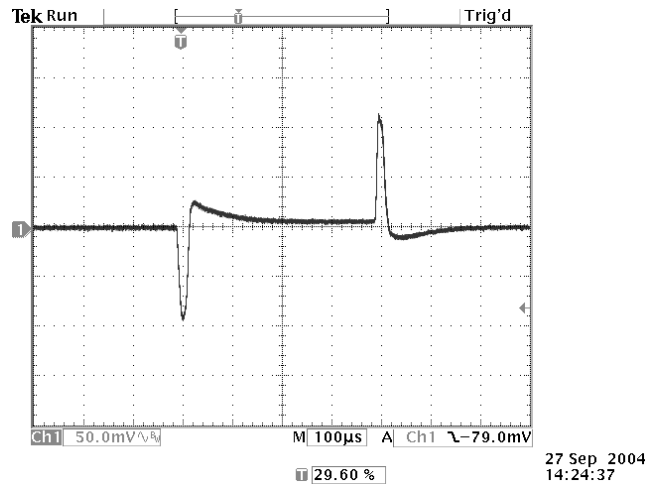


Figure 22. Vin=3V, Vout=1V. Bandwidth is 30kHz



**5.5 Thermal Derating Curves**

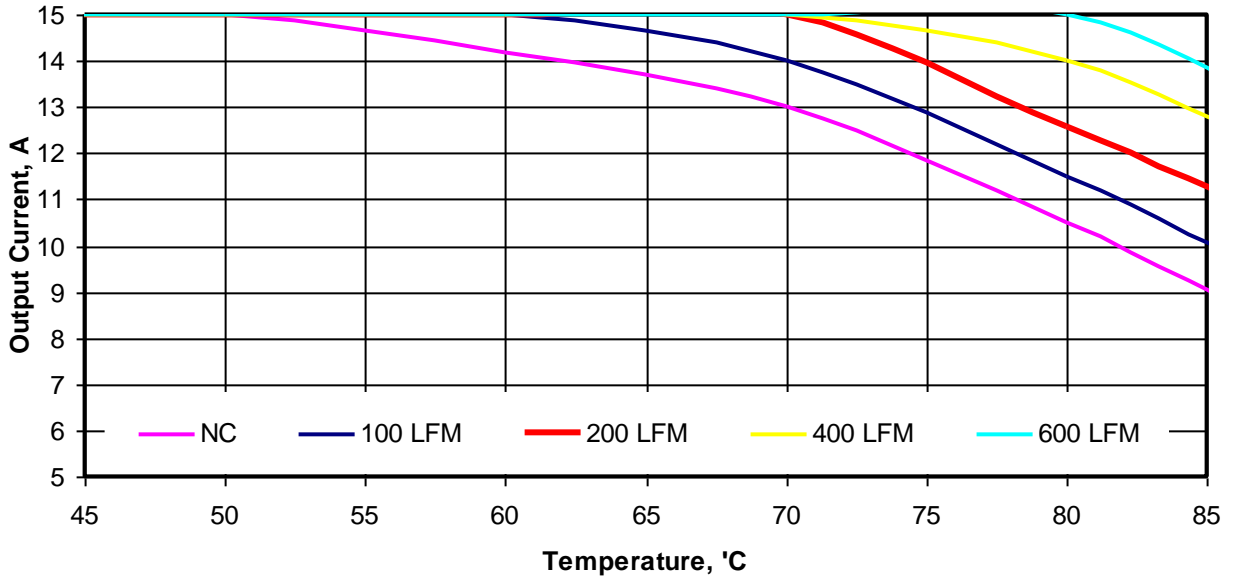


Figure 23. Thermal Derating Curves. Vin=13.2V, Vout=2.5V, Fsw=500kHz

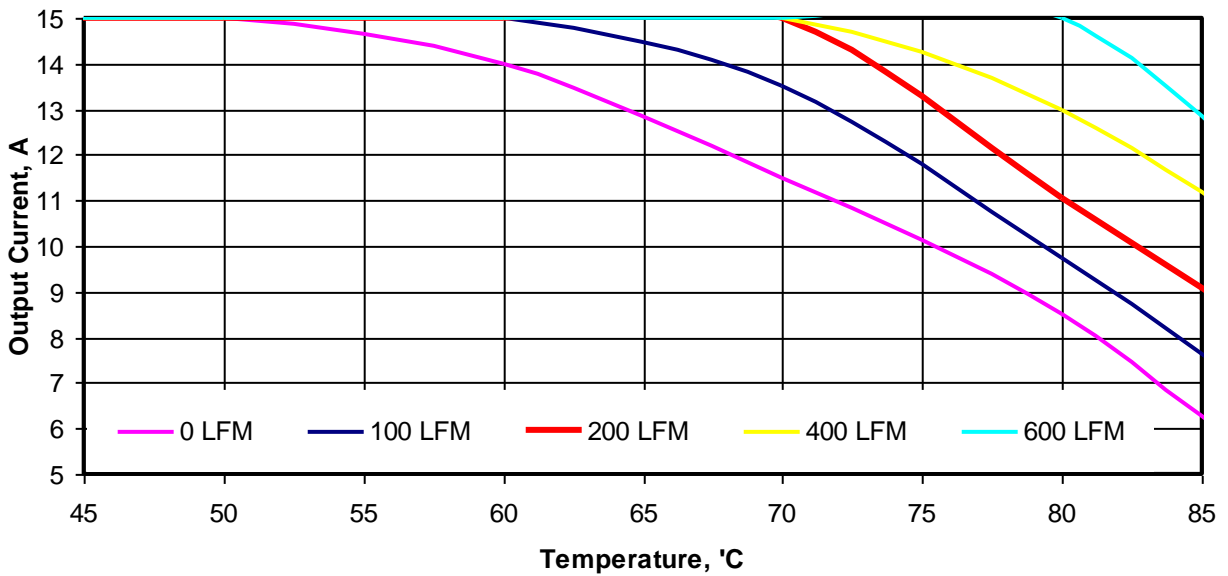


Figure 24. Thermal Derating Curves. Vin=13.2V, Vout=5V, Fsw=500kHz

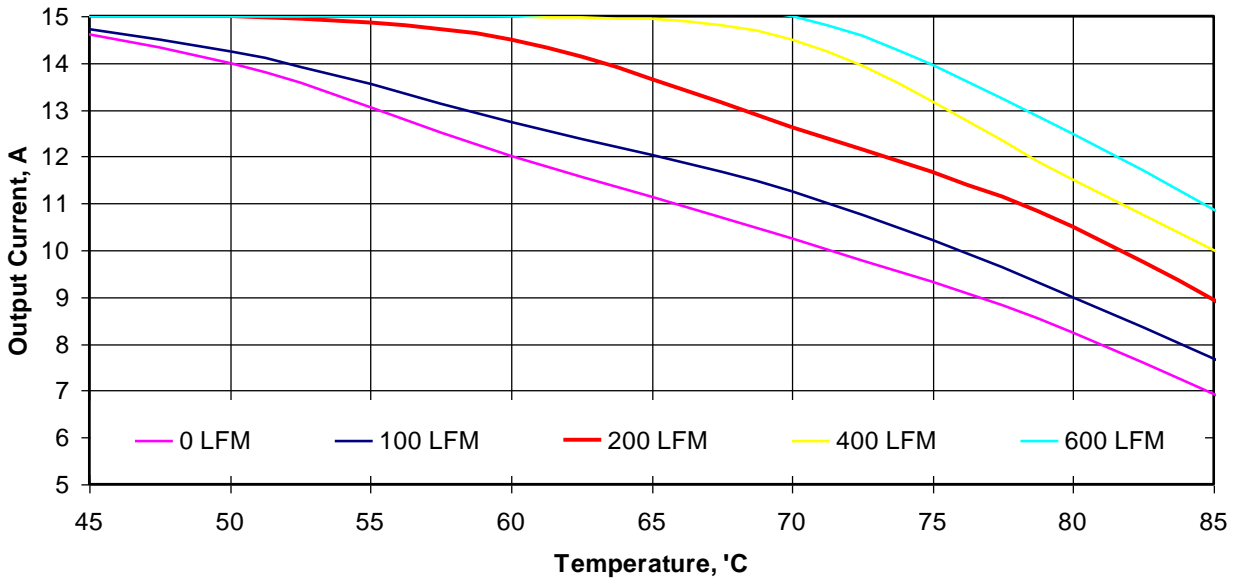


Figure 25. Thermal Derating Curves.  $V_{in}=13.2V$ ,  $V_{out}=5V$ ,  $F_{sw}=1,000kHz$

## 6. Typical Application

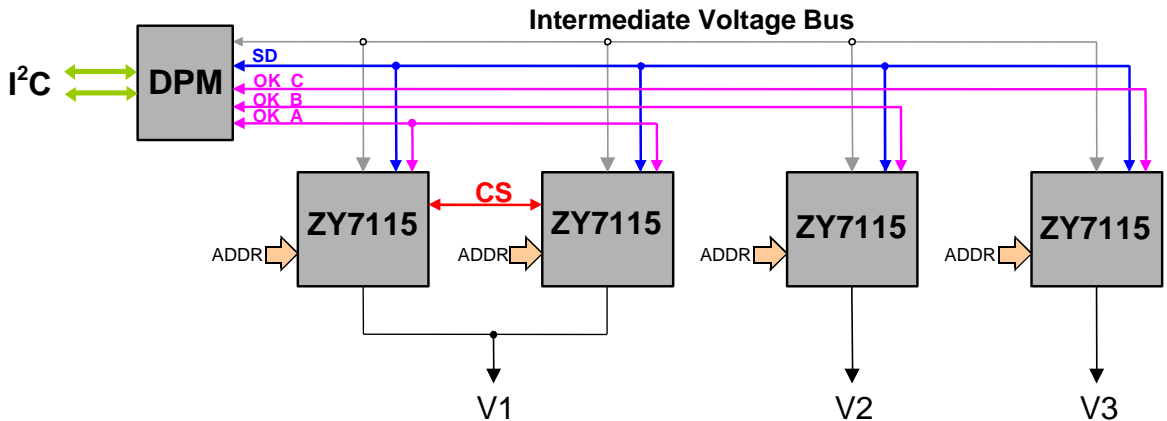


Figure 26. Block Diagram of Typical Multiple Output Application with Digital Power Manager and I<sup>2</sup>C Interface

The block diagram of a typical application of ZY7115 point-of-load converters (POL) is shown in Figure 26. The system includes multiple POLs and a ZM7300 series Digital Power Manager (DPM). All POLs are connected to the DPM and to each other via a single-wire SD (sync/data) line. The line provides synchronization of all POLs to the master clock generated by the DPM and simultaneously performs bidirectional data transfer between POLs and the DPM. Each POL has a unique 5-bit address programmed by grounding respective address pins. To enable the current share, CS pins of POLs connected in parallel are linked together.

There are three groups of POLs in the application, groups A, B, and group C. A group is defined as a number of POLs interconnected via OK pins. Grouping of POLs enables users to program, control, and monitor multiple POLs simultaneously and execute advanced fault management schemes.

The complete schematic of the application is shown in Figure 27.

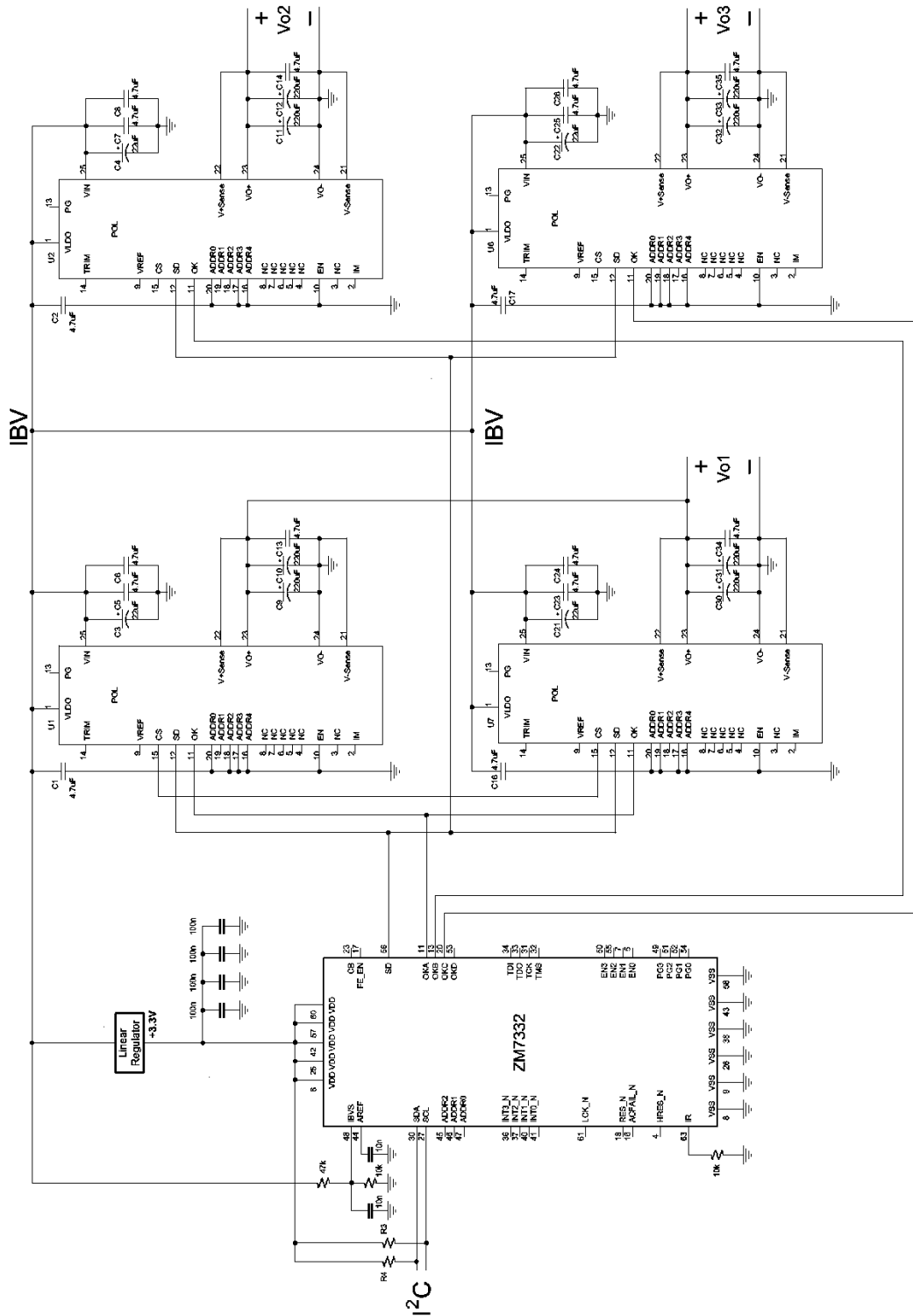


Figure 27. Complete Schematic of the Application Shown in Figure 26. Intermediate Bus Voltage is from 4.75V to 13.2V.

# ZY7115 15A DC-DC Intelligent POL Data Sheet

## 3V to 13.2V Input • 0.5V to 5.5V Output



### 7. Pin Assignments and Description

| Pin Name | Pin Number | Pin Type | Buffer Type | Pin Description        | Notes   |
|----------|------------|----------|-------------|------------------------|---|
| VLDO     | 1          | P        |             | Low Voltage Dropout    | Connect to an external voltage source higher than 4.75V, if $V_{IN} < 4.75V$ . Connect to $V_{IN}$ , if $V_{IN} \geq 4.75V$ |
| IM       | 2          |          |             | Not Used               | Leave floating  |
| NC       | 3          |          |             | Not Used               | Leave floating  |
| NC       | 4          |          |             | Not Used               | Leave floating  |
| NC       | 5          |          |             | Not Used               | Leave floating  |
| NC       | 6          |          |             | Not Used               | Leave floating  |
| NC       | 7          |          |             | Not Used               | Leave floating  |
| NC       | 8          |          |             | Not Used               | Leave floating  |
| VREF     | 9          |          |             | Not Used               | Leave floating  |
| EN       | 10         |          |             | Connect to PGND        | Connect to PGND   |
| OK       | 11         | I/O      | PU          | Fault/Status Condition | Connect to OK pin of other Z-POL and/or DPM. Leave floating, if not used  |
| SD       | 12         | I/O      | PU          | Sync/Data Line         | Connect to SD pin of DPM  |
| PGOOD    | 13         | I/O      | PU          | Power Good             |   |
| TRIM     | 14         |          |             | Not Used               | Leave floating  |
| CS       | 15         | I/O      | PU          | Current Share          | Connect to CS pin of other Z-POLs connected in parallel   |
| ADDR4    | 16         | I        | PU          | POL Address Bit 4      | Tie to PGND for 0 or leave floating for 1   |
| ADDR3    | 17         | I        | PU          | POL Address Bit 3      | Tie to PGND for 0 or leave floating for 1   |
| ADDR2    | 18         | I        | PU          | POL Address Bit 2      | Tie to PGND for 0 or leave floating for 1   |
| ADDR1    | 19         | I        | PU          | POL Address Bit 1      | Tie to PGND for 0 or leave floating for 1   |
| ADDR0    | 20         | I        | PU          | POL Address Bit 0      | Tie to PGND for 0 or leave floating for 1   |
| -VS      | 21         | I        | PU          | Negative Voltage Sense | Connect to the negative point close to the load   |
| +VS      | 22         | I        | PU          | Positive Voltage Sense | Connect to the positive point close to the load   |
| VOUT     | 23         | P        |             | Output Voltage         |   |
| PGND     | 24         | P        |             | Power Ground           |   |
| VIN      | 25         | P        |             | Input Voltage          |   |

Legend: I=input, O=output, I/O=input/output, P=power, A=analog, PU=internal pull-up





### 8. Programmable Features

Performance parameters of ZY7115 POL converters can be programmed via the industry standard I<sup>2</sup>C communication bus without replacing any components or rewiring PCB traces. Each parameter has a default value stored in the volatile memory registers detailed in Table 1. The setup registers 00h through 14h are programmed at the system power-up. When the user programs new performance parameters, the values in the registers are overwritten. Upon removal of the input voltage, the default values are restored.

Table 1. ZY7115 Memory Registers

| Register | Content  | Address |
|----------|--|---------|
| PC1      | Protection Configuration 1                               | 00h     |
| PC2      | Protection Configuration 2                               | 01h     |
| PC3      | Protection Configuration 3                               | 02h     |
| DON      | Turn-On Delay  | 05h     |
| DOF      | Turn-Off Delay   | 06h     |
| TC       | Tracking Configuration                                   | 03h     |
| INT      | Interleave Configuration and Frequency Selection         | 04h     |
| RUN      | RUN Register   | 15h     |
| ST       | Status Register  | 16h     |
| VOS      | Output Voltage Setpoint                                  | 07h     |
| CLS      | Current Limit Setpoint                                   | 08h     |
| DCL      | Duty Cycle Limit   | 09h     |
| B1       | Dig Controller Denominator $z^{-1}$ Coefficient          | 0Ah     |
| B2       | Dig Controller Denominator $z^{-2}$ Coefficient          | 0Bh     |
| B3       | Dig Controller Denominator $z^{-3}$ Coefficient          | 0Ch     |
| C0L      | Dig Controller Numerator $z^0$ Coefficient, Low Byte     | 0Dh     |
| C0H      | Dig Controller Numerator $z^0$ Coefficient, High Byte    | 0Eh     |
| C1L      | Dig Controller Numerator $z^{-1}$ Coefficient, Low Byte  | 0Fh     |
| C1H      | Dig Controller Numerator $z^{-1}$ Coefficient, High Byte | 10h     |
| C2L      | Dig Controller Numerator $z^{-2}$ Coefficient, Low Byte  | 11h     |
| C2H      | Dig Controller Numerator $z^{-2}$ Coefficient, High Byte | 12h     |
| C3L      | Dig Controller Numerator $z^{-3}$ Coefficient, High Byte | 13h     |
| C3H      | Dig Controller Numerator $z^{-3}$ Coefficient, Low Byte  | 14h     |
| VOM      | Output Voltage Monitoring                                | 17h     |
| IOM      | Output Current Monitoring                                | 18h     |
| TMP      | Temperature Monitoring                                   | 19h     |

ZY7115 converters can be programmed using the Graphical User Interface or directly via the I<sup>2</sup>C bus by using high and low level commands as described in the "ZM7300 Digital Power Manager Programming Manual".

ZY7115 parameters can be reprogrammed at any time during the system operation and service except for the digital filter coefficients, the switching frequency and the duty cycle limit, that can only be changed when the POL is turned off.

### 8.1 Output Voltage

The output voltage can be programmed in the POL Configure Output window shown in the Figure 28 or directly via the I<sup>2</sup>C bus by writing into the VOS register shown in Figure 29.

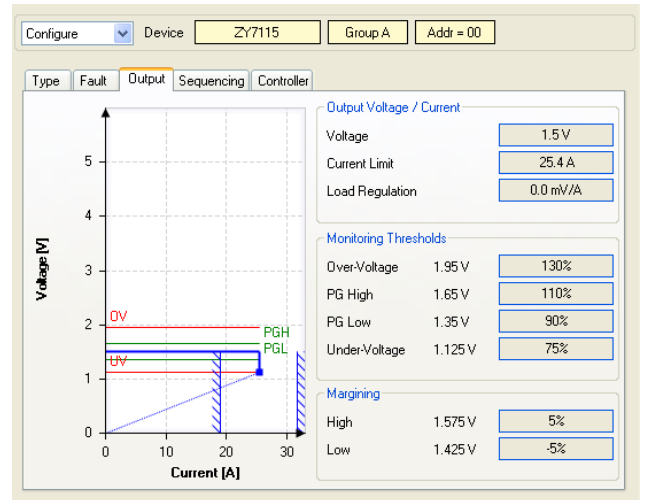


Figure 28. POL Configure Output Window

| R/W-0   | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
|---|-------|-------|-------|-------|-------|-------|-------|
| VOS7  | VOS6  | VOS5  | VOS4  | VOS3  | VOS2  | VOS1  | VOS0  |
| Bit 7   |       |       |       |       |       |       | Bit 0 |
| Bit 7:0 <b>VOS[7:0]</b> , Output voltage setting<br>00h: corresponds to 0.5000V<br>01h: corresponds to 0.5125V<br>...<br>77h: corresponds to 1.9875V<br>78h: corresponds to 2.0000V<br>79h: corresponds to 2.025V<br>...<br>F9h: corresponds to 5.225V<br>FAh: corresponds to 5.250V<br>FBh: corresponds to 5.300V<br>...<br>FFh: corresponds to 5.500V |       |       |       |       |       |       |       |
| R = Readable bit<br>W = Writable bit<br>U = Unimplemented bit, read as '0'<br>- n = Value at POR reset  |       |       |       |       |       |       |       |

Figure 29. Output Voltage Setpoint Register VOS





### 8.1.1 Output Voltage Setpoint

The output voltage programming range is from 0.5V to 5.5V. Within this range, there are 256 predefined voltage setpoints. To improve resolution of the output voltage settings, the voltage range is divided into three sub-ranges as shown in Table 2.

Table 2. Output Voltage Adjustment Resolution

| V <sub>OUT</sub> MIN, V | V <sub>OUT</sub> MAX, V | Resolution, mV |
|-------------------------|-------------------------|----------------|
| 0.500                   | 2.000                   | 12.5           |
| 2.025                   | 5.25                    | 25             |
| 5.3                     | 5.5                     | 50             |

### 8.1.2 Output Voltage Margining

If the output voltage needs to be varied by a certain percentage, the margining function can be utilized. The margining can be programmed in the POL Configure Output window or directly via the I<sup>2</sup>C bus using high level commands as described in the "DPM Programming Manual".

In order to properly margin POLs that are connected in parallel, the POLs must be members of one of the Parallel Buses. Refer to the DPM Configure Devices window shown in Figure 56.

### 8.1.3 Optimal Voltage Positioning

Optimal voltage positioning increases the voltage regulation window by properly positioning the output voltage setpoint. Positioning is determined by the load regulation that can be programmed in the POL Configure Output window shown in Figure 28 or directly via the I<sup>2</sup>C bus by writing into the CLS register shown in Figure 39.

Figure 30 illustrates optimal voltage positioning concept. If no load regulation is programmed, the headroom (voltage differential between the output voltage setpoint and a regulation limit) is approximately half of the voltage regulation window. When load regulation is programmed, the output voltage will decrease as the output current increases, so the VI characteristic will have a negative slope. Therefore, by properly selecting the operating point, it is possible to increase the headroom as shown in the picture.

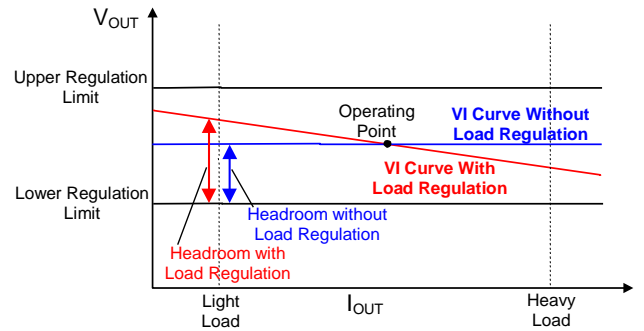


Figure 30. Concept of Optimal Voltage Positioning

Increased headroom allows tolerating larger voltage deviations. For example, the step load change from light to heavy load will cause the output voltage to drop. If the optimal voltage positioning is utilized, the output voltage will stay within the regulation window. Otherwise, the output voltage will drop below the lower regulation limit. To compensate for the voltage drop external output capacitance will need to be added, thus increasing cost and complexity of the system.

The effect of optimal voltage positioning is shown in Figure 31 and Figure 32. In this case, switching output load causes large peak-to-peak deviation of the output voltage. By programming load regulation, the peak to peak deviation is dramatically reduced.

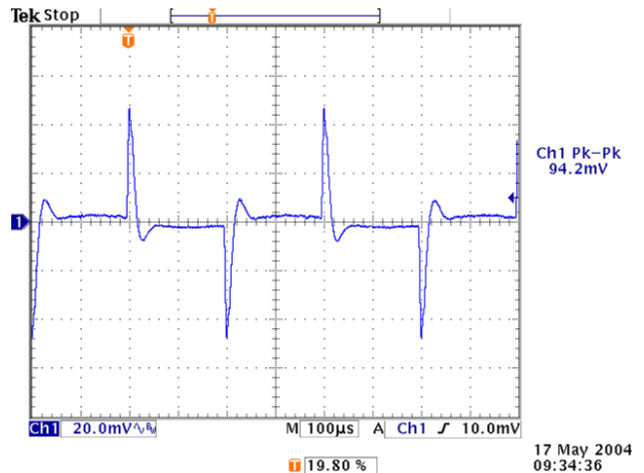


Figure 31. Transient Response without Optimal Voltage Positioning



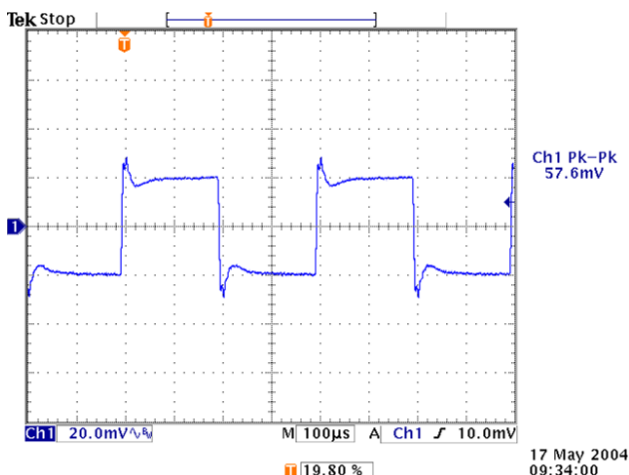


Figure 32. Transient Response with Optimal Voltage Positioning

## 8.2 Sequencing and Tracking

Turn-on delay, turn-off delay, and rising and falling output voltage slew rates can be programmed in the POL Configure Sequencing window shown in Figure 33 or directly via the I<sup>2</sup>C bus by writing into the DON, DOF, and TC registers, respectively. The registers are shown in Figure 34, Figure 35, and Figure 37.

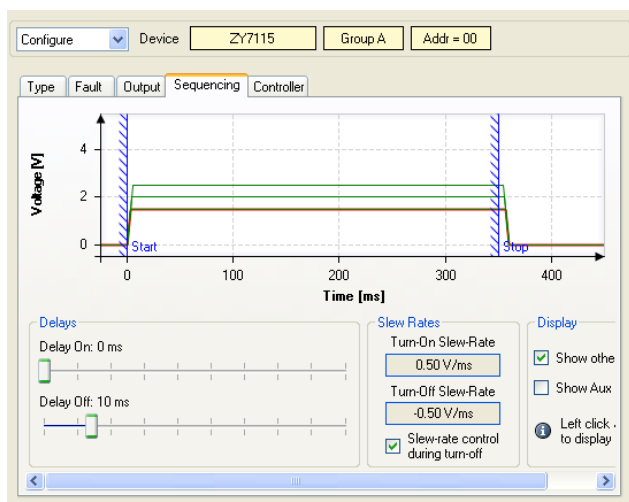


Figure 33. POL Configure Sequencing Window

### 8.2.1 Turn-On Delay

Turn-on delay is defined as an interval from the application of the Turn-On command until the output voltage starts ramping up.

|  |       |       |       |       |       |       |       |
|--|-------|-------|-------|-------|-------|-------|-------|
| R/W-0  | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| DON7   | DON6  | DON5  | DON4  | DON3  | DON2  | DON1  | DON0  |
| Bit 7  |       |       |       |       |       |       | Bit 0 |
| Bit 7:0 <b>DON[7:0]</b> : Turn-on delay time                       |       |       |       |       |       |       |       |
| 00h: corresponds to 0ms delay after turn-on command has occurred   |       |       |       |       |       |       |       |
| ...  |       |       |       |       |       |       |       |
| FFh: corresponds to 255ms delay after turn-on command has occurred |       |       |       |       |       |       |       |

Figure 34. Turn-On Delay Register DON

### 8.2.2 Turn-Off Delay

|  |     |       |       |       |       |       |       |
|--|-----|-------|-------|-------|-------|-------|-------|
| U  | U   | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-0 |
| ---  | --- | DOF5  | DOF4  | DOF3  | DOF2  | DOF1  | DOF0  |
| Bit 7  |     |       |       |       |       |       | Bit 0 |
| Bit 7:6 <b>Unimplemented</b> , read as '0'                         |     |       |       |       |       |       |       |
| Bit 5:0 <b>DOF[5:0]</b> : Turn-off delay time                      |     |       |       |       |       |       |       |
| 00h: corresponds to 0ms delay after turn-off command has occurred  |     |       |       |       |       |       |       |
| ...  |     |       |       |       |       |       |       |
| 3Fh: corresponds to 63ms delay after turn-off command has occurred |     |       |       |       |       |       |       |

Figure 35. Turn-Off Delay Register DOF

Turn-off delay is defined as an interval from the application of the Turn-Off command until the output voltage reaches zero (if the falling slew rate is programmed) or until both high side and low side switches are turned off (if the slew rate is not programmed). Therefore, for the slew rate controlled turn-off the ramp-down time is included in the turn-off delay as shown in Figure 36.

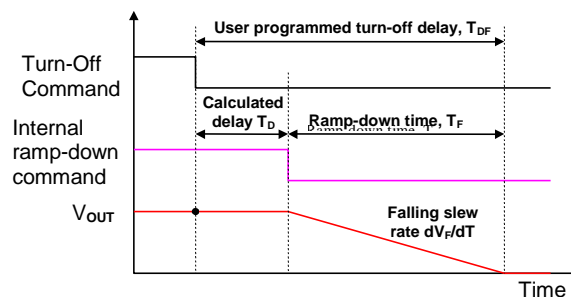


Figure 36. Relationship between Turn-Off Delay and Falling Slew Rate

As it can be seen from the figure, the internally calculated delay  $T_D$  is determined by the equation below.

$$T_D = T_{DF} - \frac{V_{OUT}}{dV_F/dT}$$

For proper operation  $T_D$  shall be greater than zero. The appropriate value of the turn-off delay needs to be programmed to satisfy the condition.





If the falling slew rate control is not utilized, the turn-off delay only determines an interval from the application of the Turn-Off command until both high side and low side switches are turned off. In this case, the output voltage ramp-down process is determined by load parameters.

### 8.2.3 Rising and Falling Slew Rates

The output voltage tracking is accomplished by programming the rising and falling slew rates of the output voltage. To achieve programmed slew rates, the output voltage is being changed in 12.5mV steps where duration of each step determines the slew rate. For example, ramping up a 1.0V output with a slew rate of 0.5V/ms will require 80 steps duration of 25µs each.

Duration of each voltage step is calculated by dividing the master clock frequency generated by the DPM. Since all POLs in the system are synchronized to the master clock, the matching of voltage slew rates of different outputs is very accurate as it can be seen in Figure 11 and Figure 16.

During the turn on process, a POL not only delivers current required by the load ( $I_{LOAD}$ ), but also charges the load capacitance. The charging current can be determined from the equation below:

$$I_{CHG} = C_{LOAD} \times \frac{dV_R}{dt}$$

Where,  $C_{LOAD}$  is load capacitance,  $dV_R/dt$  is rising voltage slew rate, and  $I_{CHG}$  is charging current.

When selecting the rising slew rate, a user needs to ensure that

$$I_{LOAD} + I_{CHG} < I_{OCP}$$

Where  $I_{OCP}$  is the overcurrent protection threshold of the ZY7115. If the condition is not met, then the overcurrent protection will be triggered during the turn-on process. To avoid this,  $dV_R/dt$  and the overcurrent protection threshold should be programmed to meet the condition above.

| U       | R/W-0  | R/W-0 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|---------|--|-------|-------|-------|-------|-------|-------|
| ---     | R2   | R1    | R0    | SC    | F2    | F1    | F0    |
| Bit 7   |  |       |       | Bit 0 |       |       |       |
| Bit 7   | <b>Unimplemented</b> , read as '0'   |       |       |       |       |       |       |
| Bit 6:4 | <b>R[2:0]</b> : Value of $V_o$ rising slope<br>0: corresponds to 0.1V/ms (default)<br>1: corresponds to 0.2V/ms<br>2: corresponds to 0.5V/ms<br>3: corresponds to 1.0V/ms<br>4: corresponds to 2.0V/ms<br>5: corresponds to 5.0V/ms<br>6: corresponds to 8.3V/ms<br>7: corresponds to 8.3V/ms          |       |       |       |       |       |       |
| Bit 3   | <b>SC</b> , Slew rate control at turn-off<br>0: Slew rate control is disabled<br>1: Slew rate control is enabled   |       |       |       |       |       |       |
| Bit 2:0 | <b>F[2:0]</b> : Value of $V_o$ falling slope<br>0: corresponds to -0.1V/ms (default)<br>1: corresponds to -0.2V/ms<br>2: corresponds to -0.5V/ms<br>3: corresponds to -1.0V/ms<br>4: corresponds to -2.0V/ms<br>5: corresponds to -5.0V/ms<br>6: corresponds to -8.3V/ms<br>7: corresponds to -8.3V/ms |       |       |       |       |       |       |

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n = Value at POR reset

Figure 37. Tracking Configuration Register TC

### 8.3 Protections

ZY7115 Series converters have a comprehensive set of programmable protections. The set includes the output over- and undervoltage protections, overcurrent protection, overtemperature protection, tracking protection, overtemperature warning, and Power Good signal. Status of protections is stored in the ST register shown in Figure 38.

| R-1  | R-0                               | R-1 | R-1 | R-1   | R-1 | R-1 | R-1 |
|--|-----------------------------------|-----|-----|-------|-----|-----|-----|
| TP   | PG                                | TR  | OT  | OC    | UV  | OV  | PV  |
| Bit 7  |                                   |     |     | Bit 0 |     |     |     |
| Bit 7  | <b>TP</b> : Temperature Warning   |     |     |       |     |     |     |
| Bit 6  | <b>PG</b> : Power Good Warning    |     |     |       |     |     |     |
| Bit 5  | <b>TR</b> : Tracking Fault        |     |     |       |     |     |     |
| Bit 4  | <b>OT</b> : Overtemperature Fault |     |     |       |     |     |     |
| Bit 3  | <b>OC</b> : Overcurrent Fault     |     |     |       |     |     |     |
| Bit 2  | <b>UV</b> : Undervoltage Fault    |     |     |       |     |     |     |
| Bit 1  | <b>OV</b> : Overvoltage Error     |     |     |       |     |     |     |
| Bit 0  | <b>PV</b> : Phase Voltage Error   |     |     |       |     |     |     |
| <b>Note:</b><br>- An activated warning/fault/error is encoded as '0' |                                   |     |     |       |     |     |     |

R = Readable bit  
W = Writable bit  
U = Unimplemented bit, read as '0'  
- n = Value at POR reset

Figure 38. Protection Status Register ST

Thresholds of overcurrent, over- and undervoltage protections, and Power Good limits can be programmed in the POL Configure Output window or directly via the I<sup>2</sup>C bus by writing into the CLS and PC2 registers shown in Figure 39 and Figure 40.





| R/W-0  | R/W-0 | R/W-0 | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-1 |
|--|-------|-------|-------|-------|-------|-------|-------|
| LR2  | LR1   | LR0   | TCE   | CLS3  | CLS2  | CLS1  | CLS0  |
| Bit 7  |       |       |       | Bit 0 |       |       |       |
| <p>Bit 7:5 <b>LR[2:0]</b>: Load regulation configuration<br/>                     000: 0 V/A/Ohm<br/>                     001: 0.39 V/A/Ohm<br/>                     010: 0.78 V/A/Ohm<br/>                     011: 1.18 V/A/Ohm<br/>                     100: 1.57 V/A/Ohm<br/>                     101: 1.96 V/A/Ohm<br/>                     110: 2.35 V/A/Ohm<br/>                     111: 2.75 V/A/Ohm</p> <p>Bit 4 <b>TCE</b>: Temperature compensation enable<br/>                     0: disabled<br/>                     1: enabled</p> <p>Bit 3:0 <b>CLS[3:0]</b>: Current limit setting<br/>                     0h: corresponds to 37%<br/>                     1h: corresponds to 47%<br/>                     ...<br/>                     Bh: corresponds to 140%<br/>                     Values higher than Bh are translated to Bh (140%)</p> |       |       |       |       |       |       |       |
| <p>R = Readable bit<br/>                     W = Writable bit<br/>                     U = Unimplemented bit, read as '0'<br/>                     - n = Value at POR reset</p>  |       |       |       |       |       |       |       |

Figure 39. Current Limit Setpoint Register CLS

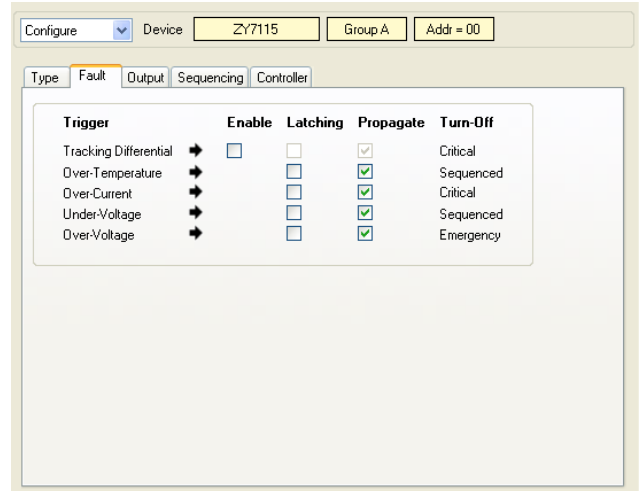


Figure 41. POL Configure Fault Window

| U  | U   | U   | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|--|-----|-----|-------|-------|-------|-------|-------|
| ---  | --- | --- | PGLL  | OVPL1 | OVPL0 | UVPL1 | UVPL0 |
| Bit 7  |     |     |       | Bit 0 |       |       |       |
| <p>Bit 7:5 <b>Unimplemented</b>, read as '0'</p> <p>Bit 4 <b>PGLL</b>: Set Power Good Low Level<br/>                     1 = 95% of Vo<br/>                     0 = 90% of Vo (Default)</p> <p>Bit 3:2 <b>OVPL[1:0]</b>: Set Over Voltage Protection Level<br/>                     00 = 110% of Vo<br/>                     01 = 120% of Vo<br/>                     10 = 130% of Vo (Default)<br/>                     11 = 130% of Vo</p> <p>Bit 1:0 <b>UVPL[1:0]</b>: Set Under Voltage Protection Level<br/>                     00 = 75% of Vo (Default)<br/>                     01 = 80% of Vo<br/>                     10 = 85% of Vo</p> |     |     |       |       |       |       |       |
| <p>R = Readable bit<br/>                     W = Writable bit<br/>                     U = Unimplemented bit, read as '0'<br/>                     - n = Value at POR reset</p>  |     |     |       |       |       |       |       |

Figure 40. Protection Configuration Register PC2

Note that the overvoltage and undervoltage protection thresholds and Power Good limits are defined as percentages of the output voltage. Therefore, the absolute levels of the thresholds change when the output voltage setpoint is changed either by output voltage adjustment or by margining.

In addition, a user can change type of protections (latching or non-latching) or disable certain protections. These settings are programmed in the DPM Configure Fault window shown in Figure 41 or directly via the I<sup>2</sup>C by writing into the PC1 register shown in Figure 42.

| R/W-0   | R/W-1 | R/W-0 | R/W-0 | R/W-0 | R/W-0 | R/W-1 | R/W-1 |
|---|-------|-------|-------|-------|-------|-------|-------|
| TRE   | PVE   | TRP   | OTP   | OCPL  | UVP   | OVP   | PVP   |
| Bit 7   |       |       |       | Bit 0 |       |       |       |
| <p>Bit 7 <b>TRE</b>: Tracking fault enable<br/>                     1 = enabled<br/>                     0 = disabled</p> <p>Bit 6 <b>PVE</b>: Phase voltage error enable<br/>                     1 = enabled<br/>                     0 = disabled</p> <p>Bit 5 <b>TRP</b>: Tracking fault protection<br/>                     1 = latching<br/>                     0 = non latching</p> <p>Bit 4 <b>OTP</b>: Overtemperature protection configuration<br/>                     1 = latching<br/>                     0 = non latching</p> <p>Bit 3 <b>OCPL</b>: Overcurrent protection configuration<br/>                     1 = latching<br/>                     0 = non latching</p> <p>Bit 2 <b>UVP</b>: Undervoltage protection configuration<br/>                     1 = latching<br/>                     0 = non latching</p> <p>Bit 1 <b>OVP</b>: Overvoltage protection configuration<br/>                     1 = latching<br/>                     0 = non latching</p> <p>Bit 0 <b>PVP</b>: Phase Voltage Protection<br/>                     1 = latching<br/>                     0 = non latching</p> |       |       |       |       |       |       |       |
| <p>R = Readable bit<br/>                     W = Writable bit<br/>                     U = Unimplemented bit, read as '0'<br/>                     - n = Value at POR reset</p>   |       |       |       |       |       |       |       |

Figure 42. Protection Configuration Register PC1

If the non-latching protection is selected, a POL will attempt to restart every 130ms until the condition that triggered the protection is removed. When restarting, the output voltages follow tracking and sequencing settings.

If the latching type is selected, a POL will turn off and stay off. The POL can be turned on after 130ms, if the condition that caused the fault is removed and the respective bit in the ST register was cleared, or





the Turn On command was recycled, or the input voltage was recycled.

All protections can be classified into three groups based on their effect on system operation: warnings, faults, and errors.

### 8.3.1 Warnings

This group includes Overtemperature Warning and Power Good Signal. The warnings do not turn off POLs but rather generate signals that can be transmitted to a host controller via the I<sup>2</sup>C bus.

#### 8.3.1.1 Overtemperature Warning

The Overtemperature Warning is generated when temperature of the controller exceeds 120°C. The Overtemperature Warning changes the PT bit of the status register ST to 0 and sends the signal to the DPM. Reporting is enabled in the DPM Configure Faults window or directly via the I<sup>2</sup>C by writing into the PC3 register shown in Figure 44. When the temperature falls below 117°C, the PT bit is cleared and the Overtemperature Warning is removed.

#### 8.3.1.2 Power Good

Power Good is an open collector output that is pulled low, if the output voltage is outside of the Power Good window. The window is formed by the Power Good High threshold that is equal to 110% of the output voltage and the Power Good Low threshold that can be programmed at 90 or 95% of the output voltage.

The Power Good protection is only enabled after the output voltage reaches its steady state level. The PG pin is pulled low during transitions of the output voltage from one level to other as shown in Figure 43.

The Power Good Warning pulls the Power Good pin low and changes the PG bit of the status register ST to 0. It sends the signal to the DPM, if the reporting is enabled. When the output voltage returns within the Power Good window, the PG pin is pulled high, the PG bit is cleared and the Power Good Warning is removed. The Power Good pin can also be pulled low by an external circuit to initiate the Power Good Warning.

**Note:** To retrieve status information, Status Monitoring in the DPM Configure Devices window should be enabled (refer to Digital Power Manager Data Sheet). The DPM will retrieve

the status information from each POL on a continuous basis.

### 8.3.2 Faults

This group includes overcurrent, overtemperature, undervoltage, and tracking protections. Triggering any protection in this group will turn off the POL.

#### 8.3.2.1 Overcurrent Protection

Overcurrent protection is active whenever the output voltage of the POL exceeds the pre-bias voltage (if any). When the output current reaches the OC threshold, the output voltage will start decreasing. As soon as the output voltage decreases below the undervoltage protection threshold, the OC fault signal is generated, the POL turns off and the OC bit in the register ST is changed to 0. Both high side and low side switches of the POL are turned off instantly (fast turn-off).

The temperature compensation is added to keep the OC threshold approximately constant at temperatures above room temperature. Note that the temperature compensation can be disabled in the POL Configure Output window or directly via the I<sup>2</sup>C by writing into the CLS register. However, it is recommended to keep the temperature compensation enabled.

#### 8.3.2.2 Undervoltage Protection

The undervoltage protection is only active during steady state operation of the POL to prevent nuisance tripping. If the output voltage decreases below the UV threshold and there is no OC fault, the UV fault signal is generated, the POL turns off, and the UV bit in the register ST is changed to 0. The output voltage is ramped down according to sequencing and tracking settings (regular turn-off).

#### 8.3.2.3 Overtemperature Protection

Overtemperature protection is active whenever the POL is powered up. If temperature of the controller exceeds 130°C, the OT fault is generated, POL turns off, and the OT bit in the register ST is changed to 0. The output voltage is ramped down according to sequencing and tracking settings (regular turn-off).

If non-latching OTP is programmed, the POL will restart as soon as the temperature of the controller decreases below the Overtemperature Warning threshold of 120°C.





### 8.3.2.4 Tracking Protection

Tracking protection is active only when the output voltage is ramping up. The purpose of the protection is to ensure that the voltage differential between multiple rails being tracked does not exceed 250mV. This protection eliminates the need for external clamping diodes between different voltage rails which are frequently recommended by ASIC manufacturers.

When the tracking protection is enabled, the POL continuously compares actual value of the output voltage to its programmed value as defined by the output voltage and its rising slew rate. If absolute

value of the difference exceeds 250mV, the tracking fault signal is generated, the POL turns off, and the TR bit in the register ST is changed to 0. Both high side and low side switches of the POL are turned off instantly (fast turn-off).

The tracking protection can be disabled, if it contradicts requirements of a particular system (for example turning into high capacitive load where rising slew rate is not important). It can be disabled in the DPM Configure Faults window or directly via the I<sup>2</sup>C bus by writing into the PC1 register.

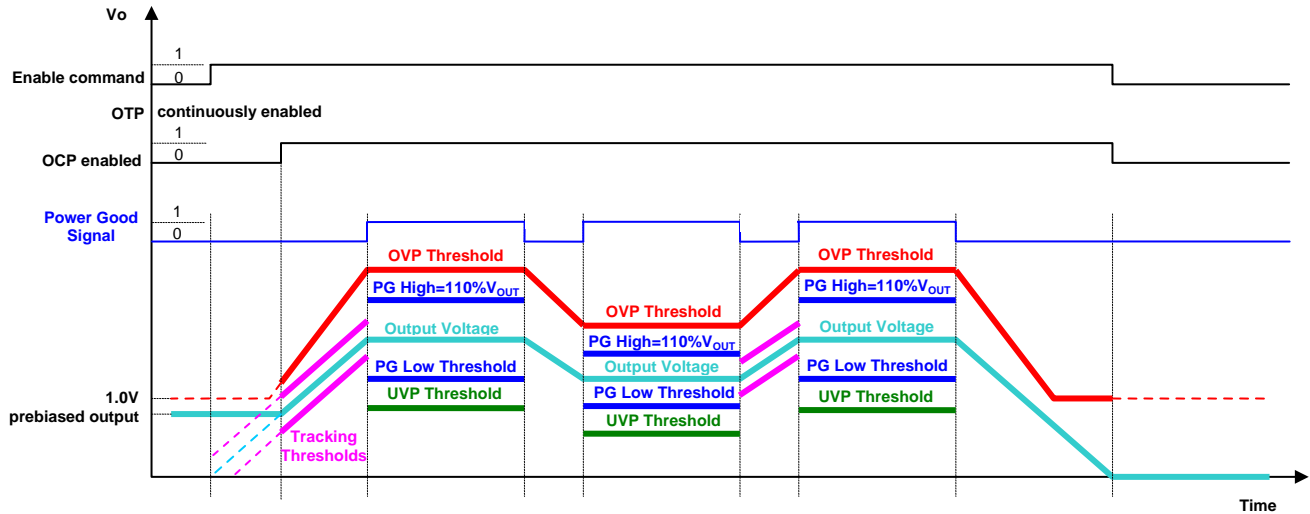


Figure 43. Protections Enable Conditions

### 8.3.3 Errors

The group includes overvoltage protection and the phase voltage error. The phase voltage error is not available in ZY7115.

#### 8.3.3.1 Overvoltage Protection

The overvoltage protection is active whenever the output voltage of the POL exceeds the pre-bias voltage (if any). If the output voltage exceeds the overvoltage protection threshold, the overvoltage error signal is generated, the POL turns off, and the OV bit in the register ST is changed to 0. The high side switch is turned off instantly, and simultaneously the low side switch is turned on to ensure reliable protection of sensitive loads. The low side switch provides low impedance path to quickly dissipate energy stored in the output filter and achieve effective voltage limitation.

The OV threshold can be programmed from 110% to 130% of the output voltage setpoint, but not lower than 1.0V.

### 8.3.4 Faults and Errors Propagation

The feature adds flexibility to the fault management scheme by giving users control over propagation of fault signals within and outside of the system. The propagation means that a fault in one POL can be programmed to turn off other POLs and devices in the system, even if they are not directly affected by the fault.

#### 8.3.4.1 Grouping of POLs

ZY-Series POLs can be arranged in several groups to simplify fault management. A group of POLs is defined as a number of POLs with interconnected OK pins. A group can include from 1 to 32 POLs. If





fault propagation within a group is desired, the propagation bit needs to be checked in the DPM Configure Faults Window. The parameters can also be programmed directly via the I<sup>2</sup>C bus by writing into the PC3 register shown in Figure 44.

When propagation is enabled, the faulty POL pulls its OK pin low. A low OK line initiates turn-off of other POLs in the group.

| R/W-0   | R/W-0 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 | R/W-1 |
|---|-------|-------|-------|-------|-------|-------|-------|
| PTM   | PGM   | TRP   | OTP   | OCF   | UVP   | OVP   | PVP   |
| Bit 7   |       |       |       | Bit 0 |       |       |       |
| Bit 7 <b>PTM</b> : Temperature warning Message<br>1 = enabled<br>0 = disabled<br><br>Bit 6 <b>PGM</b> : Power good message<br>1 = enabled<br>0 = disabled<br><br>Bit 5 <b>TRP</b> : Tracking fault propagation<br>1 = enabled<br>0 = disabled<br><br>Bit 4 <b>OTP</b> : Overtemperature fault propagation<br>1 = enabled<br>0 = disabled<br><br>Bit 3 <b>OCF</b> : Overcurrent fault propagation<br>1 = enabled<br>0 = disabled<br><br>Bit 2 <b>UVP</b> : Undervoltage fault propagation<br>1 = enabled<br>0 = disabled<br><br>Bit 1 <b>OVP</b> : Overvoltage error propagation<br>1 = enabled<br>0 = disabled<br><br>Bit 0 <b>PVP</b> : Phase voltage error propagation<br>1 = enabled<br>0 = disabled |       |       |       |       |       |       |       |
| R = Readable bit<br>W = Writable bit<br>U = Unimplemented bit, read as '0'<br>- n = Value at POR reset  |       |       |       |       |       |       |       |

Figure 44. Protection Configuration Register PC3

In addition, the OK lines can be connected to the DPM to facilitate propagation of faults and errors between groups. One DPM can control up to 4 independent groups. To enable fault propagation between groups, the respective bit needs to be checked in the DPM Configure Faults window, Group Fault Propagation sub window shown in Figure 45.

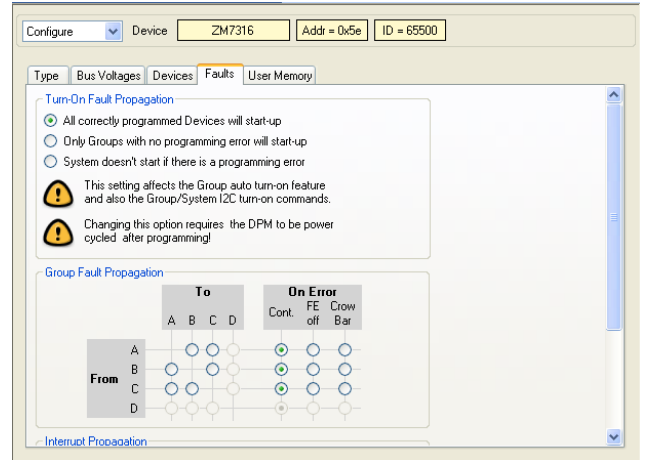


Figure 45. DPM Configure Faults Window

In this case low OK line will signal DPM to pull other OK lines low to initiate shutdown of other POLs as programmed in the DPM Configure Faults window. If an error is propagated, the DPM can also generate commands to turn off a front end (a DC-DC converter generating the intermediate bus voltage) and trigger an optional crowbar protection to accelerate removal of the IBV voltage.

### 8.3.4.2 Propagation Process

Propagation of a fault (OCF, UVP, OTP, and TRP) initiates regular turn-off of other POLs. The faulty POL in this case performs either the regular or the fast turn-off depending on a specific fault as described in section 8.3.2.

Propagation of an error initiates fast turn-off of other POLs. The faulty POL performs the fast turn-off and turns on its low side switch.

Example of the fault propagation is shown in Figure 46 - Figure 47. In this three-output system (refer to the block diagram in Figure 26), the POL powering the output V3 (Ch 1 in the picture) encounters the undervoltage fault after the turn-on. When the fault propagation is not enabled, the POL turns off and generates the UV fault signal. Because the UV fault triggers the regular turn off, the POL meets its turn-off delay and falling slew rate settings during the turn-off process as shown in Figure 46. Since the UV fault is programmed to be non-latching, the POL will attempt to restart every 130ms, repeating the process described above until the condition causing the undervoltage is removed.





If the fault propagation between groups is enabled, the POL powering the output V3 pulls its OK line low and the DPM propagates the signal to the POL powering the output V1 that belongs to other group. The POL powering the output V1 (Ch3 in the picture) executes the regular turn-off. Since both V1 and V3 have the same delay and slew rate settings they will continue to turn off and on synchronously every 130ms as shown in Figure 47 until the condition causing the undervoltage is removed. The POL powering the output V2 continues to ramp up until it reaches its steady state level.

130ms is the interval from the instant of time when the output voltage ramps down to zero until the output voltage starts to ramp up again. Therefore, the 130ms hiccup interval is guaranteed regardless of the turn-off delay setting.

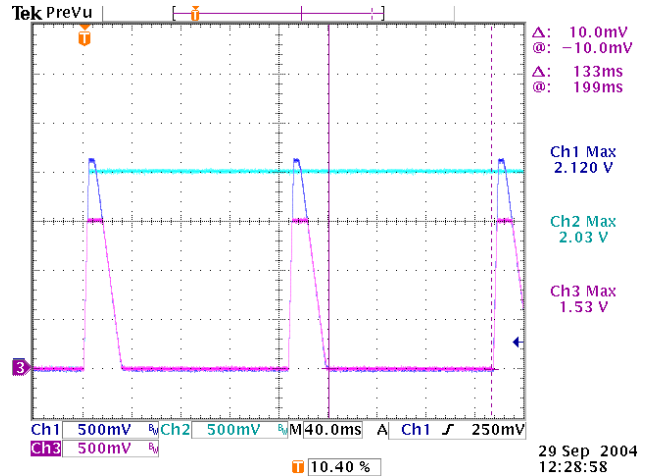


Figure 47. Turn-On into UVP on V3. The UV Fault Is Programmed To Be Non-Latching and Propagate From Group C to Group A. Ch1 – V3 (Group C), Ch2 – V2, Ch3 – V1 (Group A)

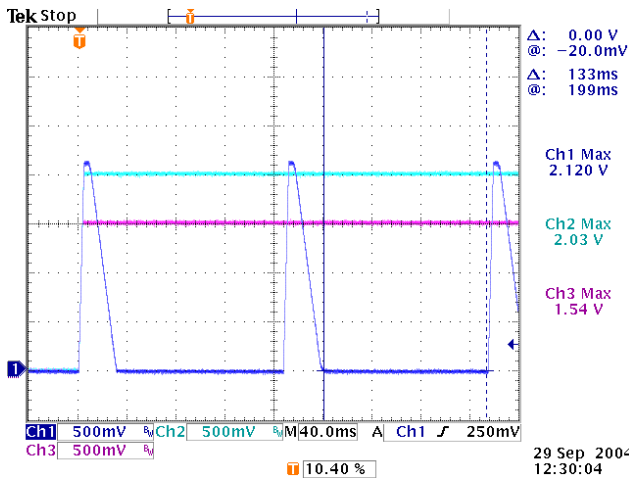


Figure 46. Turn-On into UVP on V3. The UV Fault Is Programmed To Be Non-Latching. Ch1 – V3 (Group C), Ch2 – V2, Ch3 – V1 (Group A)

Summary of protections, their parameters and features are shown in Table 3

Table 3. Summary of Protections Parameters and Features

| Code | Name                | Type    | When Active                    | Turn Off | Low Side Switch | Propagation      | Disable |
|------|---------------------|---------|--------------------------------|----------|-----------------|------------------|---------|
| PT   | Temperature Warning | Warning | Whenever $V_{IN}$ is applied   | No       | N/A             | Readable by DPM  | No      |
| PG   | Power Good          | Warning | During steady state            | No       | N/A             | Readable by DPM  | No      |
| TR   | Tracking            | Fault   | During ramp up                 | Fast     | Off             | Regular turn off | Yes     |
| OT   | Overtemperature     | Fault   | Whenever $V_{IN}$ is applied   | Regular  | Off             | Regular turn off | No      |
| OC   | Overcurrent         | Fault   | When $V_{OUT}$ exceeds prebias | Fast     | Off             | Regular turn off | No      |
| UV   | Undervoltage        | Fault   | During steady state            | Regular  | Off             | Regular turn off | No      |
| OV   | Overvoltage         | Error   | When $V_{OUT}$ exceeds prebias | Fast     | On              | Fast turn off    | No      |





### 8.4 PWM Parameters

Z-Series POLs utilize the digital PWM controller. The controller enables users to program most of the PWM performance parameters, such as switching frequency, interleave, duty cycle, and feedback loop compensation.

#### 8.4.1 Switching Frequency

The switching frequency can be programmed in the POL Controller Compensation window shown in Figure 48 or directly via the I<sup>2</sup>C bus by writing into the INT register shown in Figure 49. Note that the content of the register can be changed only when the POL is turned off.

Switching actions of all POLs connected to the SD line are synchronized to the master clock generated by the DPM. Each POL is equipped with a PLL and a frequency divider so they can operate at multiples (including fractional) of the master clock frequency as programmed by a user. The POL converters can operate at 500 kHz, 750 kHz, and 1 MHz. Although synchronized, switching frequencies of different POLs are independent of each other. It is permissible to mix POLs operating at different frequencies in one system. It allows optimizing efficiency and transient response of each POL in the system individually.

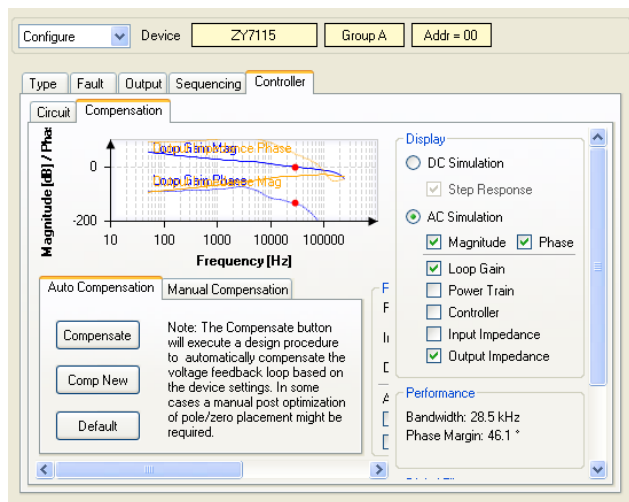


Figure 48. POL Configure Controller Compensation Window

| R/W-0   | R/W-0 | R/W-0 | R/W-0 <sup>1)</sup> | R/W-0 <sup>1)</sup> | R/W-0 <sup>1)</sup> | R/W-0 <sup>1)</sup> | R/W-0 <sup>1)</sup> |
|---|-------|-------|---------------------|---------------------|---------------------|---------------------|---------------------|
| FRQ2  | FRQ1  | FRQ0  | INT4                | INT3                | INT2                | INT1                | INT0                |
| Bit 7   |       |       |                     |                     |                     |                     | Bit 0               |
| Bit 7:5 <b>FRQ[2:0]</b> : PWM Frequency Selection<br>000: 500kHz<br>001: 750kHz<br>010: 1000Hz<br>011: 1250kHz<br>100: 1250kHz<br>101: 1500kHz<br>110: 1750kHz<br>111: 2000kHz  |       |       |                     |                     |                     |                     |                     |
| Bit 4:0 <b>INT[4:0]</b> : Interleave position<br>00h: Ton starts with 0.0° Phase lag to SD Line<br>01h: Ton starts with 11.25° Phase lag to SD Line<br>02h: Ton starts with 22.50° Phase lag to SD Line<br>...<br>1Fh: Ton starts with 348.75° Phase lag to SD Line |       |       |                     |                     |                     |                     |                     |
| <sup>1)</sup> Initial value depends on the state of the Interleave Mode ( <b>IM</b> ) Input:<br>IM=Open: At POR reset the 5 corresponding ADDRESS bits are loaded<br>IM=Low: At POR reset a 0 is loaded   |       |       |                     |                     |                     |                     |                     |

Figure 49. Interleave Configuration Register INT

#### 8.4.2 Interleave

Interleave is defined as a phase delay between the synchronizing slope of the master clock on the SD pin and PWM signal of a POL. The interleave can be programmed in the POL Configure Controller Compensation window or directly via the I<sup>2</sup>C bus by writing into the INT register.

Every POL generates switching noise. If no interleave is programmed, all POLs in the system switch simultaneously and noise reflected to the input source from all POLs is added together as shown in Figure 50.

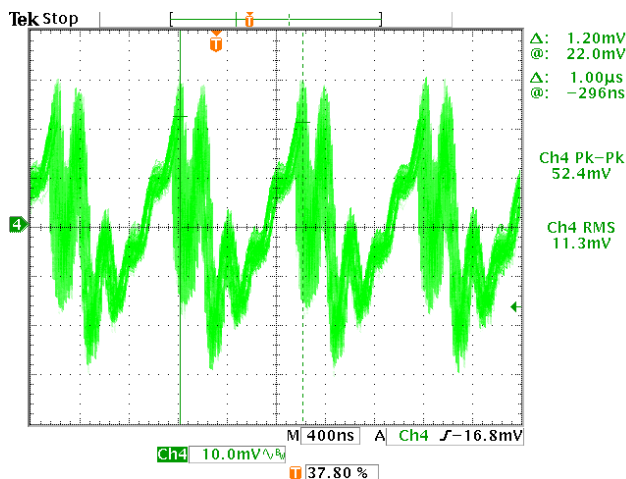


Figure 50. Input Voltage Noise, No Interleave





Figure 51 shows the input voltage noise of the three-output system with programmed interleave. Instead of all three POLs switching at the same time as in the previous example, the POLs V1, V2, and V3 switch at 67.5°, 180°, and 303.75°, respectively. Noise is spread evenly across the switching cycle resulting in more than 1.5 times reduction. To achieve similar noise reduction without the interleave will require the addition of an external LC filter.

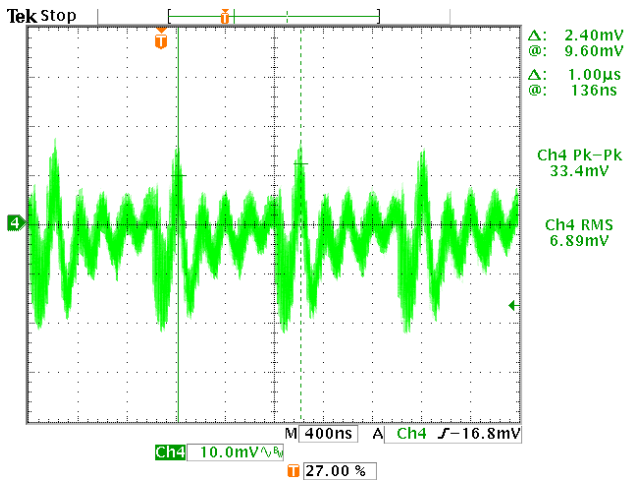


Figure 51. Input Voltage Noise with Interleave

Similar noise reduction can be achieved on the output of POLs connected in parallel. Figure 52 and Figure 53 show the output noise of two ZY7115s connected in parallel without and with 180° interleave, respectively. Resulting noise reduction is more than 2 times and is equivalent to doubling switching frequency or adding extra capacitance on the output of the POLs.

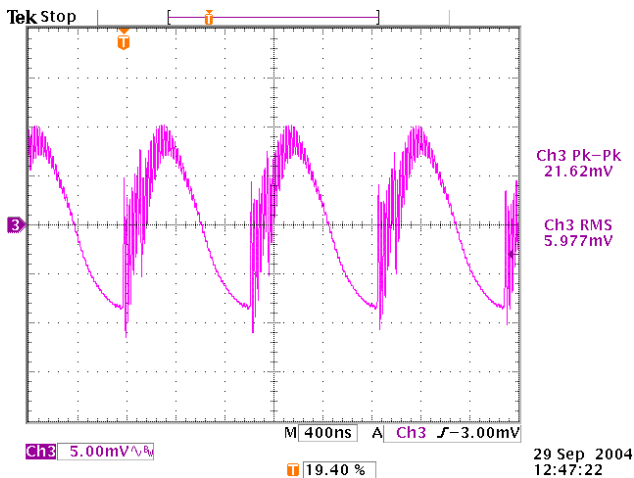


Figure 52. Output Voltage Noise, Full Load, No Interleave

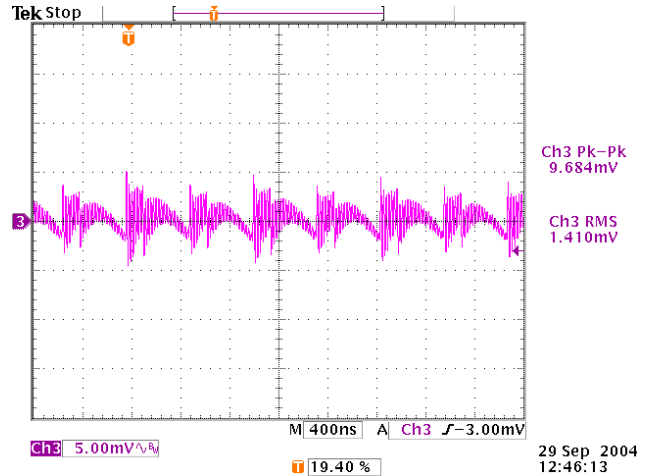


Figure 53. Output Voltage Noise, Full Load, 180° Interleave

The ZY7115 interleave feature is similar to that of multiphase converters, however, unlike in the case of multiphase converters, interleave does not have to be equal to 360/N, where N is the number of POLs in a system. ZY7115 interleave is independent of the number of POLs in a system and is fully programmable in 11.25° steps. It allows maximum output noise reduction by intelligently spreading switching energy.

**Note:** Due to noise sensitivity issues that may occur in limited cases, it is recommended to avoid phase lag settings of 112.5 and 123.75 degrees, otherwise false PG and/or OV indications may occur.

### 8.4.3 Duty Cycle Limit

The ZY7115 is a step-down converter therefore  $V_{OUT}$  is always less than  $V_{IN}$ . The relationship between the two parameters is characterized by the duty cycle and can be estimated from the following equation:

$$DC = \frac{V_{OUT}}{V_{IN,MIN}}$$

Where, DC is the duty cycle,  $V_{OUT}$  is the required maximum output voltage (including margining),  $V_{IN,MIN}$  is the minimum input voltage.

It is good practice to limit the maximum duty cycle of the controller's PWM to a somewhat higher value compared to the steady-state duty cycle as expressed by the above equation. This will further protect the output from excessive voltages. The duty cycle limit can be programmed in the POL Configure Controller Compensation window or directly via the





I<sup>2</sup>C bus by writing into the DCL register shown in Figure 54.

| R/W-1   | R/W-1 | R/W-1 | R/W-0 | R/W-1 | R/W-0 | R/W-0 | R/W-0 |
|---|-------|-------|-------|-------|-------|-------|-------|
| DCL5  | DCL4  | DCL3  | DCL2  | DCL1  | DCL0  | HI    | LO    |
| Bit 7   |       |       |       |       |       | Bit 0 |       |
| Bit 7:2 <b>DCL[5:0]</b> , Duty Cycle Limitation<br>00h: 0<br>01h: 1/64<br>...<br>3Fh: 63/64 |       |       |       |       |       |       |       |
| Bit 1: <b>HI</b> , ADC high saturation feed-forward<br>0: disabled<br>1: enabled            |       |       |       |       |       |       |       |
| Bit 0: <b>LO</b> , ADC low saturation feed-forward<br>0: disabled<br>1: enabled             |       |       |       |       |       |       |       |

R = Readable bit  
 W = Writable bit  
 U = Unimplemented bit, read as '0'  
 - n = Value at POR reset

Figure 54. Duty Cycle Limit Register

### 8.4.4 ADC Saturation Feedforward

To speed up the PWM response in case of heavy dynamic loads, the duty cycle can be forced either to 0 or the duty cycle limit depending on the polarity of the transient. This function is equivalent to having two comparators defining a window around the output voltage setpoint. When an error signal is inside the window, it will produce gradual duty cycle change proportional to the error signal. If the error signal goes outside the window (usually due to large output current steps), the duty cycle will change to its limit in one switching cycle. In most cases this will significantly improve transient response of the controller, reducing amount of required external capacitance.

Under certain circumstances, usually when the maximum duty cycle limit significantly exceeds its nominal value, the ADC saturation can lead to the overcompensation of the output error. The phenomenon manifests itself as low frequency oscillations on the output of the POL. It can usually be reduced or eliminated by disabling the ADC saturation or limiting the maximum duty cycle to 120-140% of the calculated value. It is not recommended to use ADC saturation for output voltages higher than 2.0V.

The ADC saturation feedforward can be programmed in the POL Configure Controller Compensation window or directly via the I<sup>2</sup>C bus by writing into the DCL register.

### 8.4.5 Feedback Loop Compensation

Feedback loop compensation can be programmed in the GUI POL Configure Controller Compensation window by setting frequency of poles and zeros of the transfer function.

The transfer function of the POL converter is shown in Figure 55. It is a third order function with two zeros and three poles. Pole 1 is the integrator pole, Pole 2 is used in conjunction with Zero 1 and Zero 2 to adjust the phase lead and limit the gain increase in mid band. Pole 3 is used as a high frequency low-pass filter to limit PWM noise.

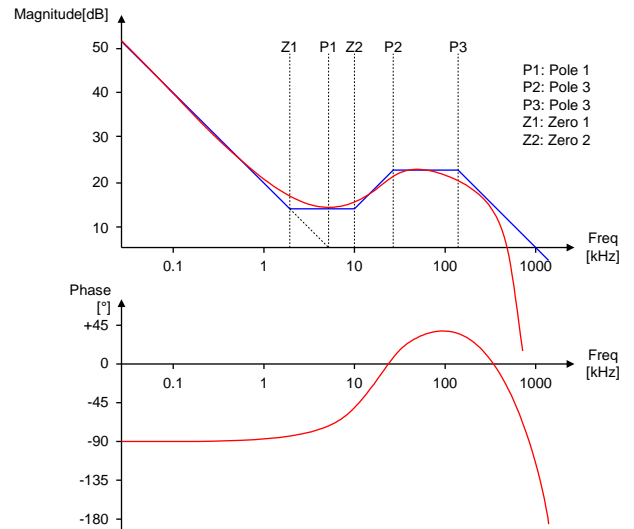


Figure 55. Transfer Function of PWM

Positions of poles and zeroes are determined by coefficients of the digital filter. The filter is characterized by four numerator coefficients ( $C_0, C_1, C_2, C_3$ ) and three denominator coefficients ( $B_1, B_2, B_3$ ). The coefficients are automatically calculated when desired frequency of poles and zeros is entered in the GUI POL Configure Controller Compensation window. The coefficients are stored in the C0H, C0L, C1H, C1L, C2H, C2L, C3H, C3L, B1, B2, and B3 registers.

**Note:** The GUI automatically transforms zero and pole frequencies into the digital filter coefficients. It is strongly recommended to use the GUI to determine the filter coefficients.

Programming feedback loop compensation allows optimizing POL performance for various application





conditions. For example, increase in bandwidth can significantly improve dynamic response.

### 8.5 Current Share

The POL converters are equipped with the digital current share function. To activate the current share, interconnect the CS pins of the POLs connected in parallel. The digital signal transmitted over the CS line sets output currents of all POLs to the same level.

When POLs are connected in parallel, they must be included in the same parallel bus in the DPM Configure Devices window shown in Figure 56. In this case, the GUI automatically copies critical parameters of one POL onto all POLs connected to the parallel bus. It makes it impossible to configure different performance parameters for POLs connected in parallel except for interleave and load regulation settings that are independent. The interleave allows to reduce and move the output noise of the converters connected in parallel to higher frequencies as shown in Figure 52 and Figure 53. The load regulation allows controlling the current share loop gain in case of small signal oscillations. It is recommended to always add a small amount of load regulation to one of the converters connected in parallel to reduce loop gain and therefore improve stability.

### 8.6 Performance Parameters Monitoring

The POL converters can monitor their own performance parameters such as output voltage, output current, and temperature.

The output voltage is measured at the output sense pins, output current is measured using the ESR of the output inductor and temperature is measured by the thermal sensor built into the controller IC. Output current readings are adjusted based on temperature readings to compensate for the change of ESR of the inductor with temperature.

An 8-Bit Analog to Digital Converter (ADC) converts the output voltage, output current, and temperature into a digital signal to be transmitted via the serial interface. The ADC allows a minimum sampling frequency of 1 kHz for all three values.

Monitored parameters are stored in registers (VOM, IOM, and TMON) that are continuously updated. If the Retrieve Monitoring bits in the DPM Configure Devices window shown in Figure 56 are checked, those registers are being copied into the ring buffer located in the DPM. Contents of the ring buffer can be displayed in the DPM Monitor Window shown in Figure 57 or it can be read directly via the I<sup>2</sup>C bus using high and low level commands as described in the "ZM7300 Digital Power Manager Programming Manual".



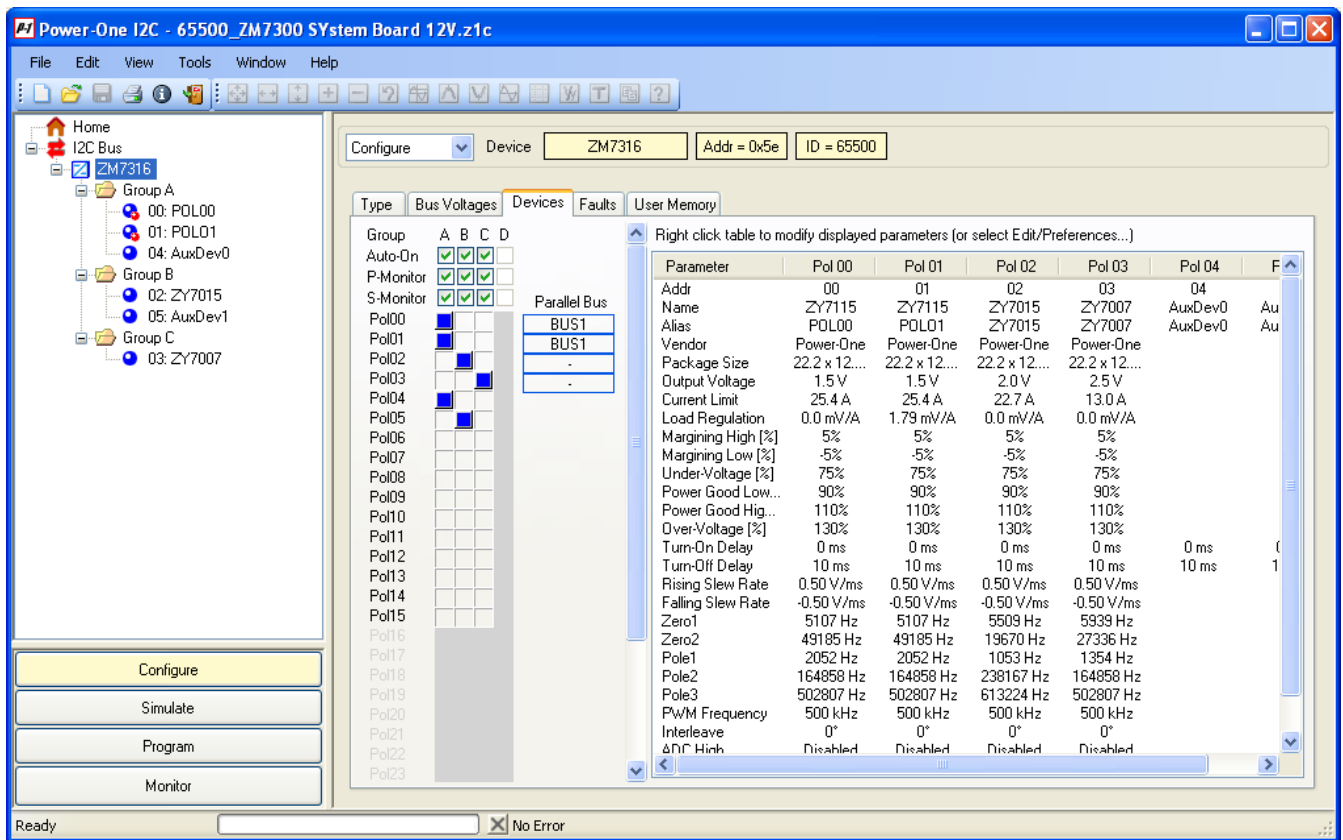


Figure 56. DPM Configure Devices Window

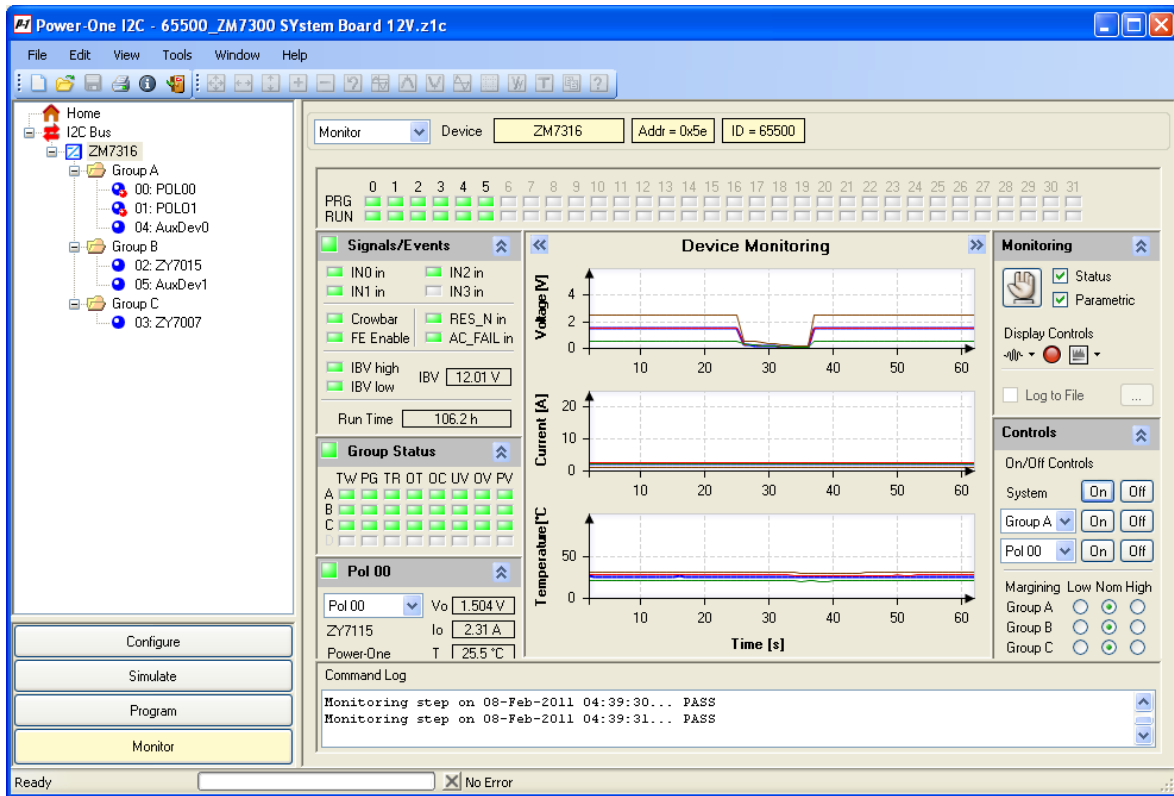


Figure 57. DPM Monitor Window

## 9. Safety

The ZY7115 POL converters **do not provide isolation** from input to output. The input devices powering ZY7115 must provide relevant isolation requirements according to all IEC60950 based standards. Nevertheless, if the system using the converter needs to receive safety agency approval, certain rules must be followed in the design of the system. In particular, all of the creepage and clearance requirements of the end-use safety requirements must be observed. These requirements are included in UL60950 - CSA60950-00 and EN60950, although specific applications may have other or additional requirements.

The ZY7115 POL converters have no internal fuse. If required, the external fuse needs to be provided to protect the converter from catastrophic failure. Refer to the "Input Fuse Selection for DC/DC converters" application note on [www.power-one.com](http://www.power-one.com) for proper selection of the input fuse. Both input traces and the

chassis ground trace (if applicable) must be capable of conducting a current of 1.5 times the value of the fuse without opening. The fuse must not be placed in the grounded input line.

Abnormal and component failure tests were conducted with the POL input protected by a fast-acting 65 V, 15 A, fuse. If a fuse rated greater than 15 A is used, additional testing may be required.

In order for the output of the ZY7115 POL converter to be considered as SELV (Safety Extra Low Voltage), according to all IEC60950 based standards, the input to the POL needs to be supplied by an isolated secondary source providing a SELV also.



10. Mechanical Drawings

All Dimensions are in mm  
 Tolerances:  
 0.5-10 ±0.1  
 10-100 ±0.2  
 Pin Coplanarity: 0.1 max

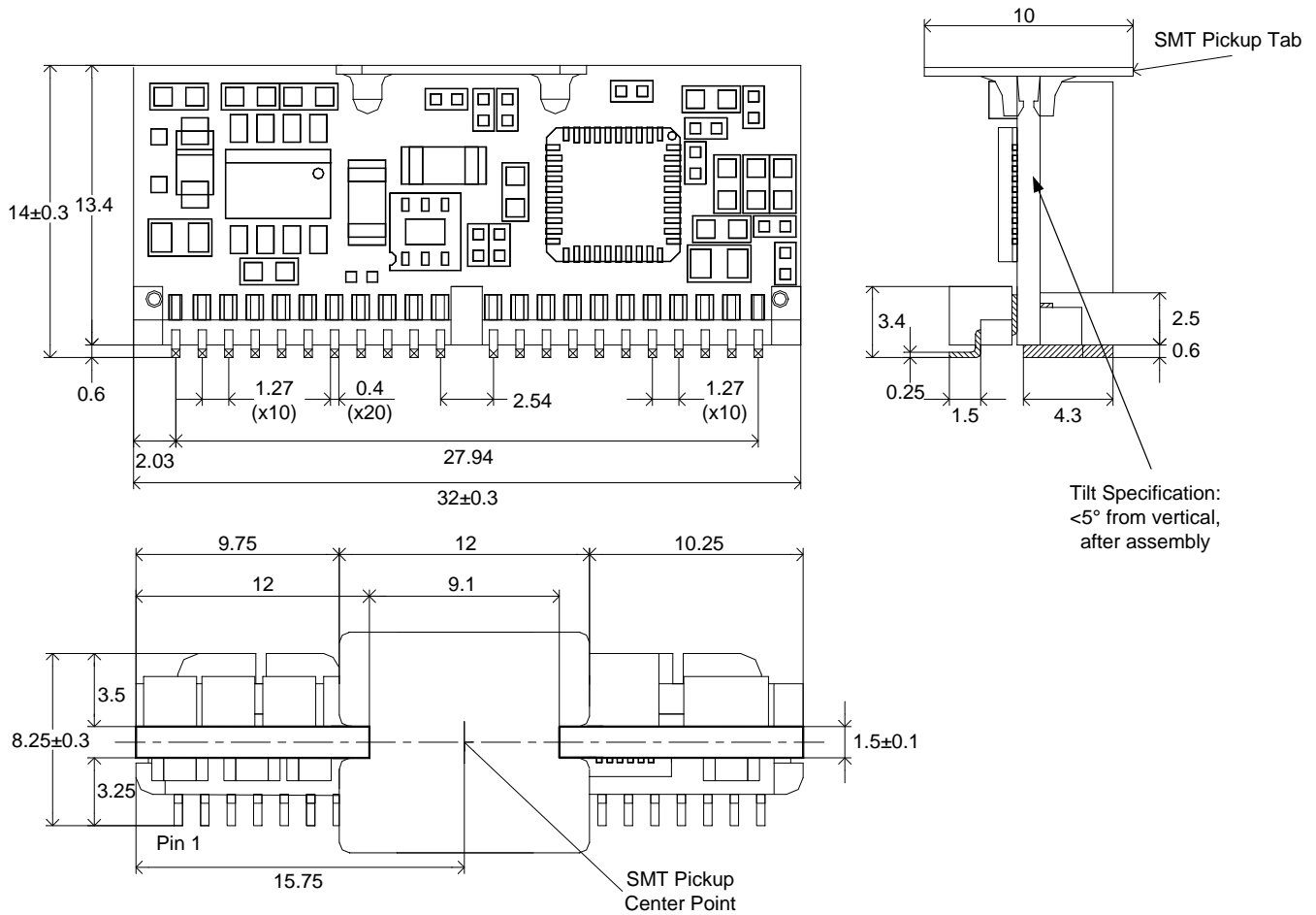


Figure 58. Mechanical Drawing

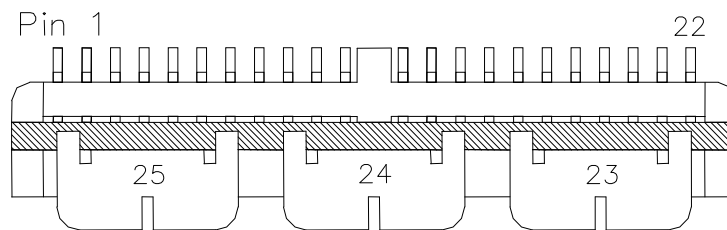


Figure 59. Pinout Diagram (Bottom View)



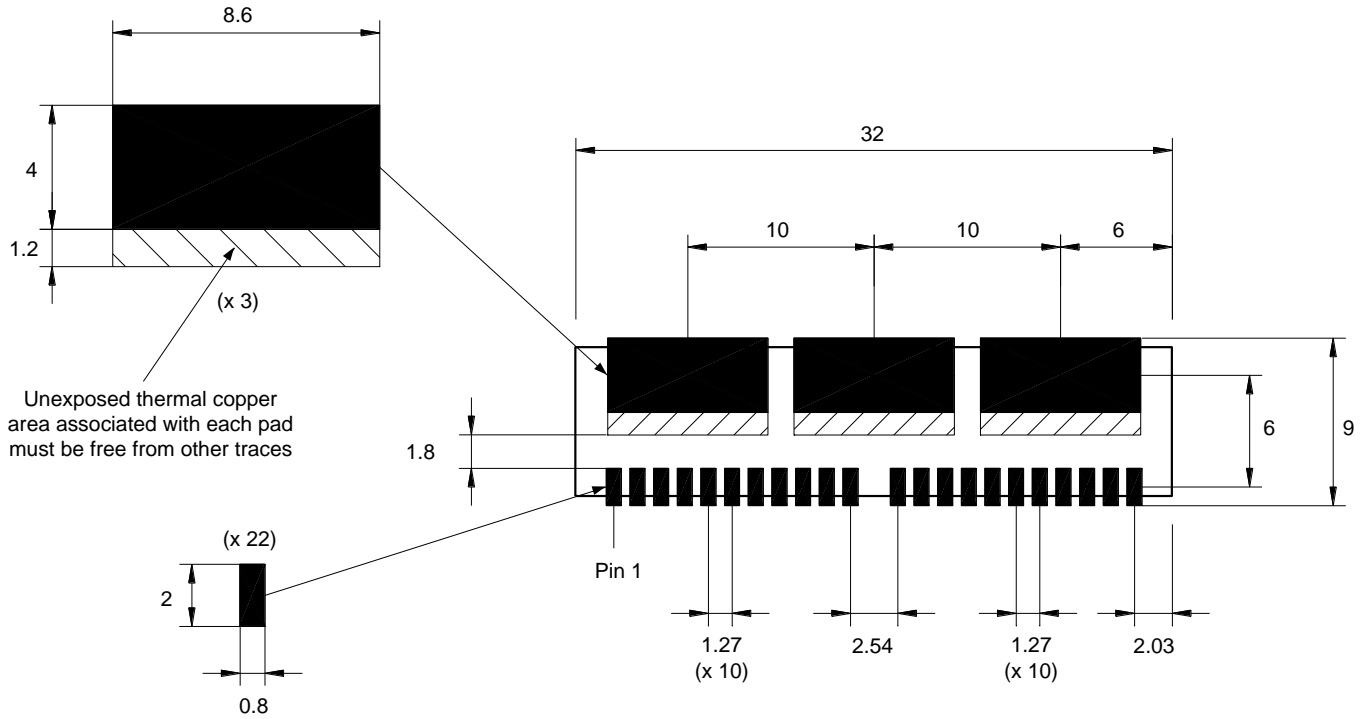


Figure 60. Recommended Pad Sizes

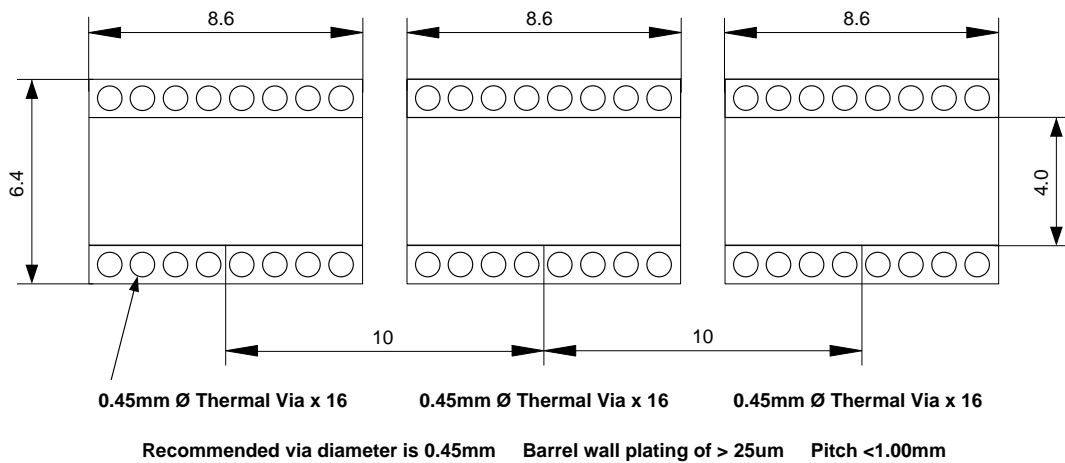


Figure 61. Recommended PCB Layout for Multilayer PCBs

**Notes:**

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