



THE DATASHEET OF AO4441



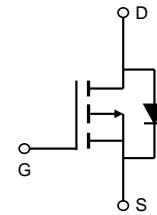
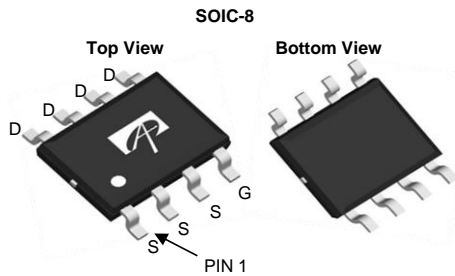


General Description

The AO4441 uses advanced trench technology to provide excellent $R_{DS(ON)}$, and ultra-low low gate charge. This device is suitable for use as a load switch or in PWM applications.

Product Summary

V_{DS}	-60V
I_D (at $V_{GS}=-10V$)	-4A
$R_{DS(ON)}$ (at $V_{GS}=-10V$)	< 100m Ω
$R_{DS(ON)}$ (at $V_{GS} = -4.5V$)	< 130m Ω



Absolute Maximum Ratings $T_A=25^\circ\text{C}$ unless otherwise noted

Parameter	Symbol	Maximum	Units
Drain-Source Voltage	V_{DS}	-60	V
Gate-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current ^A	I_D	$T_A=25^\circ\text{C}$	-4
		$T_A=70^\circ\text{C}$	-3.1
Pulsed Drain Current ^B	I_{DM}	-20	A
Power Dissipation ^A	P_D	$T_A=25^\circ\text{C}$	3.1
		$T_A=70^\circ\text{C}$	2
Junction and Storage Temperature Range	T_J, T_{STG}	-55 to 150	$^\circ\text{C}$

Thermal Characteristics

Parameter	Symbol	Typ	Max	Units
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	24	40	$^\circ\text{C/W}$
$t \leq 10\text{s}$				
Maximum Junction-to-Ambient ^A	$R_{\theta JA}$	54	75	$^\circ\text{C/W}$
Steady-State				
Maximum Junction-to-Lead ^C	$R_{\theta JL}$	21	30	$^\circ\text{C/W}$
Steady-State				

Electrical Characteristics (T_J=25°C unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Units
STATIC PARAMETERS						
BV _{DSS}	Drain-Source Breakdown Voltage	I _D =-250μA, V _{GS} =0V	-60			V
I _{DSS}	Zero Gate Voltage Drain Current	V _{DS} =-48V, V _{GS} =0V T _J =55°C			-1 -5	μA
I _{GSS}	Gate-Body leakage current	V _{DS} =0V, V _{GS} = ±20V			±100	nA
V _{GS(th)}	Gate Threshold Voltage	V _{DS} =V _{GS} , I _D =-250μA	-1	-2.1	-3	V
R _{DS(ON)}	Static Drain-Source On-Resistance	V _{GS} =-10V, I _D =-4A T _J =125°C		80 130	100	mΩ
		V _{GS} =-4.5V, I _D =-3A		102	130	mΩ
g _{FS}	Forward Transconductance	V _{DS} =-5V, I _D =-4A		10		S
V _{SD}	Diode Forward Voltage	I _S =-1A, V _{GS} =0V		-0.77	-1	V
I _S	Maximum Body-Diode Continuous Current				-4	A
DYNAMIC PARAMETERS						
C _{iss}	Input Capacitance	V _{GS} =0V, V _{DS} =-30V, f=1MHz		930		pF
C _{oss}	Output Capacitance			85		pF
C _{riss}	Reverse Transfer Capacitance			35		pF
R _g	Gate resistance	f=1MHz		9.5	15	Ω
SWITCHING PARAMETERS						
Q _{g(10V)}	Total Gate Charge	V _{GS} =-10V, V _{DS} =-30V, I _D =-4A		16	22	nC
Q _{g(4.5V)}	Total Gate Charge			8	12	nC
Q _{gs}	Gate Source Charge			2.5		nC
Q _{gd}	Gate Drain Charge			3.2		nC
t _{D(on)}	Turn-On DelayTime	V _{GS} =-10V, V _{DS} =-30V, R _L =7.5Ω, R _{GEN} =3Ω		8		ns
t _r	Turn-On Rise Time			3.8		ns
t _{D(off)}	Turn-Off DelayTime			31.5		ns
t _f	Turn-Off Fall Time			7.5		ns
t _{rr}	Body Diode Reverse Recovery Time		I _F =-4A, di/dt=100A/μs		27	
Q _{rr}	Body Diode Reverse Recovery Charge	I _F =-4A, di/dt=100A/μs		32		nC

A: The value of R_{θJA} is measured with the device mounted on 1in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The value in any a given application depends on the user's specific board design. The current rating is based on the t ≤ 10s thermal resistance rating.
 B: Repetitive rating, pulse width limited by junction temperature.
 C: The R_{θJA} is the sum of the thermal impedance from junction to lead R_{θJL} and lead to ambient.
 D: The static characteristics in Figures 1 to 6,12,14 are obtained using 80 μs pulses, duty cycle 0.5% max.
 E: These tests are performed with the device mounted on 1 in² FR-4 board with 2oz. Copper, in a still air environment with T_A=25° C. The SOA curve provides a single pulse rating.

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TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

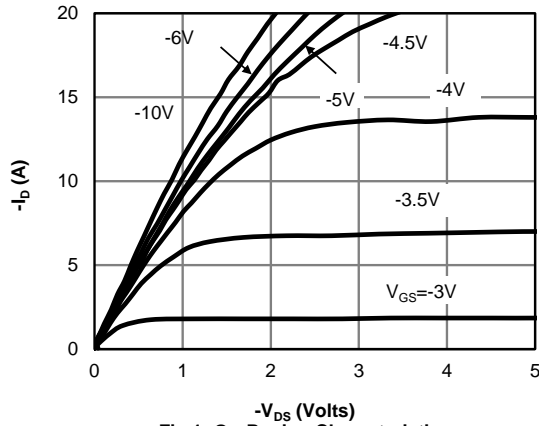


Fig 1: On-Region Characteristics

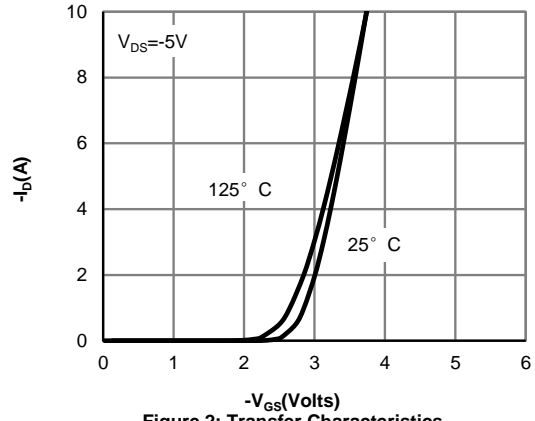


Figure 2: Transfer Characteristics

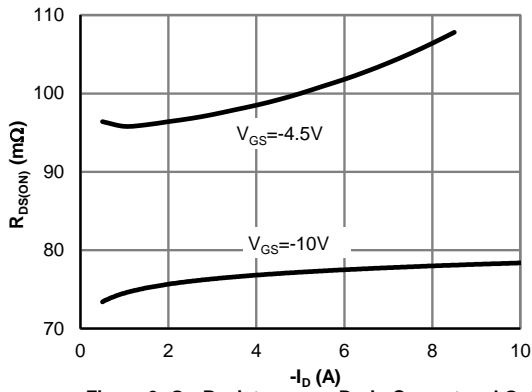


Figure 3: On-Resistance vs. Drain Current and Gate Voltage

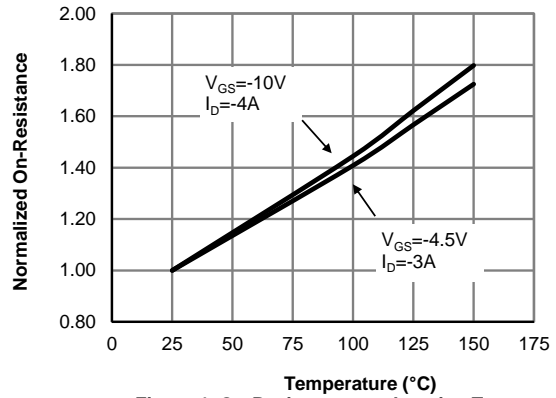


Figure 4: On-Resistance vs. Junction Temperature

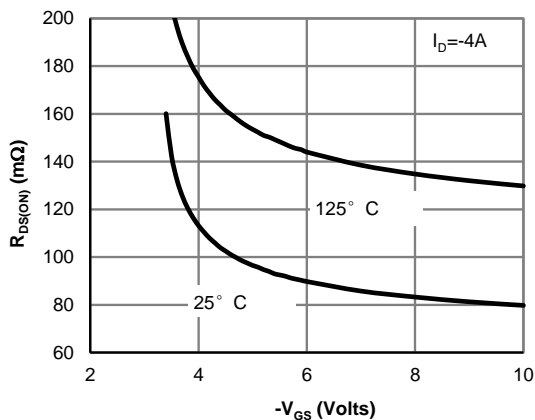


Figure 5: On-Resistance vs. Gate-Source Voltage

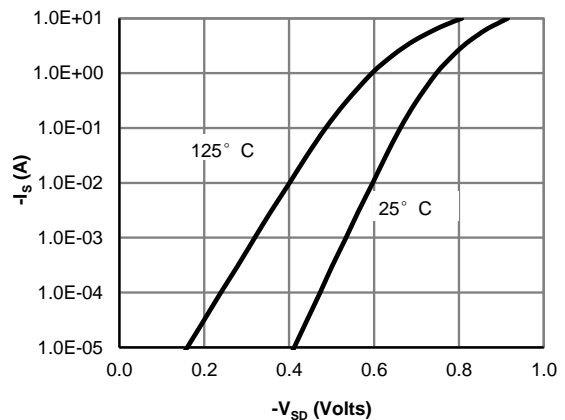


Figure 6: Body-Diode Characteristics

TYPICAL ELECTRICAL AND THERMAL CHARACTERISTICS

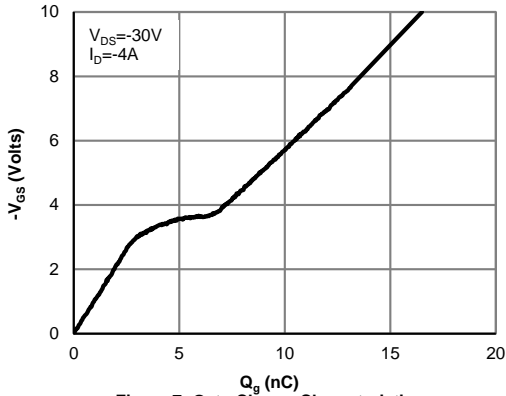


Figure 7: Gate-Charge Characteristics

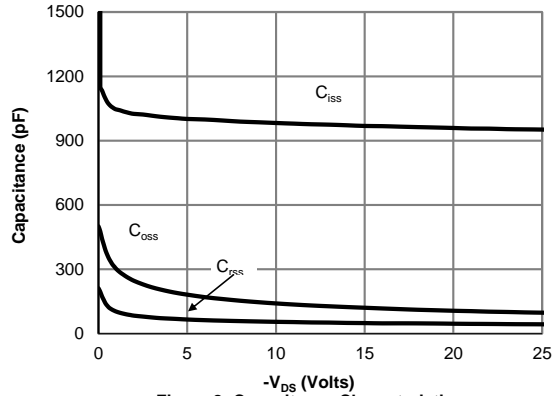


Figure 8: Capacitance Characteristics

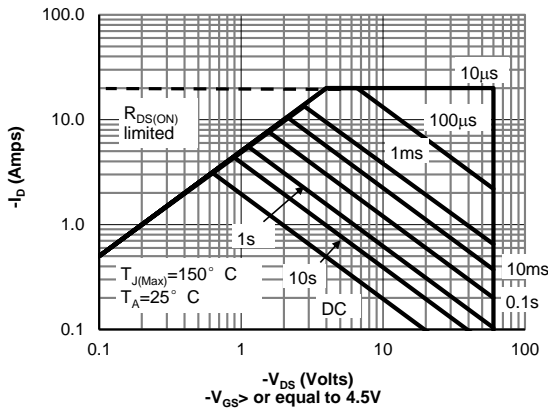


Figure 9: Maximum Forward Biased Safe Operating Area (Note E)

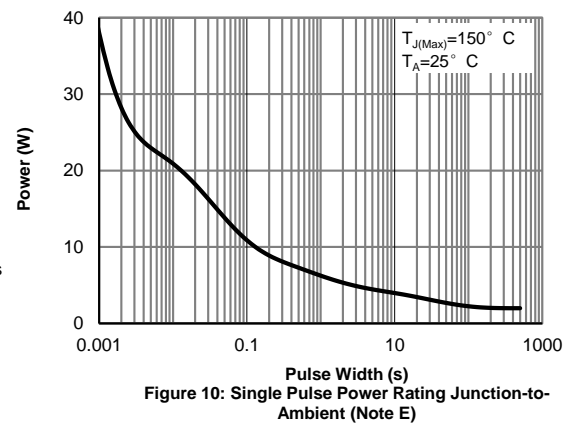


Figure 10: Single Pulse Power Rating Junction-to-Ambient (Note E)

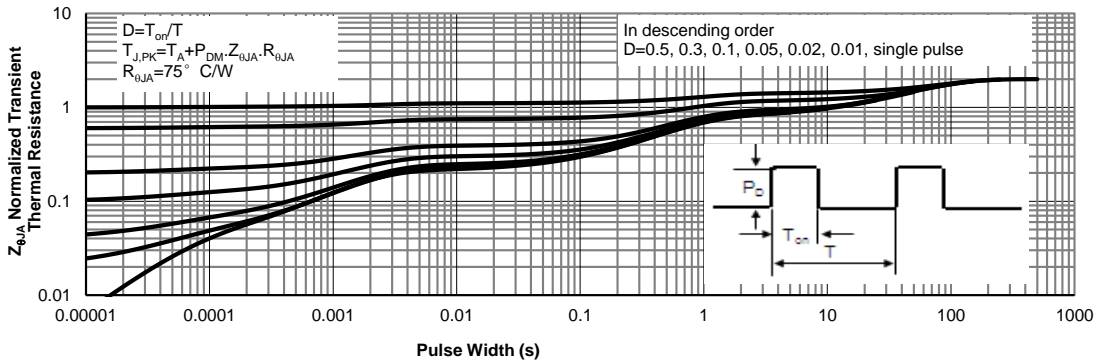
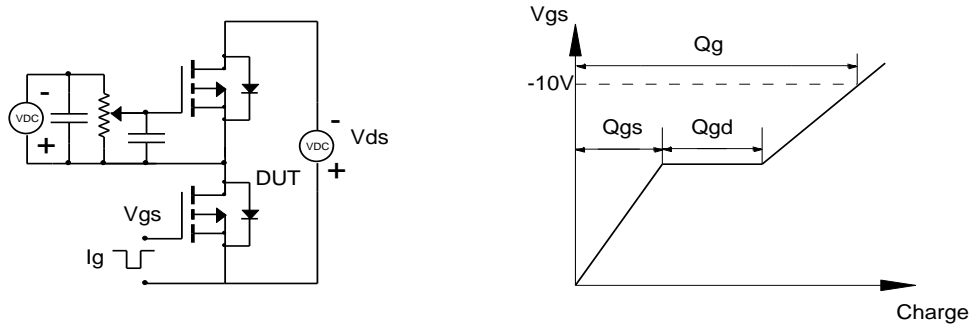
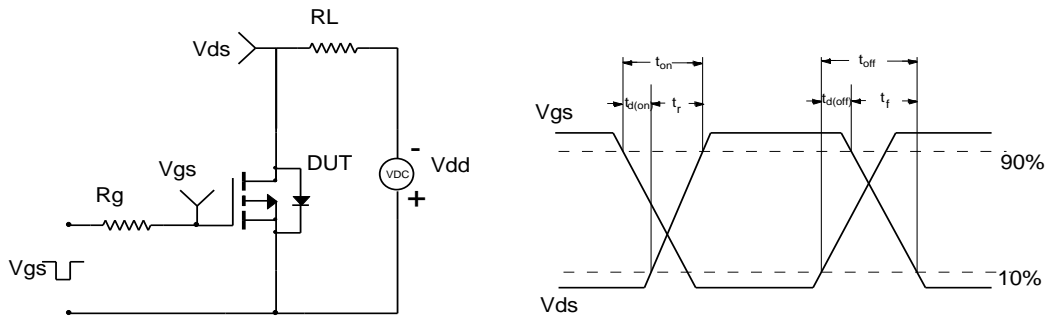


Figure 11: Normalized Maximum Transient Thermal Impedance

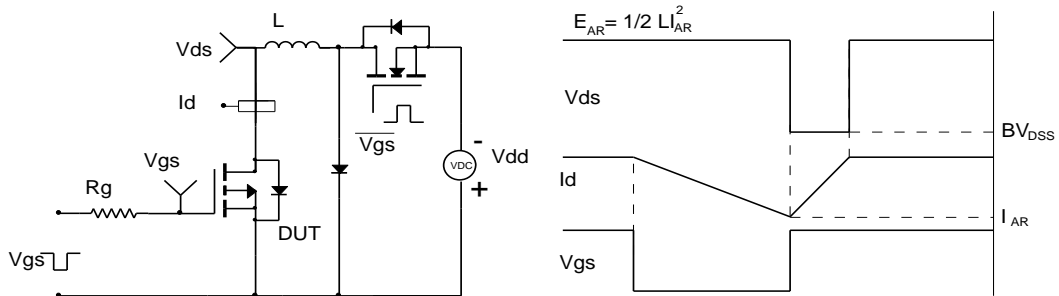
Gate Charge Test Circuit & Waveform



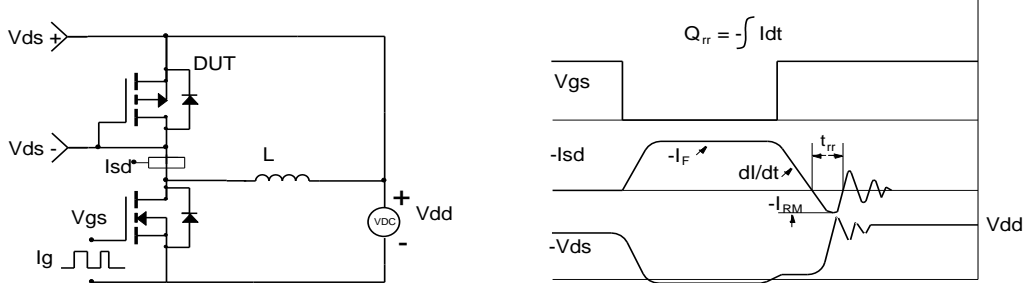
Resistive Switching Test Circuit & Waveforms



Unclamped Inductive Switching (UIS) Test Circuit & Waveforms



Diode Recovery Test Circuit & Waveforms



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