



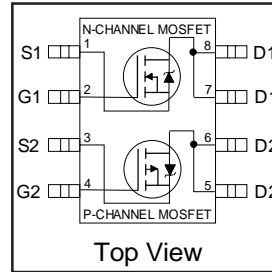
**THE DATASHEET OF
IRF7309QTRPBF**



IRF7309QPbF

HEXFET® Power MOSFET

- Advanced Process Technology
- Ultra Low On-Resistance
- Dual N and P Channel MOSFET
- Surface Mount
- Available in Tape & Reel
- 150°C Operating Temperature
- Lead-Free

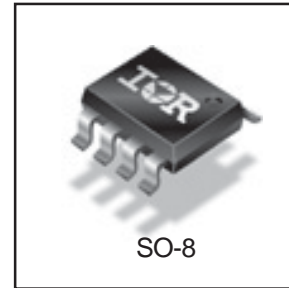


	N-Ch	P-Ch
V_{DS}	30V	-30V
$R_{DS(on)}$	0.050Ω	0.10Ω

Description

These HEXFET® Power MOSFET's in a Dual SO-8 package utilize the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of these HEXFET Power MOSFET's are a 150°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These benefits combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.

The efficient SO-8 package provides enhanced thermal characteristics and dual MOSFET die capability making it ideal in a variety of power applications. This dual, surface mount SO-8 can dramatically reduce board space and is also available in Tape & Reel.



Absolute Maximum Ratings

Parameter		Max.		Units
		N-Channel	P-Channel	
$I_D @ T_A = 25^\circ\text{C}$	10 Sec. Pulse Drain Current, $V_{GS} @ 10\text{V}$	4.7	-3.5	A
$I_D @ T_A = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	4.0	-3.0	A
$I_D @ T_A = 70^\circ\text{C}$	Continuous Drain Current, $V_{GS} @ 10\text{V}$	3.2	-2.4	A
I_{DM}	Pulsed Drain Current $\text{\textcircled{D}}$	16	-12	A
$P_D @ T_A = 25^\circ\text{C}$	Power Dissipation (PCB Mount)**	1.4		W
	Linear Derating Factor (PCB Mount)**	0.011		W/°C
V_{GS}	Gate-to-Source Voltage	± 20		V
dv/dt	Peak Diode Recovery dv/dt $\text{\textcircled{D}}$	6.9	-6.0	V/ns
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Junction-to-Amb. (PCB Mount, steady state)**	—	—	90	°C/W

** When mounted on 1" square PCB (FR-4 or G-10 Material).

For recommended footprint and soldering techniques refer to application note #AN-994.

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

Parameter	Description	Type	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	N-Ch	30	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
		P-Ch	-30	—	—		$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	N-Ch	—	0.032	—	V/°C	Reference to $25^\circ\text{C}, I_D = 1\text{mA}$
		P-Ch	—	-0.037	—		Reference to $25^\circ\text{C}, I_D = -1\text{mA}$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	N-Ch	—	—	0.050	Ω	$V_{GS} = 10V, I_D = 2.4A$ ③
			—	—	0.080		$V_{GS} = 4.5V, I_D = 2.0A$ ③
		P-Ch	—	—	0.10		$V_{GS} = -10V, I_D = -1.8A$ ③
			—	—	0.16		$V_{GS} = -4.5V, I_D = -1.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	N-Ch	1.0	—	—	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
		P-Ch	-1.0	—	—		$V_{DS} = V_{GS}, I_D = -250\mu A$
g_{fs}	Forward Transconductance	N-Ch	5.2	—	—	S	$V_{DS} = 15V, I_D = 2.4A$ ③
		P-Ch	2.5	—	—		$V_{DS} = -24V, I_D = -1.8A$ ③
I_{DSS}	Drain-to-Source Leakage Current	N-Ch	—	—	1.0	μA	$V_{DS} = 24V, V_{GS} = 0V$
		P-Ch	—	—	-1.0		$V_{DS} = -24V, V_{GS} = 0V$
		N-Ch	—	—	25		$V_{DS} = 24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
		P-Ch	—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage	N-P	—	—	± 100	nA	$V_{GS} = \pm 20V$
Q_g	Total Gate Charge	N-Ch	—	—	25	nC	N-Channel $I_D = 2.6A, V_{DS} = 16V, V_{GS} = 4.5V$ ③
		P-Ch	—	—	25		
Q_{gs}	Gate-to-Source Charge	N-Ch	—	—	2.9	nC	P-Channel $I_D = -2.2A, V_{DS} = -16V, V_{GS} = -4.5V$
		P-Ch	—	—	2.9		
Q_{gd}	Gate-to-Drain ("Miller") Charge	N-Ch	—	—	7.9	nC	P-Channel $I_D = -2.2A, V_{DS} = -16V, V_{GS} = -4.5V$
		P-Ch	—	—	9.0		
$t_{d(on)}$	Turn-On Delay Time	N-Ch	—	6.8	—	ns	N-Channel $V_{DD} = 10V, I_D = 2.6A, R_G = 6.0\Omega, R_D = 3.8\Omega$ ③
		P-Ch	—	11	—		
t_r	Rise Time	N-Ch	—	21	—	ns	P-Channel $V_{DD} = -10V, I_D = -2.2A, R_G = 6.0\Omega, R_D = 4.5\Omega$ ③
		P-Ch	—	17	—		
$t_{d(off)}$	Turn-Off Delay Time	N-Ch	—	22	—	ns	P-Channel $V_{DD} = -10V, I_D = -2.2A, R_G = 6.0\Omega, R_D = 4.5\Omega$ ③
		P-Ch	—	25	—		
t_f	Fall Time	N-Ch	—	7.7	—	ns	P-Channel $V_{DD} = -10V, I_D = -2.2A, R_G = 6.0\Omega, R_D = 4.5\Omega$ ③
		P-Ch	—	18	—		
L_D	Internal Drain Inductance	N-P	—	4.0	—	nH	Between lead tip and center of die contact
L_S	Internal Source Inductance	N-P	—	6.0	—		
C_{ISS}	Input Capacitance	N-Ch	—	520	—	pF	N-Channel $V_{GS} = 0V, V_{DS} = 15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	440	—		
C_{OSS}	Output Capacitance	N-Ch	—	180	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$ ③
		P-Ch	—	200	—		
C_{RSS}	Reverse Transfer Capacitance	N-Ch	—	72	—	pF	P-Channel $V_{GS} = 0V, V_{DS} = -15V, f = 1.0\text{MHz}$ ③
P-Ch	—	93	—				

Source-Drain Ratings and Characteristics

Parameter	Description	Type	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	N-Ch	—	—	1.8	A	
		P-Ch	—	—	-1.8		
I_{SM}	Pulsed Source Current (Body Diode) ①	N-Ch	—	—	16	A	
		P-Ch	—	—	-12		
V_{SD}	Diode Forward Voltage	N-Ch	—	—	1.0	V	$T_J = 25^\circ\text{C}, I_S = 1.8A, V_{GS} = 0V$ ③
		P-Ch	—	—	-1.0		$T_J = 25^\circ\text{C}, I_S = -1.8A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time	N-Ch	—	47	71	ns	N-Channel $T_J = 25^\circ\text{C}, I_F = 2.6A, di/dt = 100A/\mu s$
		P-Ch	—	53	80		
Q_{rr}	Reverse Recovery Charge	N-Ch	—	56	94	nC	P-Channel $T_J = 25^\circ\text{C}, I_F = -2.2A, di/dt = 100A/\mu s$ ③
		P-Ch	—	66	99		
t_{on}	Forward Turn-On Time	N-P	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)				

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 23)

② N-Channel $I_{SD} \leq 2.4A, di/dt \leq 73A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$
P-Channel $I_{SD} \leq -1.8A, di/dt \leq 90A/\mu s, V_{DD} \leq V_{(BR)DSS}, T_J \leq 150^\circ\text{C}$

③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.

N-Channel

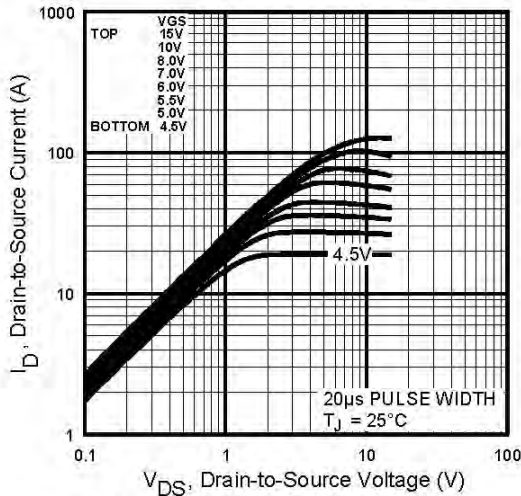


Fig 1. Typical Output Characteristics,
 $T_J = 25^\circ\text{C}$

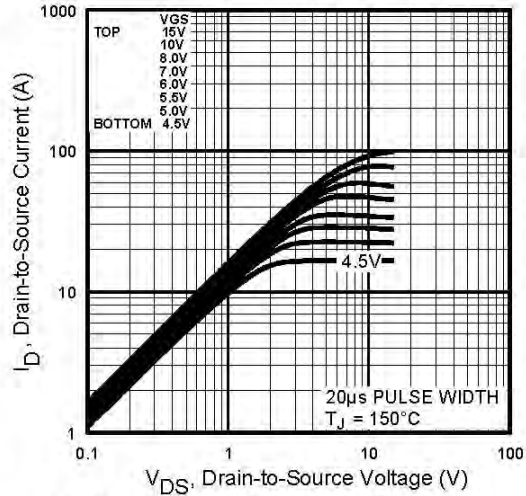


Fig 2. Typical Output Characteristics,
 $T_J = 150^\circ\text{C}$

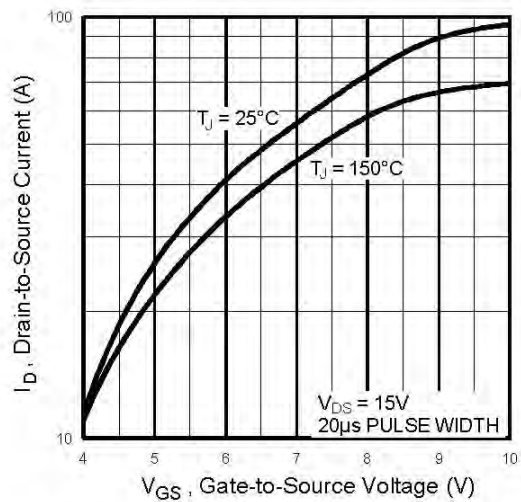


Fig 3. Typical Transfer Characteristics

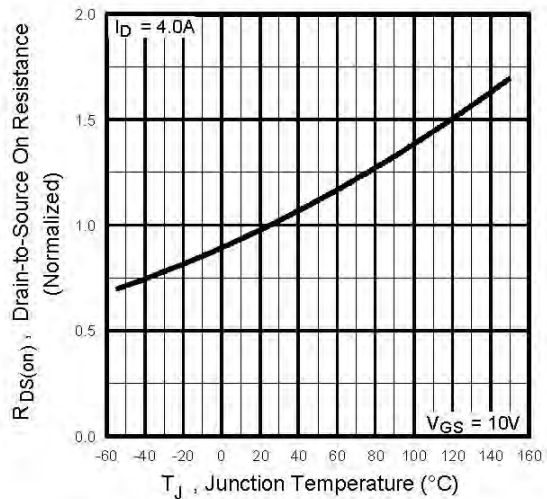


Fig 4. Normalized On-Resistance
Vs. Temperature

N-Channel

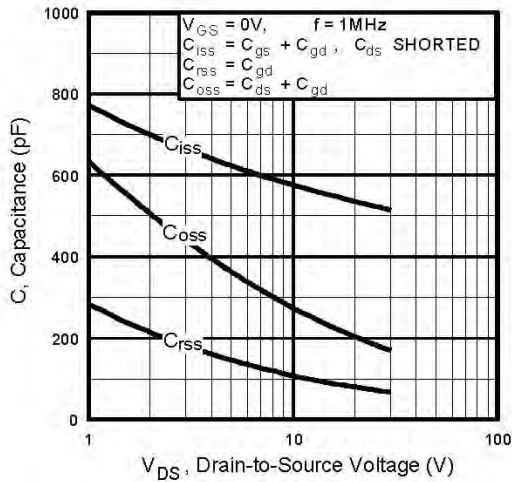


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

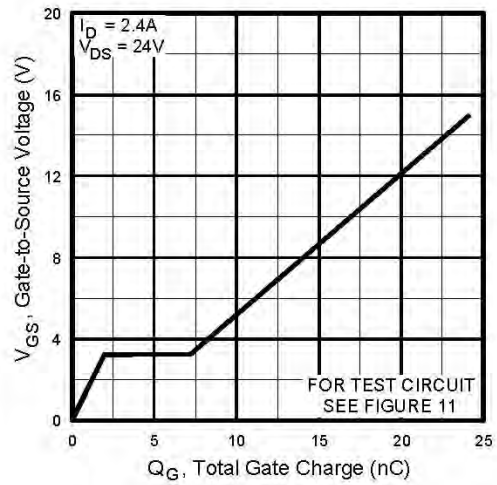


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

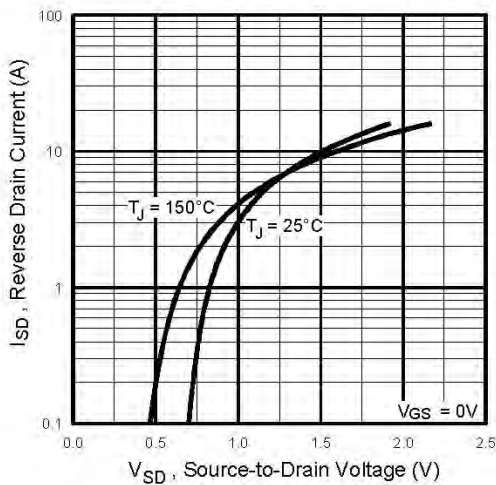


Fig 7. Typical Source-Drain Diode Forward Voltage

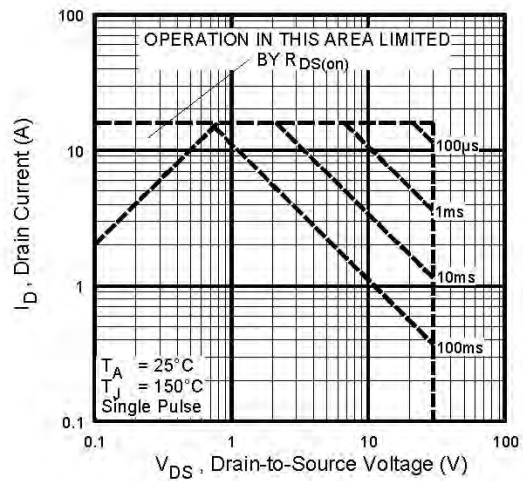


Fig 8. Maximum Safe Operating Area

N-Channel

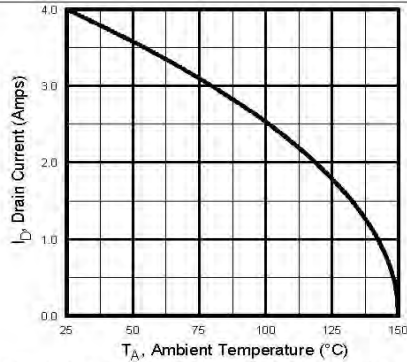


Fig 9. Max. Drain Current Vs. Ambient Temp.

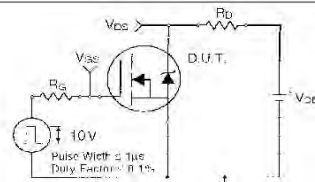


Fig 10a. Switching Time Test Circuit

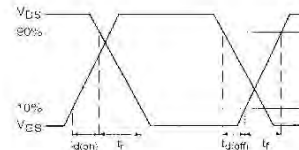


Fig 10b. Switching Time Waveforms

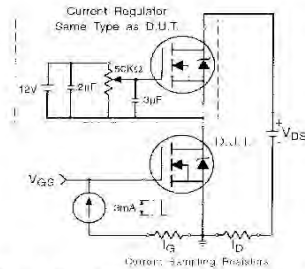


Fig 11a. Gate Charge Test Circuit

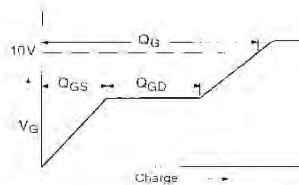


Fig 11b. Basic Gate Charge Waveform

P-Channel

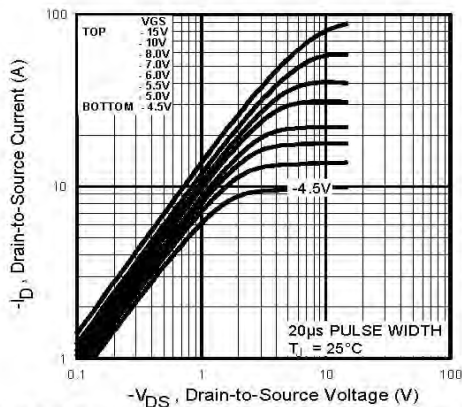


Fig 12. Typical Output Characteristics, $T_J = 25^\circ\text{C}$

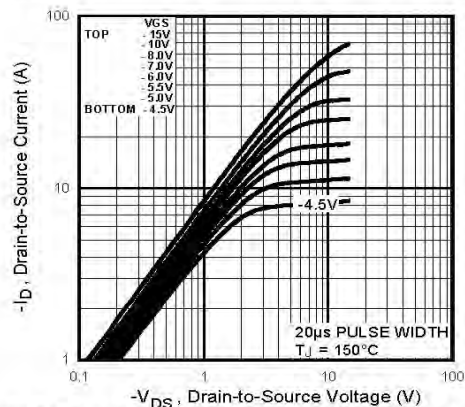


Fig 13. Typical Output Characteristics, $T_J = 150^\circ\text{C}$

P-Channel

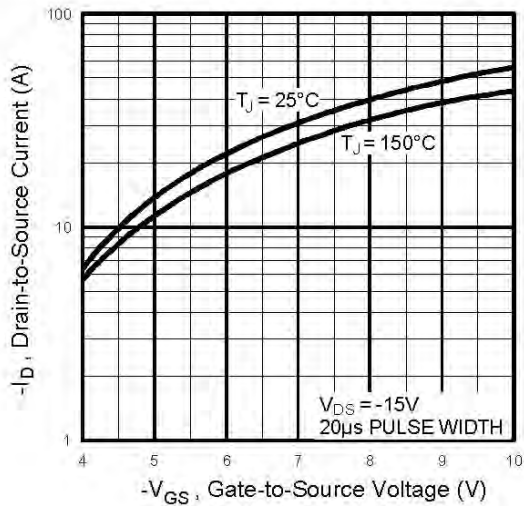


Fig 14. Typical Transfer Characteristics

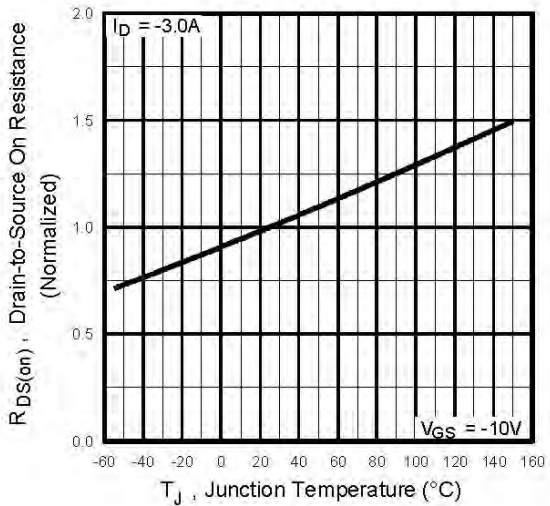


Fig 15. Normalized On-Resistance Vs. Temperature

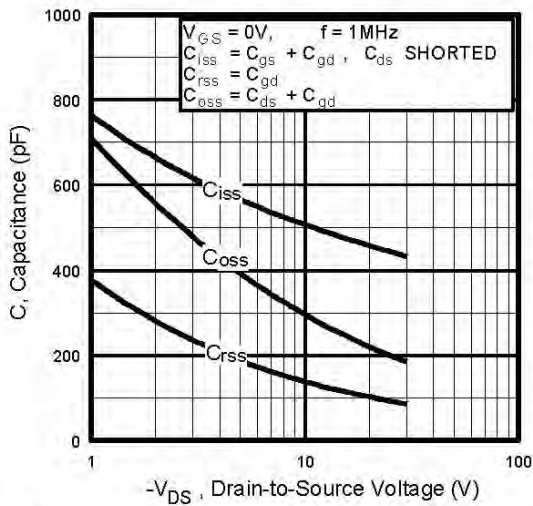


Fig 16. Typical Capacitance Vs. Drain-to-Source Voltage

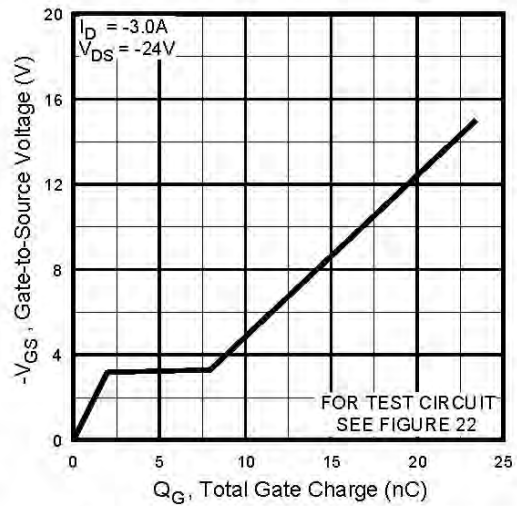


Fig 17. Typical Gate Charge Vs. Gate-to-Source Voltage

P-Channel

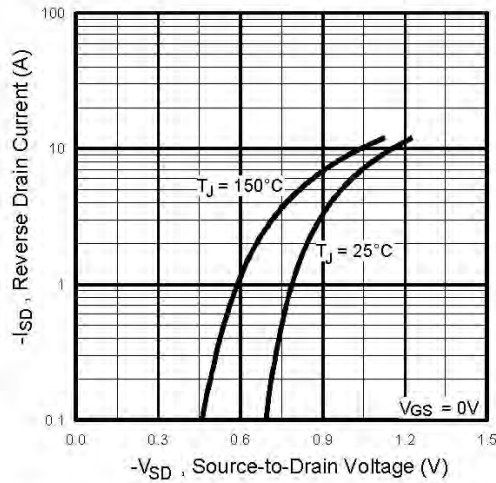


Fig 18. Typical Source-Drain Diode Forward Voltage

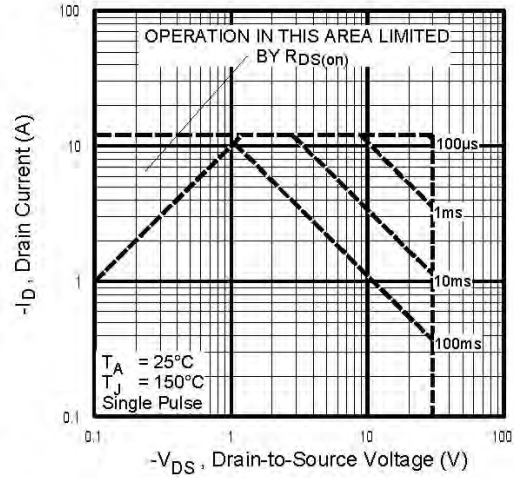


Fig 19. Maximum Safe Operating Area

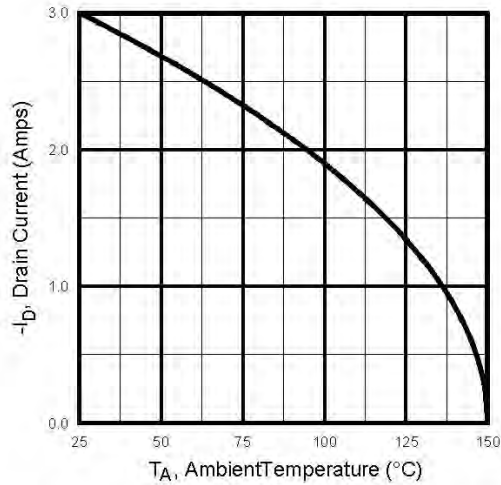


Fig 20. Max. Drain Current Vs. Ambient Temp.

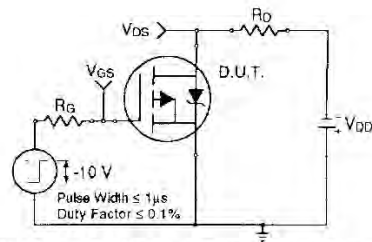


Fig 21a. Switching Time Test Circuit

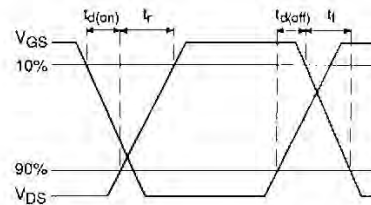


Fig 21b. Switching Time Waveforms

P-Channel

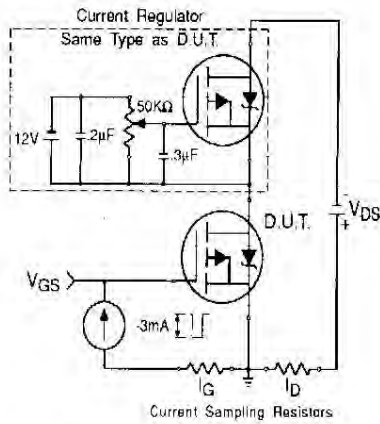


Fig 22b. Gate Charge Test Circuit

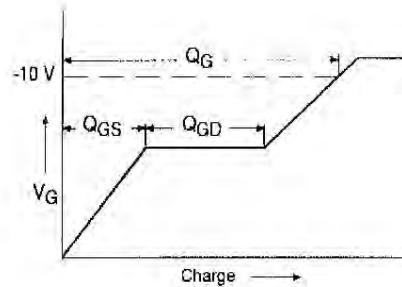


Fig 22b. Basic Gate Charge Waveform

N- and P-Channel

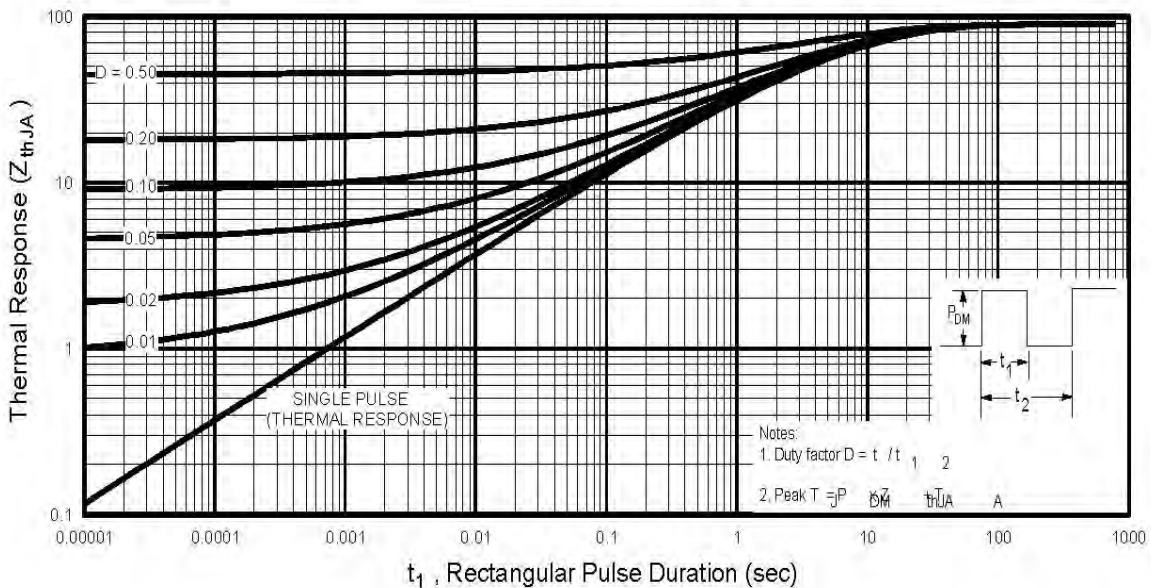
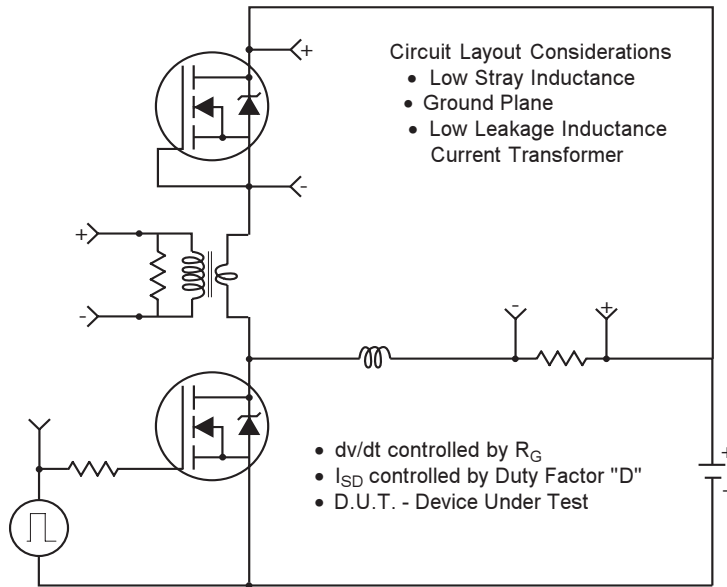


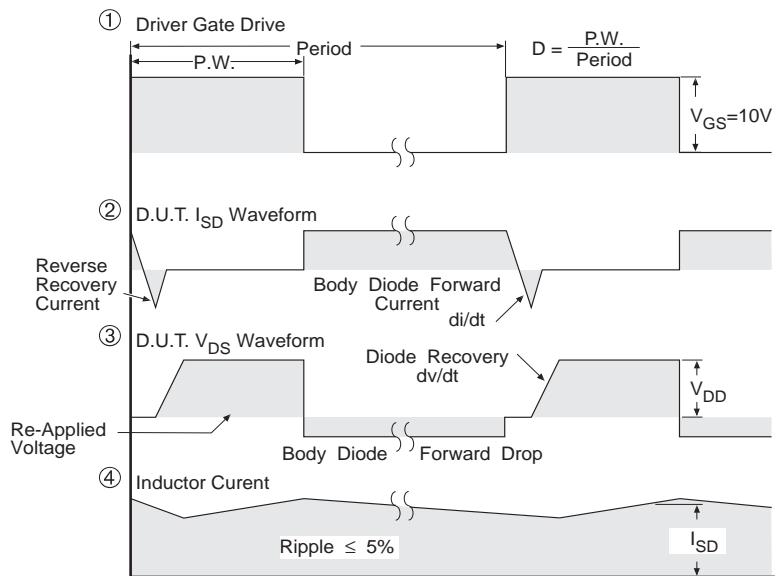
Fig 23. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

Peak Diode Recovery dv/dt Test Circuit



* Reverse Polarity for P-Channel

** Use P-Channel Driver for P-Channel Measurements



*** $V_{GS} = 5.0V$ for Logic Level and 3V Drive Devices

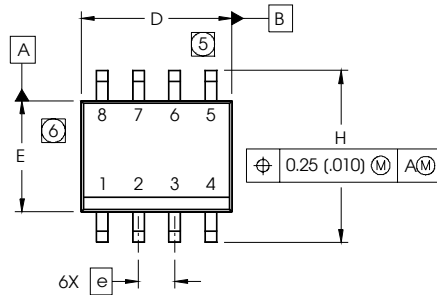
Fig 24. For N and P Channel HEXFETS

IRF7309QPbF

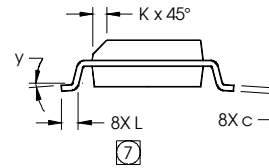
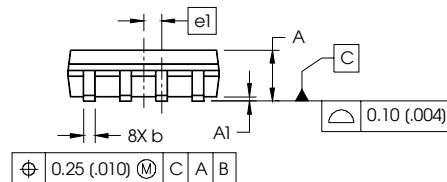
International
IR Rectifier

SO-8 Package Outline

Dimensions are shown in millimeters (inches)



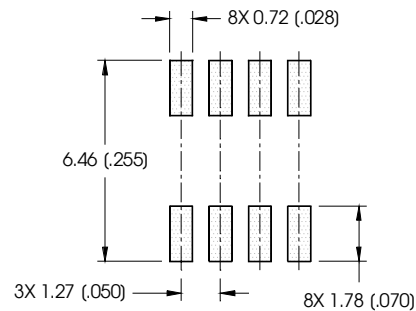
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	.0532	.0688	1.35	1.75
A1	.0040	.0098	0.10	0.25
b	.013	.020	0.33	0.51
c	.0075	.0098	0.19	0.25
D	.189	.1968	4.80	5.00
E	.1497	.1574	3.80	4.00
e	.050 BASIC		1.27 BASIC	
e1	.025 BASIC		0.635 BASIC	
H	.2284	.2440	5.80	6.20
K	.0099	.0196	0.25	0.50
L	.016	.050	0.40	1.27
y	0°	8°	0°	8°



NOTES:

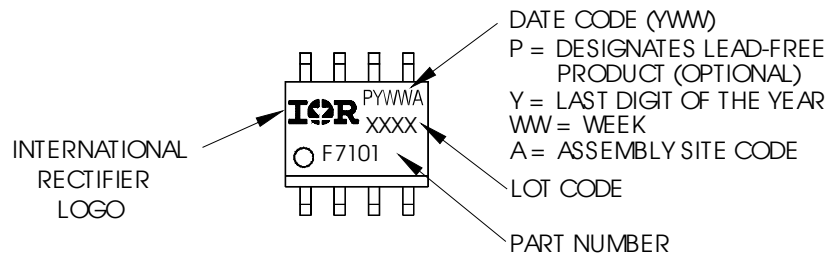
- DIMENSIONING & TOLERANCING PER ASME Y14.5M-1994.
- CONTROLLING DIMENSION: MILLIMETER
- DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
- OUTLINE CONFORMS TO JEDEC OUTLINE MS-012AA
- 5** DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.15 (.006).
- 6** DIMENSION DOES NOT INCLUDE MOLD PROTRUSIONS. MOLD PROTRUSIONS NOT TO EXCEED 0.25 (.010).
- 7** DIMENSION IS THE LENGTH OF LEAD FOR SOLDERING TO A SUBSTRATE.

FOOT PRINT



SO-8 Part Marking

EXAMPLE: THIS IS AN IRF7101 (MOSFET)

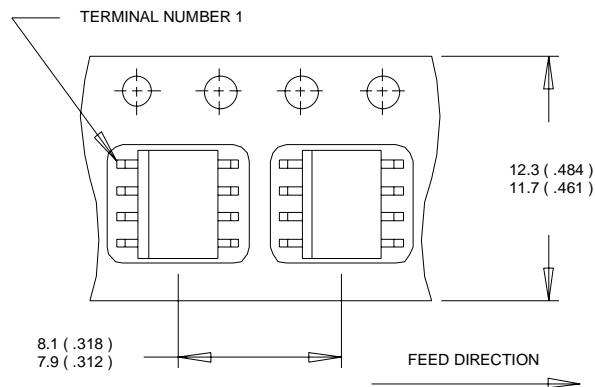


Notes:

- For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/auto/>
- For the most current drawing please refer to IR website at <http://www.irf.com/package/>

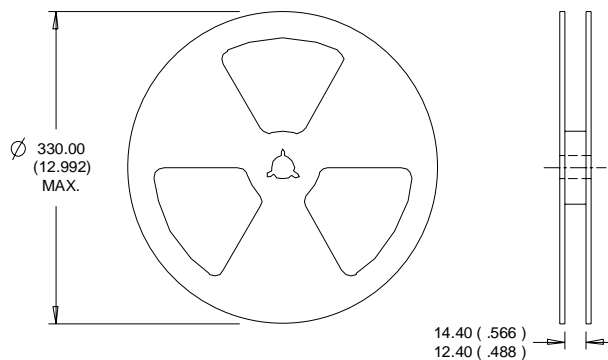
SO-8 Tape and Reel

Dimensions are shown in millimeters (inches)



NOTES:

1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS(INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :

1. CONTROLLING DIMENSION : MILLIMETER.
2. OUTLINE CONFORMS TO EIA-481 & EIA-541.

Data and specifications subject to change without notice.
 This product has been designed and qualified for the Industrial market.
 Qualification Standards can be found on IR's Web site.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View IRF7309QTRPBF on WIN SOURCE](#)

 [Infineon Technologies](#) Information

Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
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-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management