



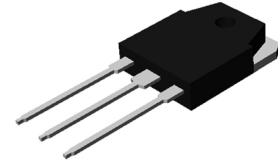
**THE DATASHEET OF
FDA59N30**



MOSFET – N-Channel, UniFET™

300 V, 59 A, 56 mΩ

FDA59N30



TO-3P-3LD / EIAJ SC-65, ISOLATED
CASE 340BZ

Description

UniFET™ MOSFET is onsemi's high voltage MOSFET family based on planar stripe and DMOS technology. This MOSFET is tailored to reduce on-state resistance, and to provide better switching performance and higher avalanche energy strength. This device family is suitable for switching power converter applications such as power factor correction (PFC), flat panel display (FPD) TV power, ATX and electronic lamp ballasts.

Features

- $R_{DS(on)} = 47 \text{ m}\Omega$ (Typ.) @ $V_{GS} = 10 \text{ V}$, $I_D = 29.5 \text{ A}$
- Low Gate Charge (Typ. 77 nC)
- Low C_{rss} (Typ. 80 pF)
- 100% Avalanche Tested

Applications

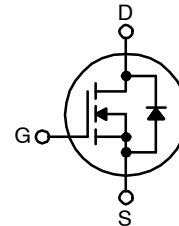
- PDP TV
- Uninterruptible Power Supply
- AC-DC Power Supply

ABSOLUTE MAXIMUM RATINGS ($T_C = 25^\circ\text{C}$ unless otherwise noted)

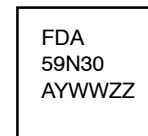
Symbol	Parameter		Value	Unit
V_{DSS}	Drain-Source Voltage		300	V
I_D	Drain Current	- Continuous ($T_C = 25^\circ\text{C}$)	59	A
		- Continuous ($T_C = 100^\circ\text{C}$)	35	A
I_{DM}	Drain Current	- Pulsed (Note 1)	236	A
V_{GSS}	Gate-Source Voltage		± 30	V
E_{AS}	Single Pulsed Avalanche Energy (Note 2)		1734	mJ
I_{AR}	Avalanche Current (Note 1)		59	A
E_{AR}	Repetitive Avalanche Energy (Note 1)		50	mJ
dv/dt	Peak Diode Recovery dv/dt (Note 3)		4.5	V/ns
P_D	Power Dissipation	($T_C = 25^\circ\text{C}$)	500	W
		- Derate Above 25°C	4	W/ $^\circ\text{C}$
T_J, T_{STG}	Operating and Storage Temperature Range		-55 to +150	$^\circ\text{C}$
T_L	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds		300	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

N-CHANNEL MOSFET



MARKING DIAGRAM



FDA59N30 = Specific Device Code
A = Assembly Location
YWW = Date Code (Year and Week)
ZZ = Assembly Lot

ORDERING INFORMATION

Device	Package	Shipping
FDA59N30	TO-3P-3L (Pb-Free)	450 Units / Tube

FDA59N30

THERMAL CHARACTERISTICS

Symbol	Parameter	Value	Unit
$R_{\theta JC}$	Thermal Resistance, Junction-to-Case, Max.	0.25	$^{\circ}\text{C}/\text{W}$
$R_{\theta JA}$	Thermal Resistance, Junction-to-Ambient, Max.	40	$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS ($T_C = 25^{\circ}\text{C}$ unless otherwise noted)

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
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OFF CHARACTERISTICS

BV_{DSS}	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	300	-	-	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$, Referenced to 25°C	-	0.3	-	$\text{V}/^{\circ}\text{C}$
I_{DSS}	Zero Gate Voltage Drain Current	$V_{DS} = 300\text{ V}, V_{GS} = 0\text{ V}$ $V_{DS} = 240\text{ V}, T_C = 125^{\circ}\text{C}$	-	-	1 10	μA μA
I_{GSSF}	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	-	-	100	nA
I_{GSSR}	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	-	-	-100	nA

ON CHARACTERISTICS

$V_{GS(th)}$	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	-	5.0	V
$R_{DS(on)}$	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 29.5\text{ A}$	-	0.047	0.056	Ω
g_{FS}	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 29.5\text{ A}$	-	52	-	S

DYNAMIC CHARACTERISTICS

C_{iss}	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$	-	3590	4670	pF
C_{oss}	Output Capacitance		-	710	920	pF
C_{rss}	Reverse Transfer Capacitance		-	80	120	pF

SWITCHING CHARACTERISTICS

$t_{d(on)}$	Turn-On Delay Time	$V_{DD} = 150\text{ V}, I_D = 59\text{ A},$ $V_{GS} = 10\text{ V}, R_G = 25\ \Omega$ (Note 4)	-	140	290	ns
t_r	Turn-On Rise Time		-	575	1160	ns
$t_{d(off)}$	Turn-Off Delay Time		-	120	250	ns
t_f	Turn-Off Fall Time		-	200	410	ns
Q_g	Total Gate Charge	$V_{DS} = 240\text{ V}, I_D = 59\text{ A}, V_{GS} = 10\text{ V}$ (Note 4)	-	77	100	nC
Q_{gs}	Gate-Source Charge		-	22	-	nC
Q_{gd}	Gate-Drain Charge		-	40	-	nC

DRAIN-SOURCE DIODE CHARACTERISTICS AND MAXIMUM RATINGS

I_S	Maximum Continuous Drain-Source Diode Forward Current	-	-	59	A	
I_{SM}	Maximum Pulsed Drain-Source Diode Forward Current	-	-	236	A	
V_{SD}	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 59\text{ A}$	-	-	1.4	V
t_{rr}	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 59\text{ A},$ $di_F/dt = 100\text{ A}/\mu\text{s}$	-	246	-	ns
Q_{rr}	Reverse Recovery Charge		-	6.9	-	μC

Product parametric performance is indicated in the Electrical Characteristics for the listed test conditions, unless otherwise noted. Product performance may not be indicated by the Electrical Characteristics if operated under different conditions.

1. Repetitive rating; pulse-width limited by maximum junction temperature.
2. $L = 0.83\text{ mH}, I_{AS} = 59\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$, starting $T_J = 25^{\circ}\text{C}$.
3. $I_{SD} \leq 59\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$, starting $T_J = 25^{\circ}\text{C}$.
4. Essentially independent of operating temperature typical characteristics.

TYPICAL PERFORMANCE CHARACTERISTICS

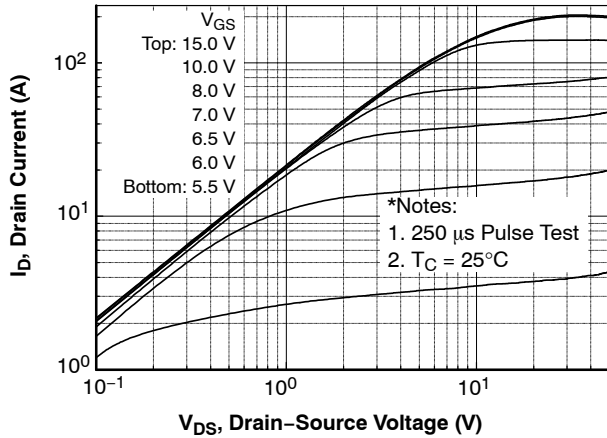


Figure 1. On-Region Characteristics

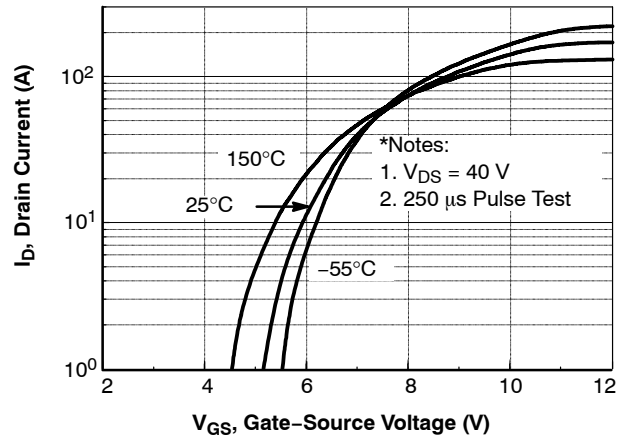


Figure 2. Transfer Characteristics

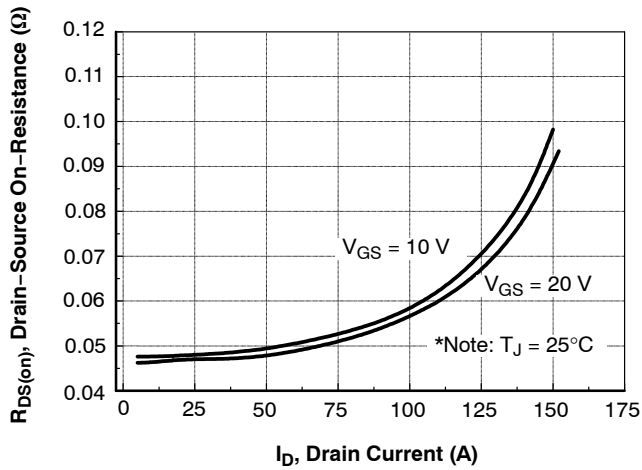


Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage

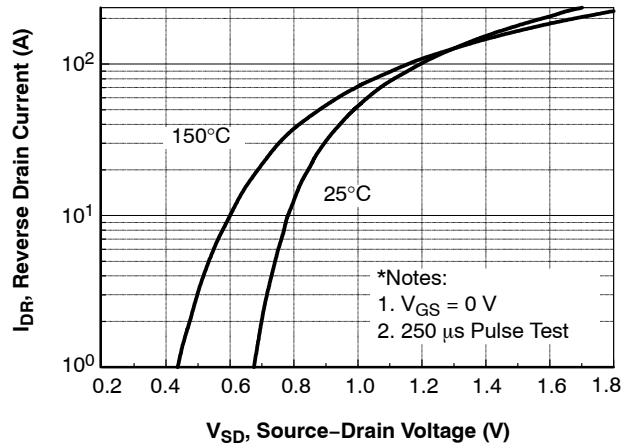


Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature

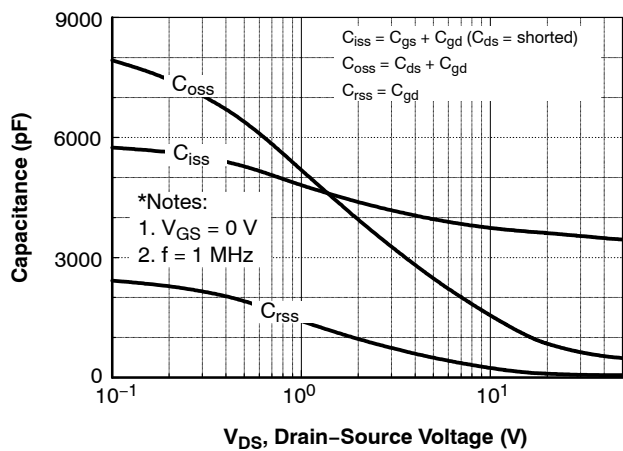


Figure 5. Capacitance Characteristics

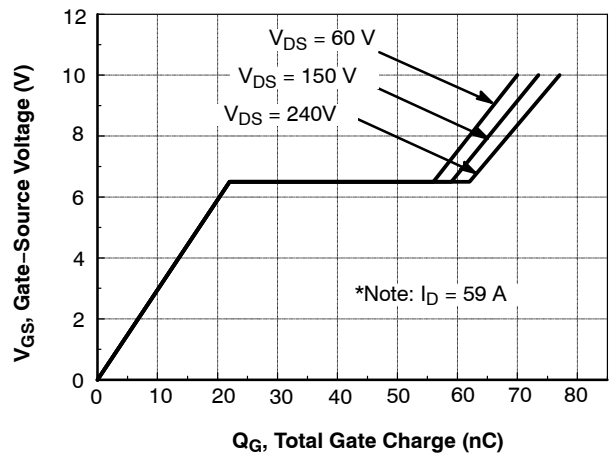


Figure 6. Gate Charge Characteristics

TYPICAL PERFORMANCE CHARACTERISTICS (continued)

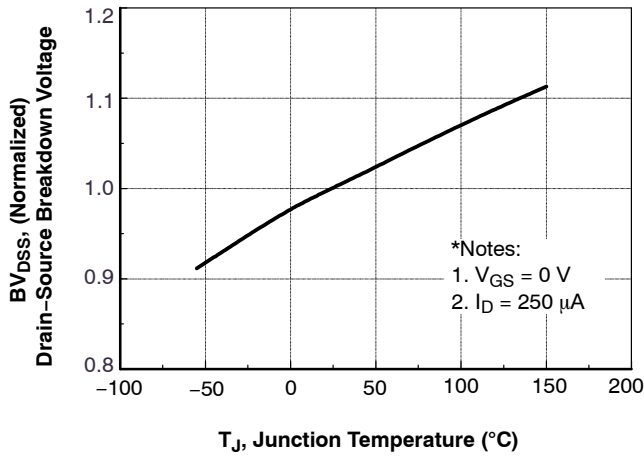


Figure 7. Breakdown Voltage Variation vs. Temperature

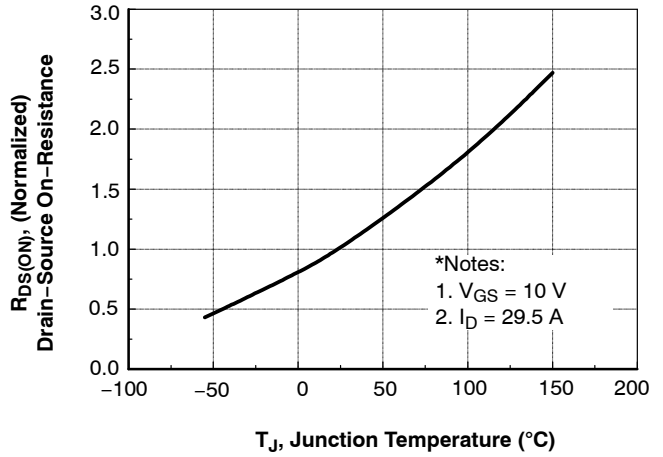


Figure 8. On-Resistance Variation vs. Temperature

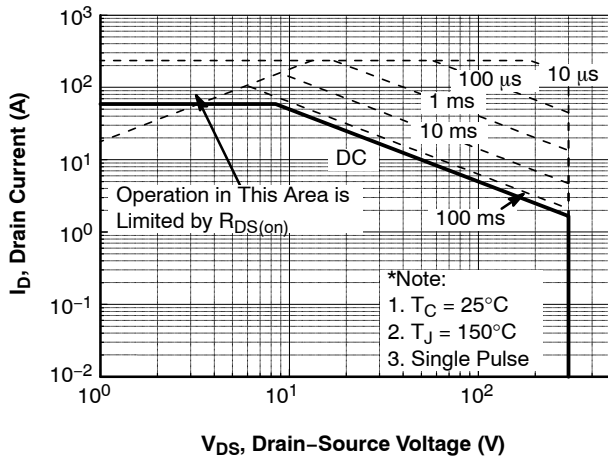


Figure 9. Maximum Safe Operating Area

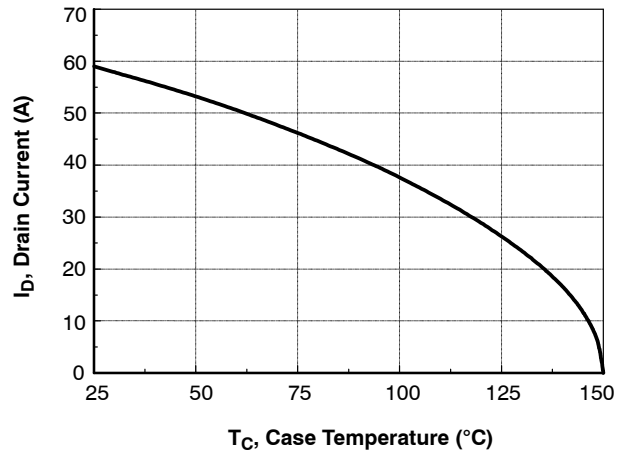


Figure 10. Maximum Drain Current vs. Case Temperature

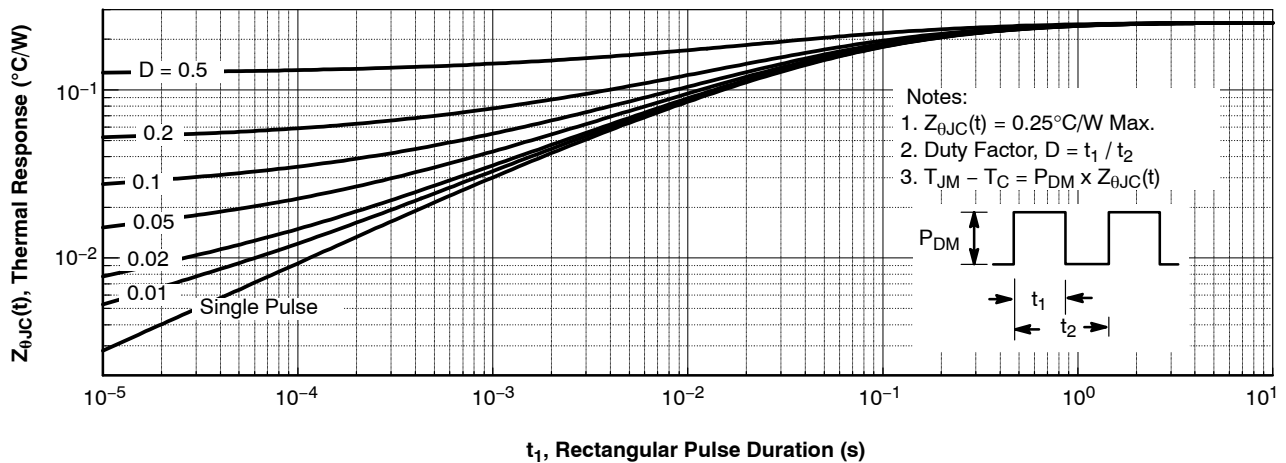


Figure 11. Transient Thermal Response Curve

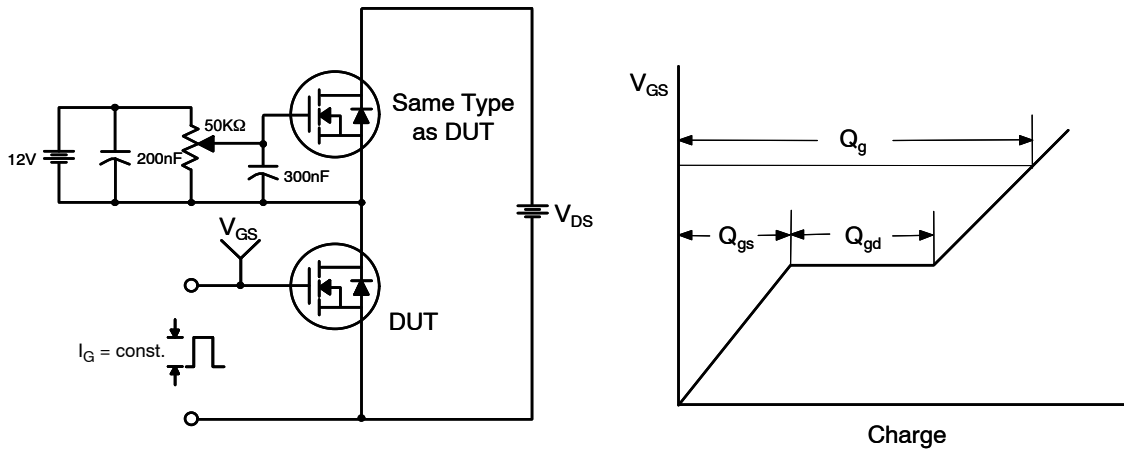


Figure 12. Gate Charge Test Circuit & Waveform

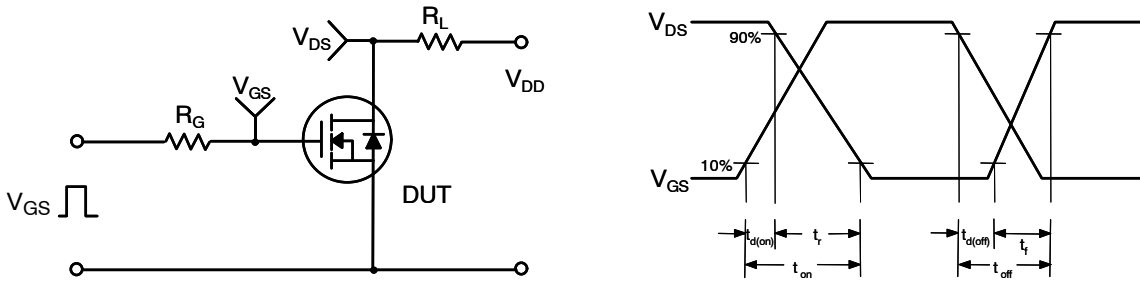


Figure 13. Resistive Switching Test Circuit & Waveforms

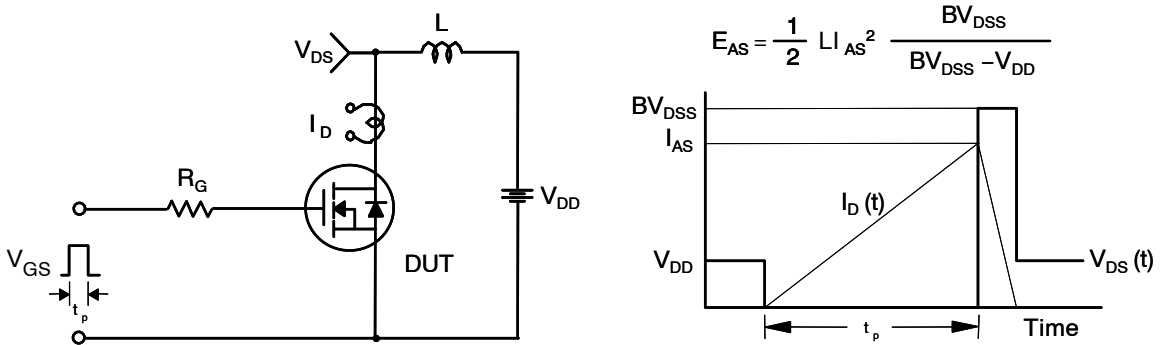


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

FDA59N30

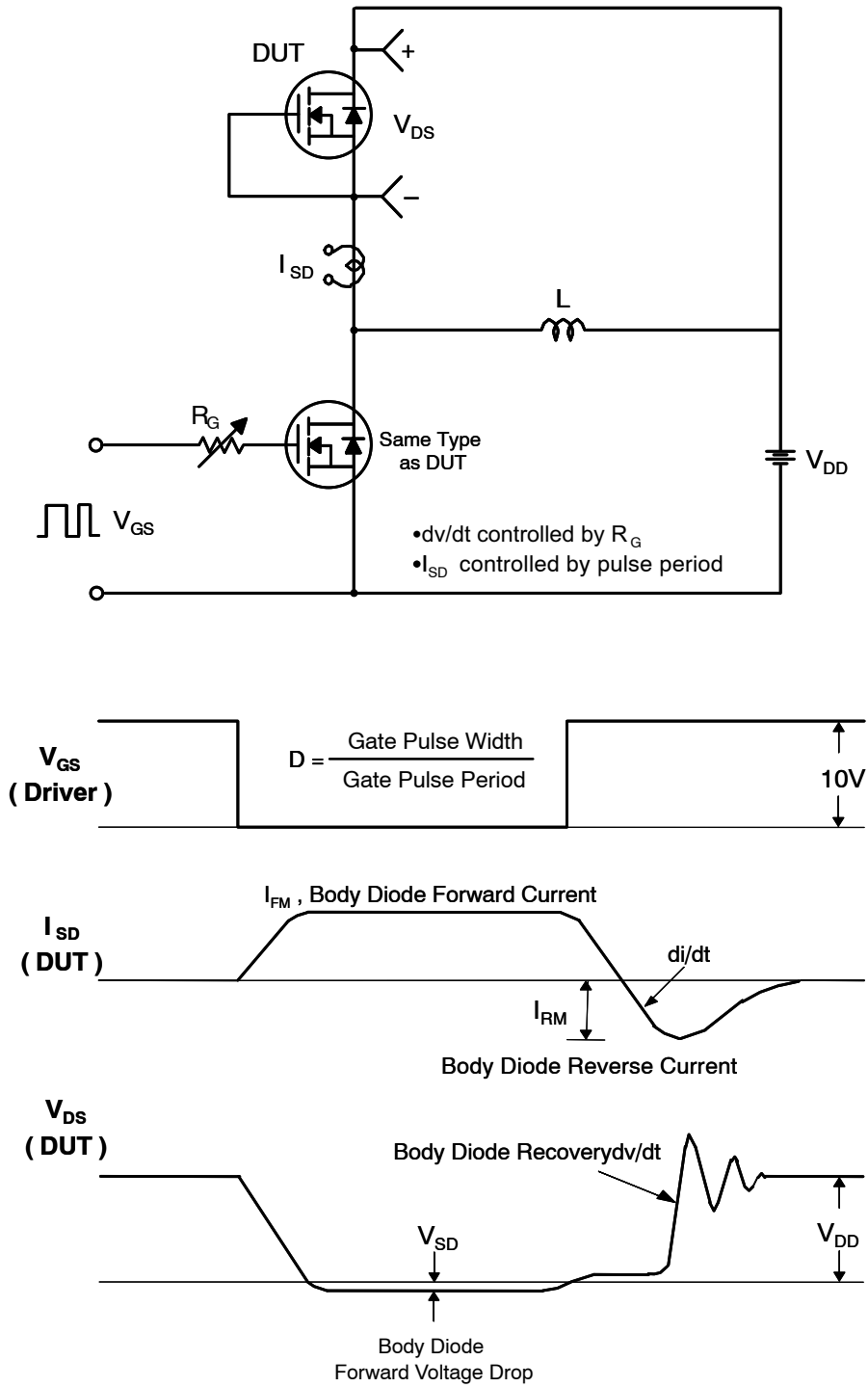


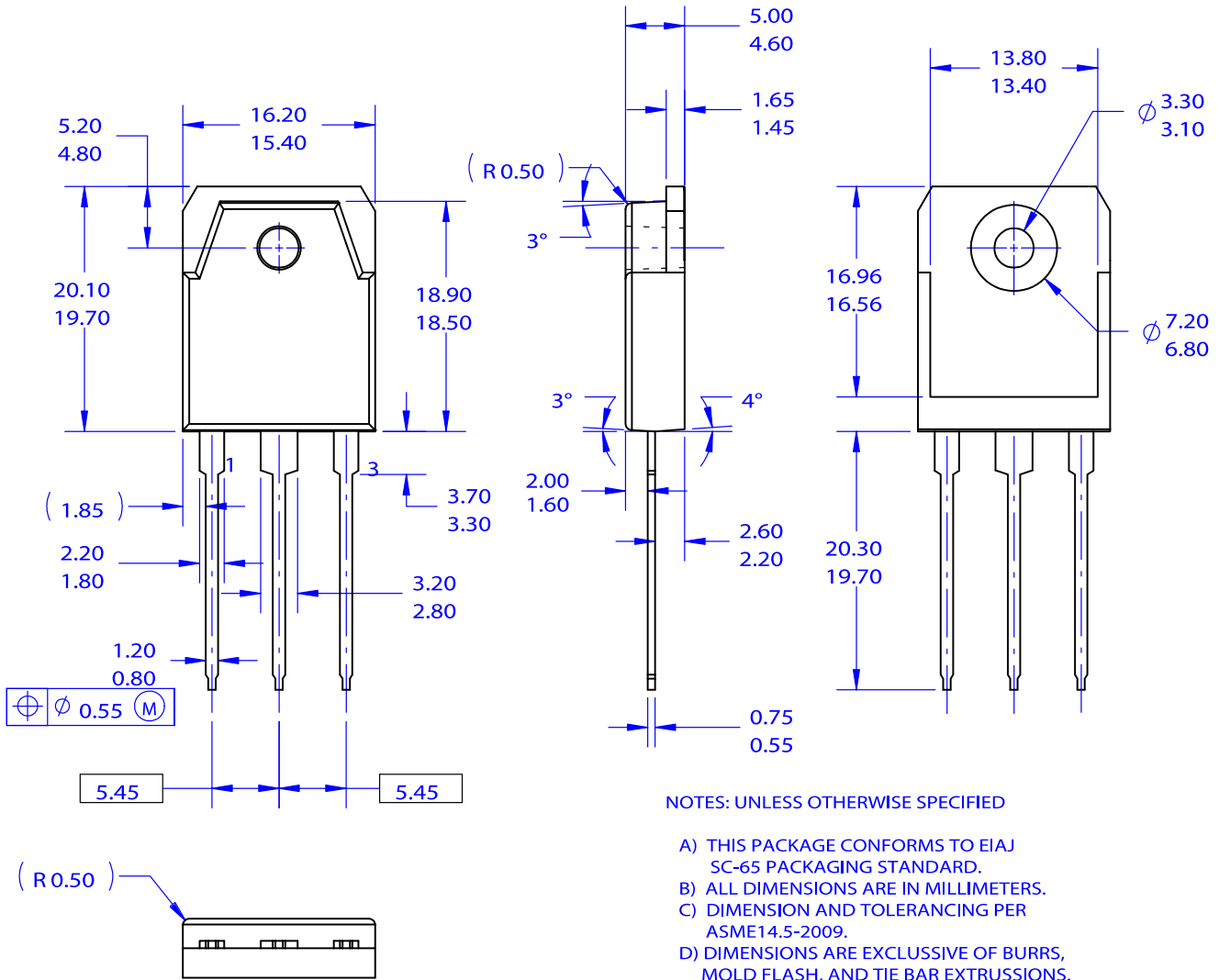
Figure 15. Peak Diode Recovery dv/dt Test Circuit & Waveforms

MECHANICAL CASE OUTLINE

PACKAGE DIMENSIONS

TO-3P-3LD / EIAJ SC-65, ISOLATED
CASE 340BZ
ISSUE O


DATE 31 OCT 2016



NOTES: UNLESS OTHERWISE SPECIFIED

- A) THIS PACKAGE CONFORMS TO EIAJ SC-65 PACKAGING STANDARD.
- B) ALL DIMENSIONS ARE IN MILLIMETERS.
- C) DIMENSION AND TOLERANCING PER ASME14.5-2009.
- D) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

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