PHP/PHB/PHD14NQ20T

TrenchMOS™ standard level FET

Rev. 03 — 11 March 2002 **Product data**

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHP14NQ20T in SOT78 (TO-220AB)

PHB14NQ20T in SOT404 (D^2-PAK)

PHD14NQ20T in SOT428 (D-PAK).

1.2 Features

- Low on-state resistance
- Fast switching

1.3 Applications

- DC to DC converters
- General purpose switching

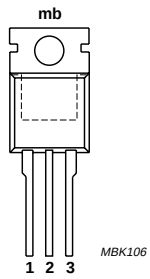
1.4 Quick reference data

- V_{DS} = 200 V
- I_D = 14 A
- $R_{DSon} \leq$ 230 mΩ
- P_D = 125 W

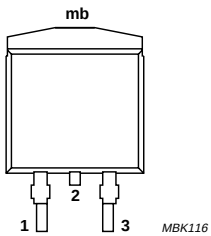
2. Pinning information

Table 1: Pinning - SOT78, SOT404, SOT428, simplified outline and symbol

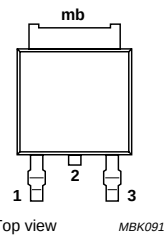
Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) [1]		
3	source (s)		
mb	mounting base, connected to drain (d)		



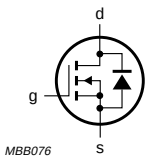
SOT78 (TO-220AB)



SOT404 (D^2-PAK)



SOT428 (D-PAK)



[1] It is not possible to make connection to pin 2 of the SOT404 or SOT428 packages.

PHILIPS

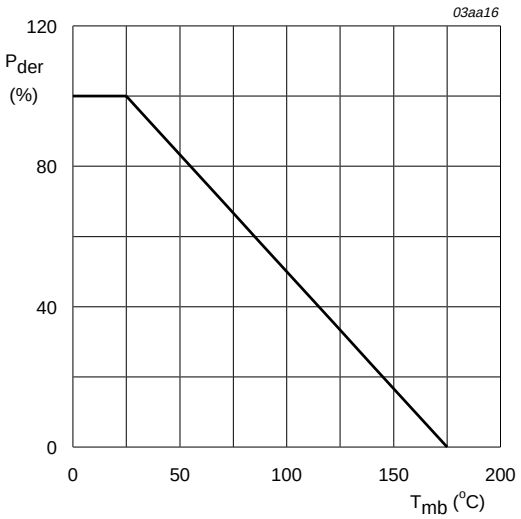
3. Limiting values

Table 2: Limiting values

In accordance with the Absolute Maximum Rating System (IEC 60134).

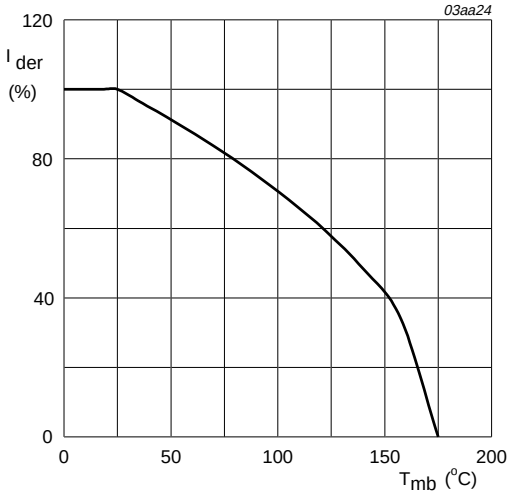
Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	T_j = 25 to 175 ºC	-	200	V
V_{DGR}	drain-gate voltage (DC)	T_j = 25 to 175 ºC; R_{GS} = 20 kΩ	-	200	V
V_{GS}	gate-source voltage		-	±20	V
I_D	drain current (DC)	V_{GS} = 10 V; Figure 2 and 3			
		T_{mb} = 25 °C	-	14	A
		T_{mb} = 100 °C	-	10	A
I_{DM}	peak drain current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs; Figure 3	-	56	A
P_{tot}	total power dissipation	T_{mb} = 25 °C; Figure 1	-	125	W
T_{stg}	storage temperature		–55	+175	°C
T_j	operating junction temperature		–55	+175	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	T_{mb} = 25 °C	-	14	A
I_{SM}	peak source (diode forward) current	T_{mb} = 25 °C; pulsed; $t_p \leq 10$ µs	-	56	A
Avalanche ruggedness					
$E_{DS(ALS)}$	non-repetitive avalanche energy	unclamped inductive load; I_D = 14 A; t_p = 20 µs; $V_{DD} \leq 25$ V; R_{GS} = 50 Ω; V_{GS} = 10 V; starting T_j = 25 °C; Figure 15	-	70	mJ
$I_{DS(ALM)}$	peak non-repetitive avalanche current		-	14	A

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

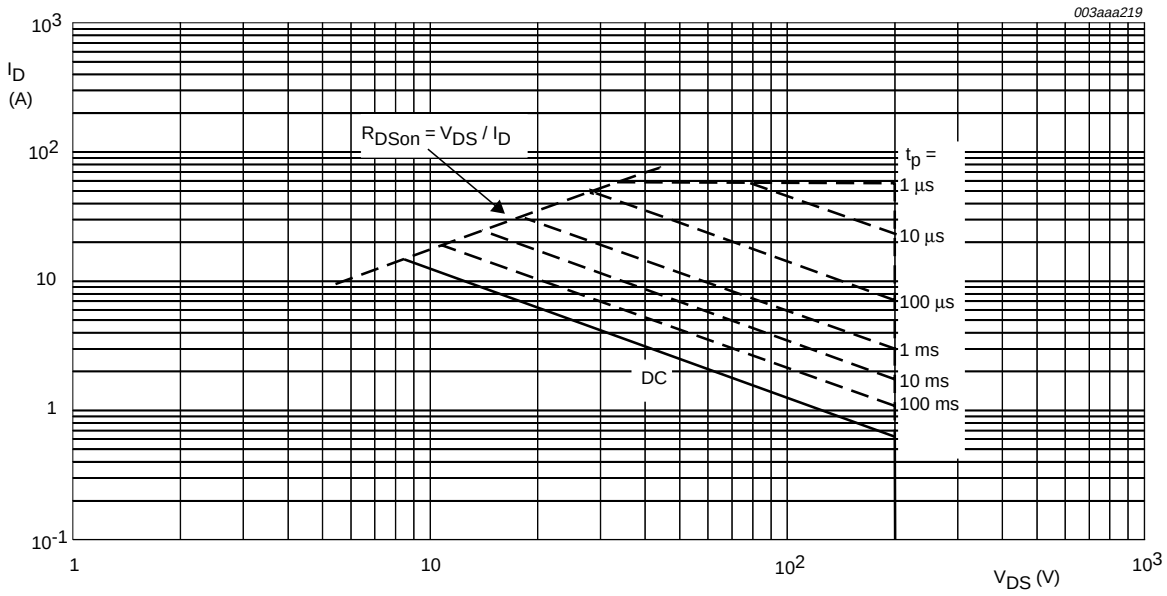
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$V_{GS} \geq 10$ V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	1.2	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	vertical in still air; SOT78 package	-	60	-	K/W
		SOT404 and SOT428 packages; SOT404 minimum footprint; mounted on a PCB	-	50	-	K/W

4.1 Transient thermal impedance

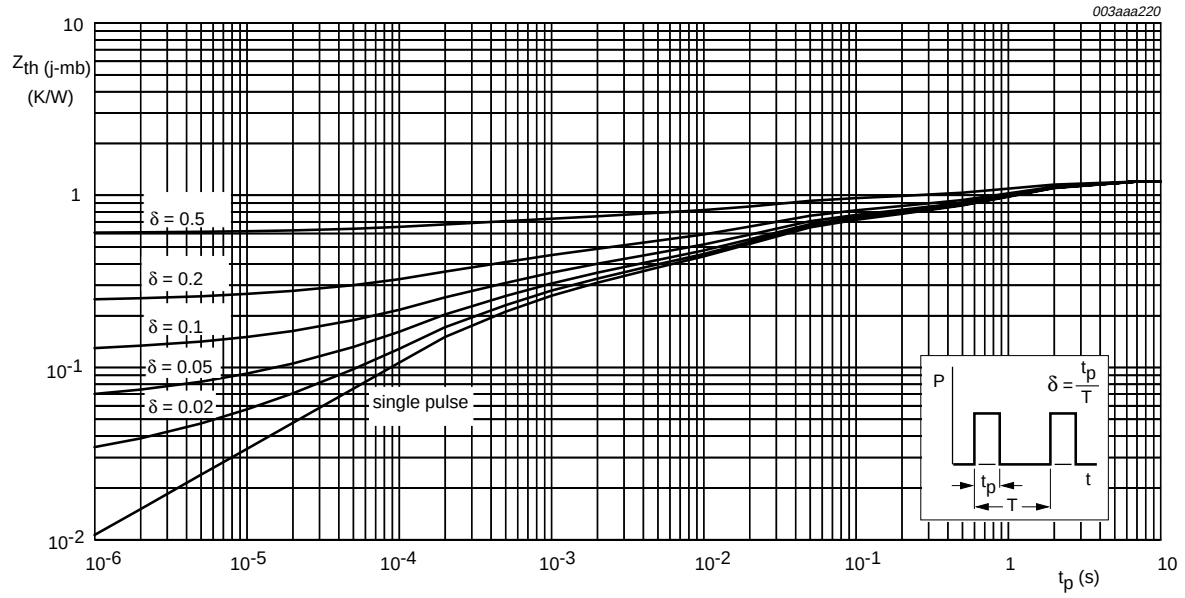


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.

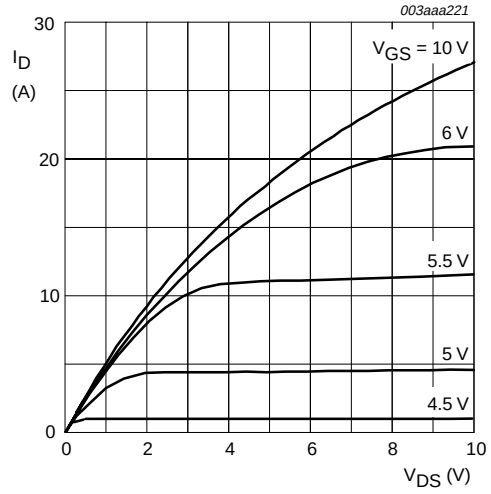
5. Characteristics

Table 4: Characteristics

T_j = 25 °C unless otherwise specified.

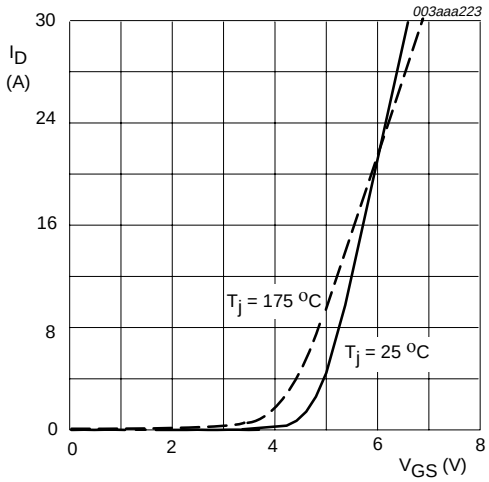
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	I_D = 250 µA; V_{GS} = 0 V				
		T_j = 25 °C	200	-	-	V
		T_j = –55 °C	178	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	I_D = 1 mA; V_{DS} = V_{GS}; Figure 9				
		T_j = 25 °C	2	3	4	V
		T_j = 175 °C	1	-	-	V
		T_j = –55 °C	-	-	6	V
I_{DSS}	drain-source leakage current	V_{DS} = 200 V; V_{GS} = 0 V				
		T_j = 25 °C	-	0.05	10	µA
		T_j = 175 °C	-	-	500	µA
I_{GSS}	gate-source leakage current	V_{GS} = ±10 V; V_{DS} = 0 V	-	10	100	nA
R_{DSon}	drain-source on-state resistance	V_{GS} = 10 V; I_D = 7 A; Figure 7 and 8				
		T_j = 25 °C	-	150	230	mΩ
		T_j = 175 °C	-	-	633	mΩ
Dynamic characteristics						
g_{fs}	forward transconductance	V_{DS} = 25 V; I_D = 7 A; Figure 14	6	12.1	-	S
$Q_{g(tot)}$	total gate charge	I_D = 14 A; V_{DD} = 160 V; V_{GS} = 10 V; Figure 13	-	38	-	nC
Q_{gs}	gate-source charge		-	4	-	nC
Q_{gd}	gate-drain (Miller) charge		-	13.3	-	nC
C_{iss}	input capacitance	V_{GS} = 0 V; V_{DS} = 25 V; f = 1 MHz; Figure 11	-	1500	-	pF
C_{oss}	output capacitance		-	128	-	pF
C_{rss}	reverse transfer capacitance		-	60	-	pF
$t_{d(on)}$	turn-on delay time	V_{DD} = 30 V; R_D = 10 Ω; V_{GS} = 10 V; R_{GS} = 50 Ω; R_{gen} = 50 Ω	-	25	-	ns
t_r	rise time		-	40	-	ns
$t_{d(off)}$	turn-off delay time		-	83	-	ns
t_f	fall time		-	31	-	ns
Source-drain diode						
V_{SD}	source-drain (diode forward) voltage	I_S = 14 A; V_{GS} = 0 V; Figure 12	-	1.0	1.5	V
t_{rr}	reverse recovery time	I_S = 14 A; dI_S/dt = –100 A/µs; V_{GS} = 0 V; V_R = 30 V	-	135	-	ns
Q_r	recovered charge		-	690	-	nC

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.



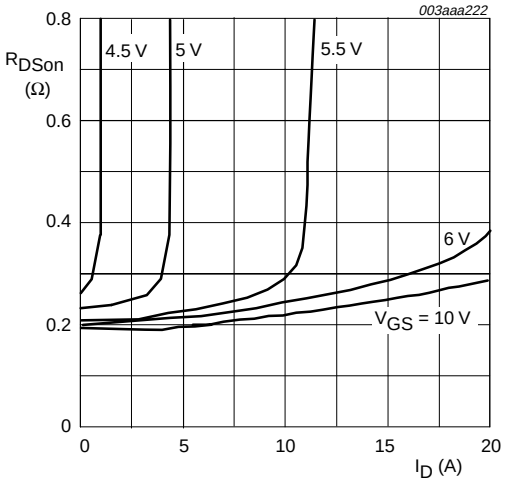
T_j = 25 °C

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



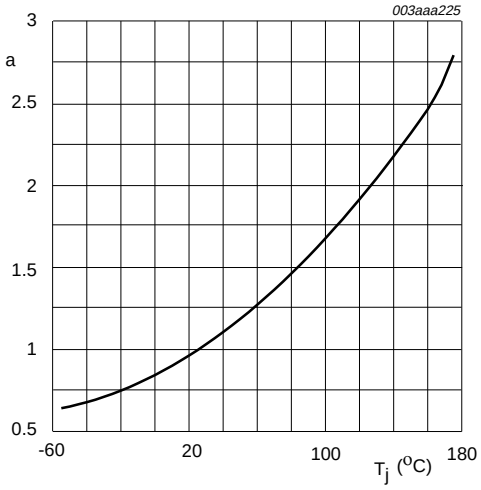
T_j = 25 °C and 175 °C; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



T_j = 25 °C

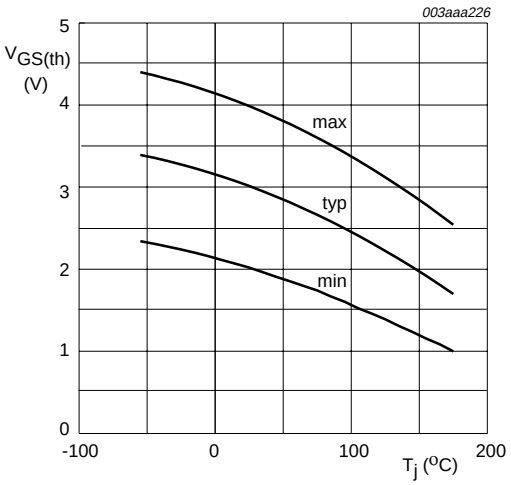
Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



$$a = \frac{R_{DSon}}{R_{DSon(25°C)}}$$

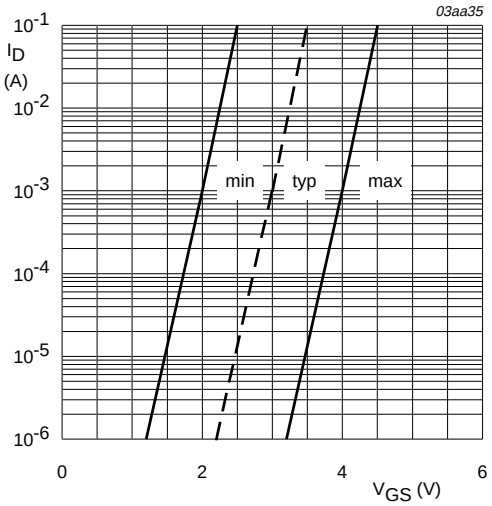
Fig 8. Normalized drain source on-state resistance factor as a function of junction temperature.

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.



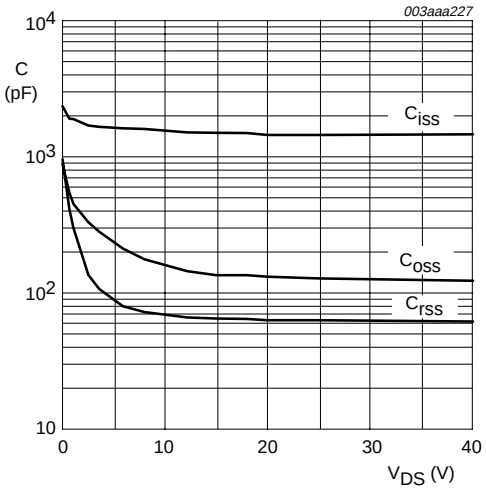
I_D = 1 mA; V_{DS} = V_{GS}

Fig 9. Gate-source threshold voltage as a function of junction temperature.



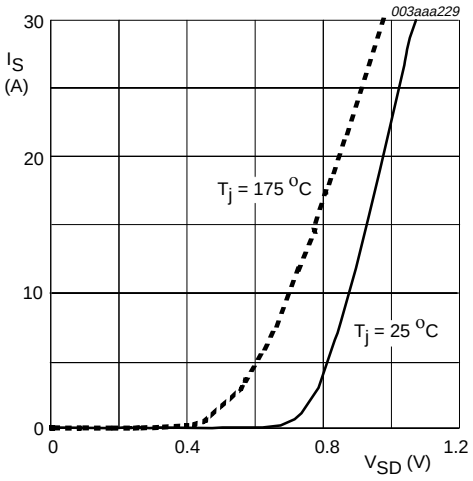
T_j = 25 °C; V_{DS} = 5 V

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



V_{GS} = 0 V; f = 1 MHz

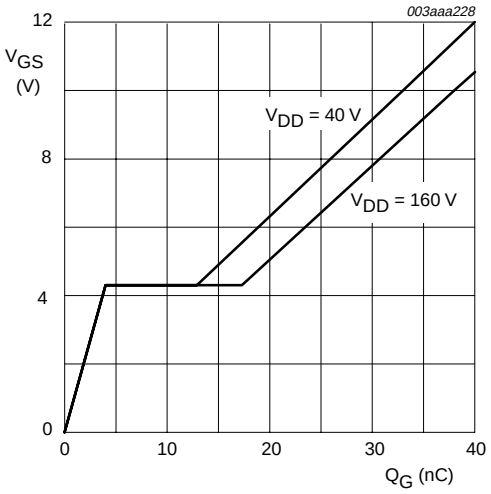
Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



T_j = 25 °C and 175 °C; V_{GS} = 0 V

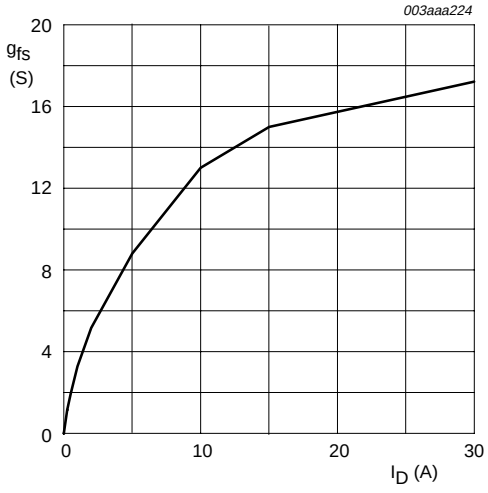
Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.



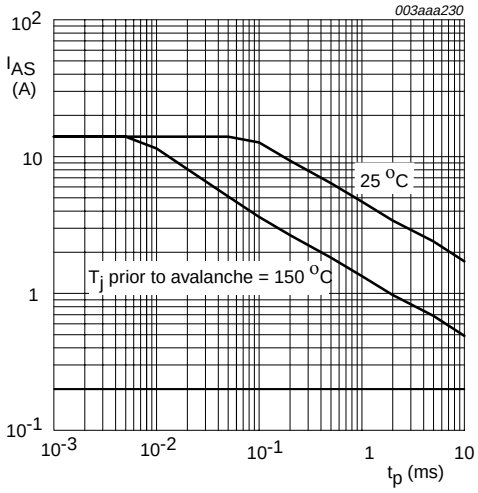
I_D = 15 A; V_{DD} = 40 V and 160 V

Fig 13. Gate-source voltage as a function of gate charge; typical values.



V_{DS} = 25 V

Fig 14. Forward transconductance as a function of drain current; typical values.



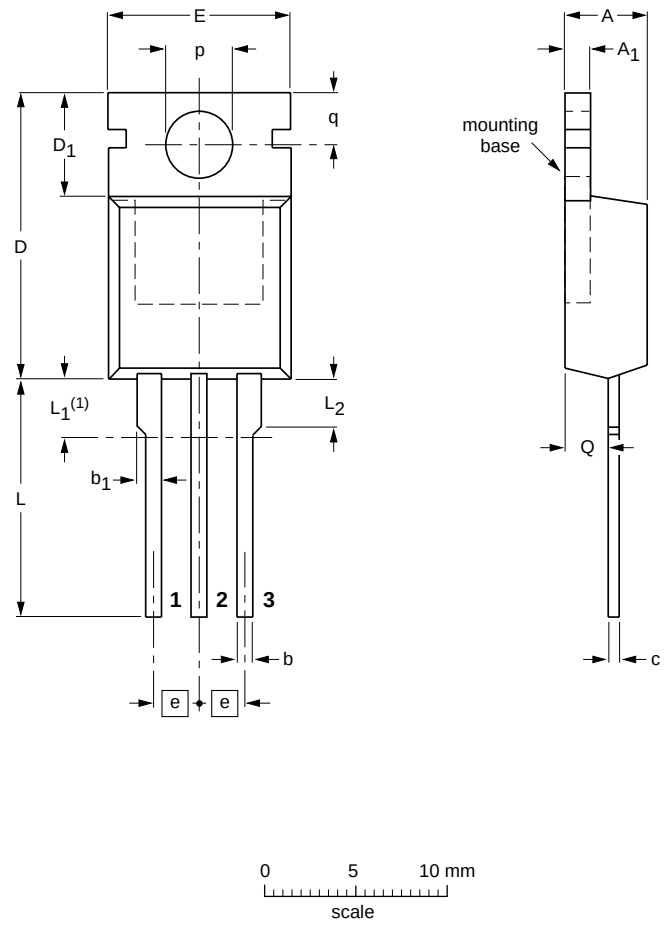
Unclamped inductive load; $V_{DD} \leq 25$ V; $R_{GS} = 50\ \Omega$; $V_{GS} = 10$ V; starting $T_j = 25$ °C and 150 °C

Fig 15. Non-repetitive avalanche ruggedness current as a function of pulse duration; typical values.

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.

6. Package outline

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB **SOT78**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	b_1	c	D	D_1	E	e	L	L_1(1)	L_2 max.	p	q	Q
mm	4.5 4.1	1.39 1.27	0.9 0.7	1.3 1.0	0.7 0.4	15.8 15.2	6.4 5.9	10.3 9.7	2.54	15.0 13.5	3.30 2.79	3.0	3.8 3.6	3.0 2.7	2.6 2.2

Note

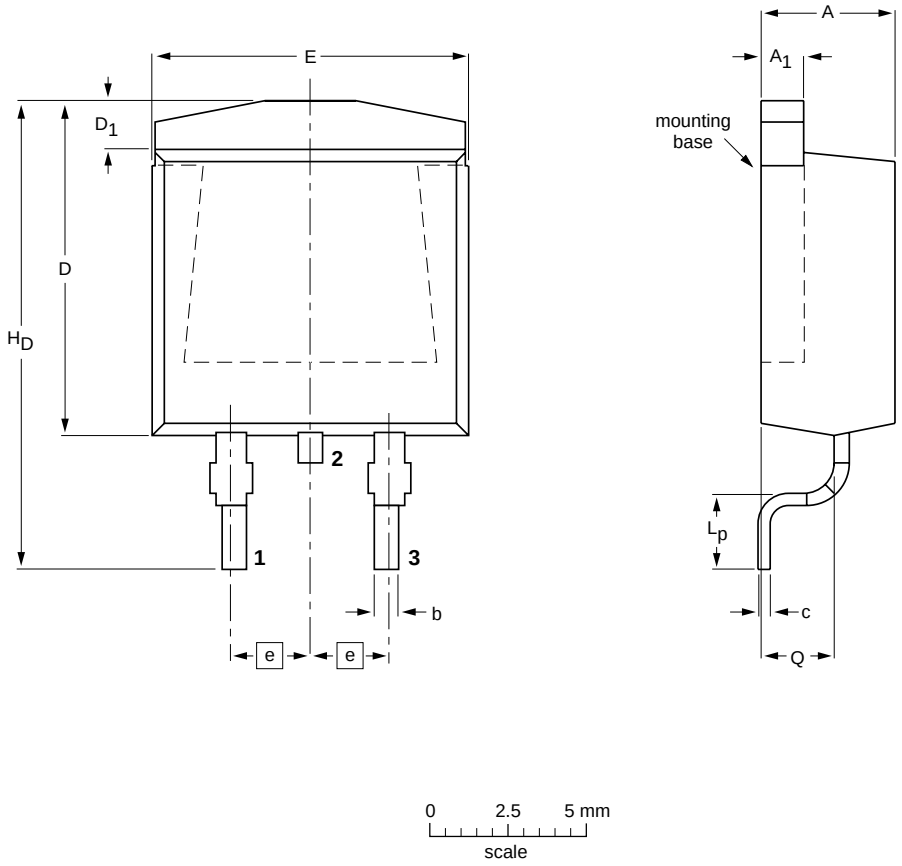
1. Terminals in this zone are not tinned.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT78		3-lead TO-220AB	SC-46			~~00-09-07~~ 01-02-16

Fig 16. SOT78 (TO-220AB).

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.

Plastic single-ended surface mounted package (Philips version of D²-PAK); 3 leads (one lead cropped) **SOT404**



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1	b	c	D max.	D_1	E	e	L_p	H_D	Q
mm	4.50 4.10	1.40 1.27	0.85 0.60	0.64 0.46	11	1.60 1.20	10.30 9.70	2.54	2.90 2.10	15.80 14.80	2.60 2.20

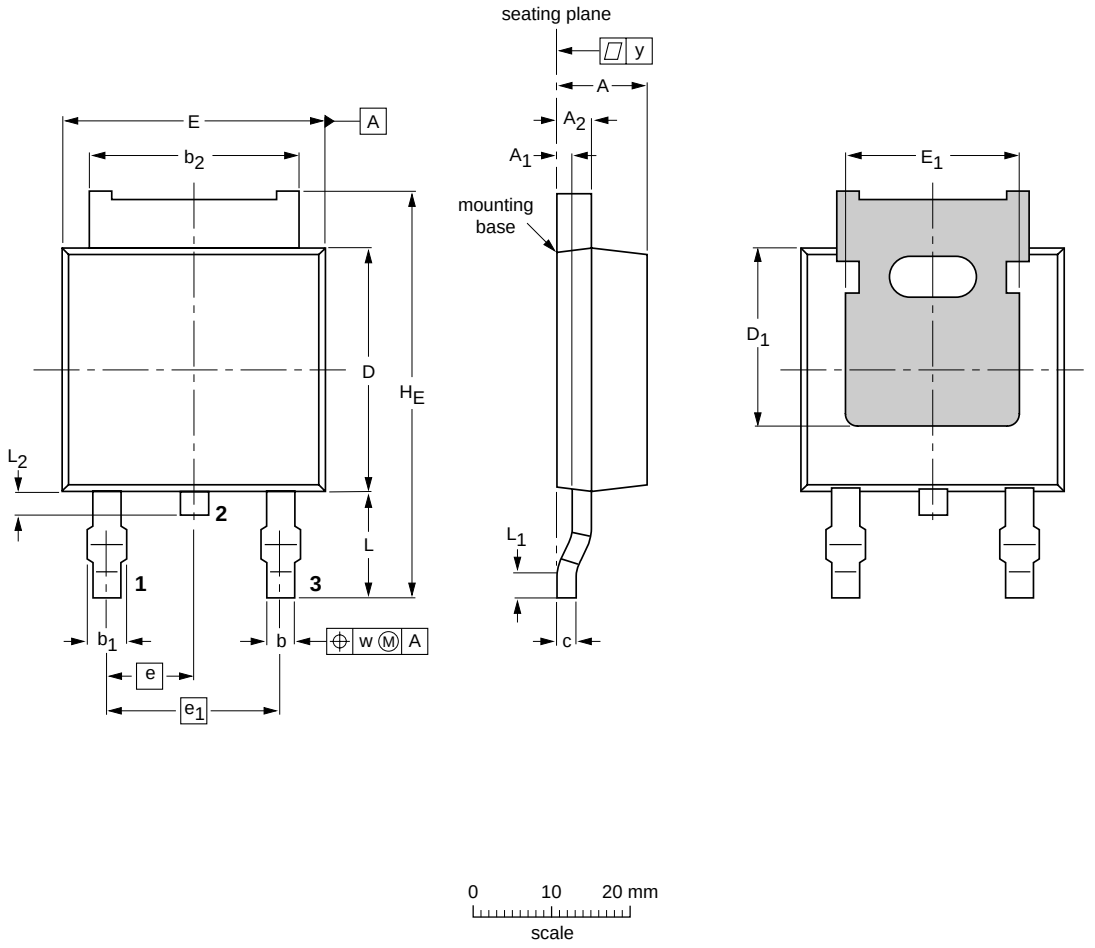
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT404						~~99-06-25~~ 01-02-12

Fig 17. SOT404 (D²-PAK).

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428



DIMENSIONS (mm are the original dimensions)

UNIT	A	A_1 (1)	A_2	b	b_1	b_2	c	D	D_1 min.	E	E_1	e	e_1	H_E	L	L_1 min.	L_2	w	y max.
mm	2.38 2.22	0.65 0.45	0.93 0.73	0.89 0.71	1.1 0.9	5.46 5.26	0.4 0.2	6.22 5.98	4.0	6.73 6.47	4.81 4.45	2.285	4.57	10.4 9.6	2.95 2.55	0.5	0.9 0.5	0.2	0.2

Note

1. Measured from heatsink back to lead.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	JEITA			
SOT428		TO-252	SC-63			~~99-09-13~~ 01-12-11

Fig 18. SOT428 (D-PAK).

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
03	20020311		**Product data; third version. Supersedes data of 6 March 2002.** **Modifications:** • Correction to product title: PHD14NQ20T.
02	20020306		**Product data; second version.Supersedes initial version of 1 October 1999.** **Modifications:** • PHD14NQ20T added.
01	19991001		**Product data; initial version**

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.

8. Data sheet status

Data sheet status[1]	Product status[2]	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL http://www.semiconductors.philips.com.

9. Definitions

Short-form specification — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

Limiting values definition — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

Application information — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

10. Disclaimers

Life support — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

Right to make changes — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

11. Trademarks

TrenchMOS — is a trademark of Koninklijke Philips Electronics N.V.

Contact information

For additional information, please visit **http://www.semiconductors.philips.com**.
For sales office addresses, send e-mail to: **sales.addresses@www.semiconductors.philips.com**. **Fax: +31 40 27 24825**

9397 750 09535

© Koninklijke Philips Electronics N.V. 2002. All rights reserved.

Contents

© Koninklijke Philips Electronics N.V. 2002.
Printed in The Netherlands

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 11 March 2002 **Document order number: 9397 750 09535**

PHILIPS

Let's make things better.

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View PHP14NQ20T,127 on WIN SOURCE
- NXP / Nexperia Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management