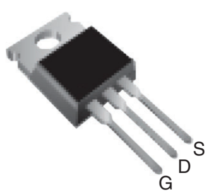
THE DATASHEET OF

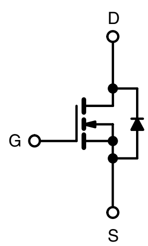
IRFB9N30A

Power MOSFET

PRODUCT SUMMARY		
V_{DS} (V)	300	
$R_{DS(on)}$ (Ω)	V_{GS} = 10 V	0.45
Q_g (Max.) (nC)	33	
Q_{gs} (nC)	6.9	
Q_{gd} (nC)	12	
Configuration	Single	

TO-220





N-Channel MOSFET

FEATURES

- Dynamic dv/dt Rating
- Repetitive Avalanche Rated
- Fast Switching
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

Pb Available
RoHS* COMPLIANT

DESCRIPTION

Third Generation Power MOSFETs from Vishay provides the designer with the best combination of fast switching, ruggedized device design, low on-resistance and cost effectiveness.
The TO-220 package is universally preferred for all commercial-industrial applications at lower dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRFB9N30APbF
	SiHFB9N30A-E3
SnPb	IRFB9N30A
	SiHFB9N30A

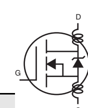
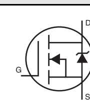
ABSOLUTE MAXIMUM RATINGS T_C = 25 °C, unless otherwise noted

PARAMETER			SYMBOL	LIMIT	UNIT
Gate-Source Voltage			V_{GS}	± 30	V
Continuous Drain Current	V_{GS} at 10 V	T_C = 25 °C	I_D	9.3	A
		T_C = 100 °C		5.9	
Pulsed Drain Current[a]			I_{DM}	37	
Linear Derating Factor				0.77	W/°C
Single Pulse Avalanche Energy[b]			E_{AS}	160	mJ
Repetitive Avalanche Current[a]			I_{AR}	9.3	A
Repetitive Avalanche Energy[a]			E_{AR}	9.6	mJ
Maximum Power Dissipation	T_C = 25 °C		P_D	96	W
Peak Diode Recovery dV/dt[c]			dV/dt	4.6	V/ns
Operating Junction and Storage Temperature Range			T_J, T_{stg}	- 55 to + 150	°C
Soldering Recommendations (Peak Temperature)	for 10 s			300[d]	
Mounting Torque	6-32 or M3 screw			10	lbf · in
				1.1	N · m

Notes
a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
b. Starting T_J = 25 °C, L = 3.7 mH, R_G = 25 Ω, I_{AS} = 9.3 A (see fig. 12).
c. $I_{SD} \leq$ 9.3 A, dI/dt $\leq$ 270 A/μs, $V_{DD} \leq V_{DS}$, $T_J \leq$ 150 °C.
d. 1.6 mm from case.

* Pb containing terminations are not RoHS compliant, exemptions may apply

THERMAL RESISTANCE RATINGS				
PARAMETER	**SYMBOL**	**TYP.**	**MAX.**	**UNIT**
Maximum Junction-to-Ambient	R_{thJA}	-	62	°C/W
Case-to-Sink, Flat, Greased Surface	R_{thCS}	0.50	-	
Maximum Junction-to-Case (Drain)	R_{thJC}	-	1.3	

SPECIFICATIONS T_J = 25 °C, unless otherwise noted							
PARAMETER	**SYMBOL**	**TEST CONDITIONS**		**MIN.**	**TYP.**	**MAX.**	**UNIT**
Static							
Drain-Source Breakdown Voltage	V_{DS}	V_{GS} = 0 V, I_D = 250 µA		300	-	-	V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to 25 °C, I_D = 1 mA		-	0.38	-	V/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$, I_D = 250 µA		2.0	-	4.0	V
Gate-Source Leakage	I_{GSS}	V_{GS} = ± 30		-	-	± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 300 V, V_{GS} = 0 V		-	-	25	µA
		V_{DS} = 240 V, V_{GS} = 0 V, T_J = 125 °C		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	V_{GS} = 10 V	I_D = 5.6 A[b]	-	-	0.45	Ω
Forward Transconductance	g_{fs}	V_{DS} = 50 V, I_D = 5.6 A[b]		6.6	-	-	S
Dynamic							
Input Capacitance	C_{iss}	V_{GS} = 0 V, V_{DS} = 25 V f = 1.0 MHz, see fig. 5		-	920	-	pF
Output Capacitance	C_{oss}			-	160	-	
Reverse Transfer Capacitance	C_{rss}			-	8.7	-	
Output Capacitance	C_{oss}	V_{GS} = 0 V, V_{DS} = 1.0 V, f = 1.0 MHz		-	1200	-	
		V_{GS} = 0 V, V_{DS} = 240 V, f = 1.0 MHz		-	52	-	
Effective Output Capacitance	$C_{oss\ eff.}$	V_{GS} = 0 V, V_{DS} = 0 V to 240 V		-	102	-	
Total Gate Charge	Q_g	V_{GS} = 10 V	I_D = 9.3 A, V_{DS} = 240 V, see fig. 6 and 13[b]	-	-	33	nC
Gate-Source Charge	Q_{gs}			-	-	6.9	
Gate-Drain Charge	Q_{gd}			-	-	12	
Turn-On Delay Time	$t_{d(on)}$	V_{DD} = 150 V, I_D = 9.3 A R_G = 12 Ω, R_D = 16 Ω, see fig. 10[b]		-	10	-	ns
Rise Time	t_r			-	25	-	
Turn-Off Delay Time	$t_{d(off)}$			-	35	-	
Fall Time	t_f			-	29	-	
Internal Drain Inductance	L_D	Between lead, 6 mm (0.25") from package and center of 		-	4.5	-	nH
Internal Source Inductance	L_S			-	7.5	-	
Drain-Source Body Diode Characteristics							
Continuous Source-Drain Diode Current	I_S	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	9.3	A
Pulsed Diode Forward Current[a]	I_{SM}			-	-	37	
Body Diode Voltage	V_{SD}	T_J = 25 °C, I_S = 9.3 A, V_{GS} = 0 V[b]		-	-	1.5	V
Body Diode Reverse Recovery Time	t_{rr}	T_J = 25 °C, I_F = 9.3 A, di/dt = 100 A/µs[b]		-	280	420	ns
Body Diode Reverse Recovery Charge	Q_{rr}			-	1.5	2.3	µC
Forward Turn-On Time	t_{on}	Intrinsic turn-on time is negligible (turn-on is dominated by L_S and L_D)					

Notes

a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).

b. Pulse width ≤ 300 µs; duty cycle ≤ 2 %.

c. C_{oss} eff. ia a fixed capacitance that gives the same charging time as C_{oss} while V_{DS} is rising from 0 % to 80% V_{DS}

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

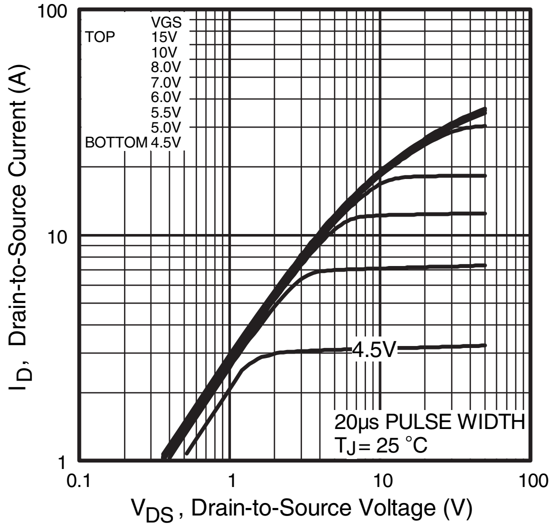


Fig. 1 - Typical Output Characteristics

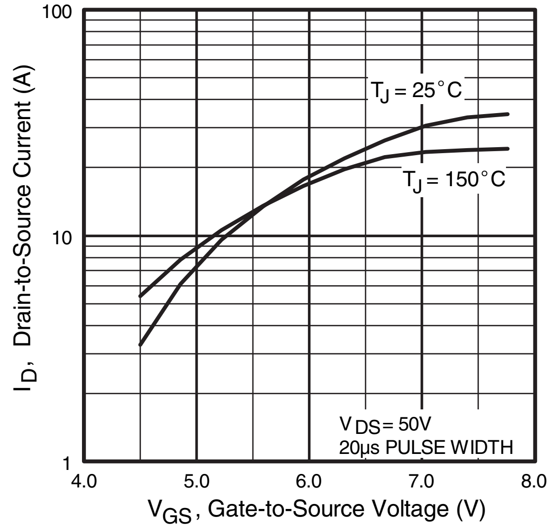


Fig. 3 - Typical Transfer Characteristics

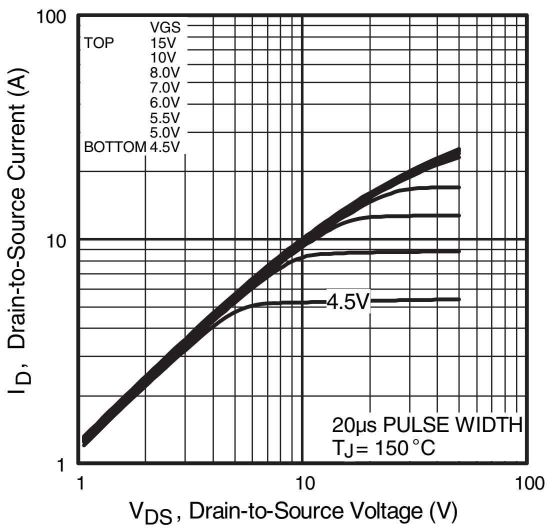


Fig. 2 - Typical Output Characteristics

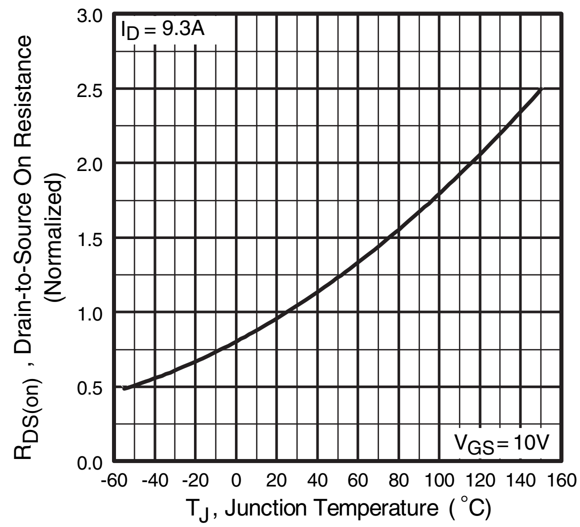


Fig. 4 - Normalized On-Resistance vs. Temperature

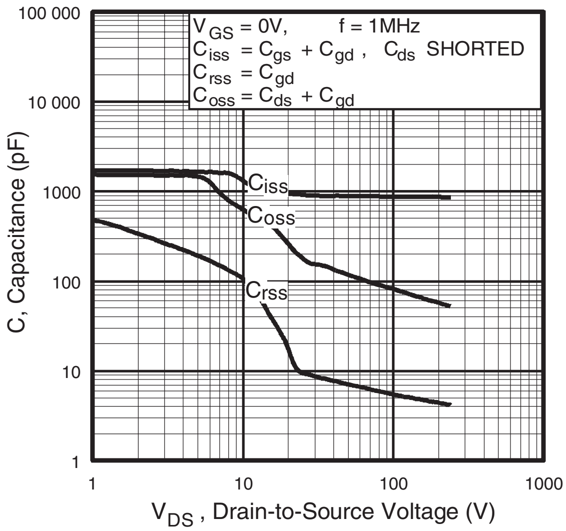


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

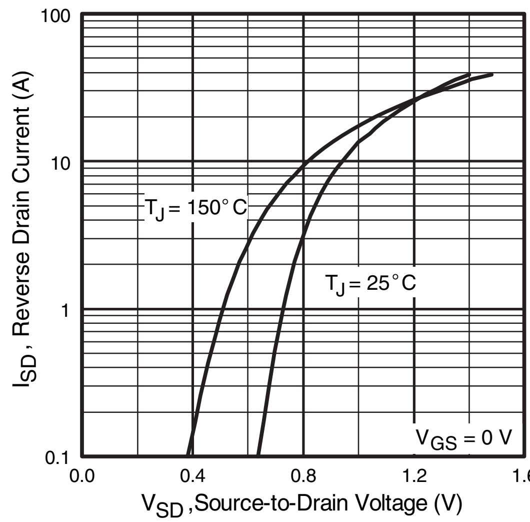


Fig. 7 - Typical Source-Drain Diode Forward Voltage

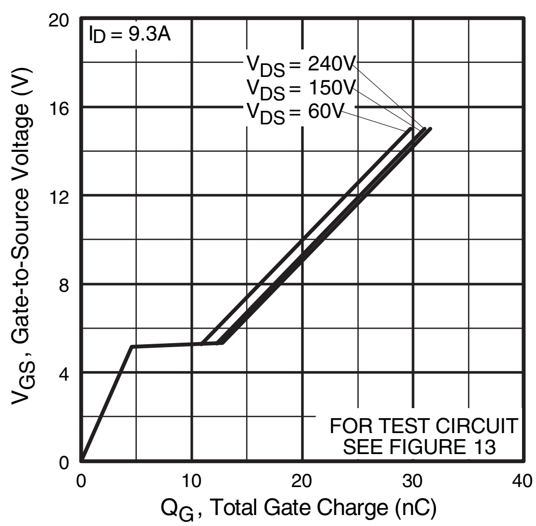


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

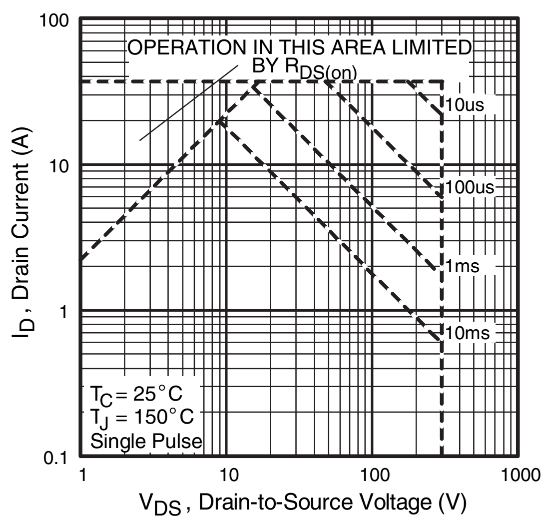


Fig. 8 - Maximum Safe Operating Area

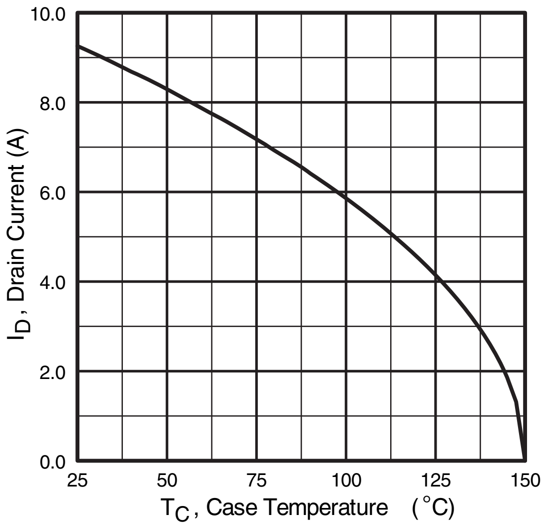


Fig. 9 - Maximum Drain Current vs. Case Temperature

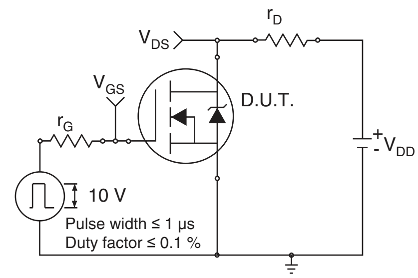


Fig. 10a - Switching Time Test Circuit

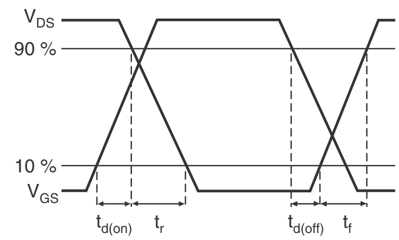


Fig. 10b - Switching Time Waveforms

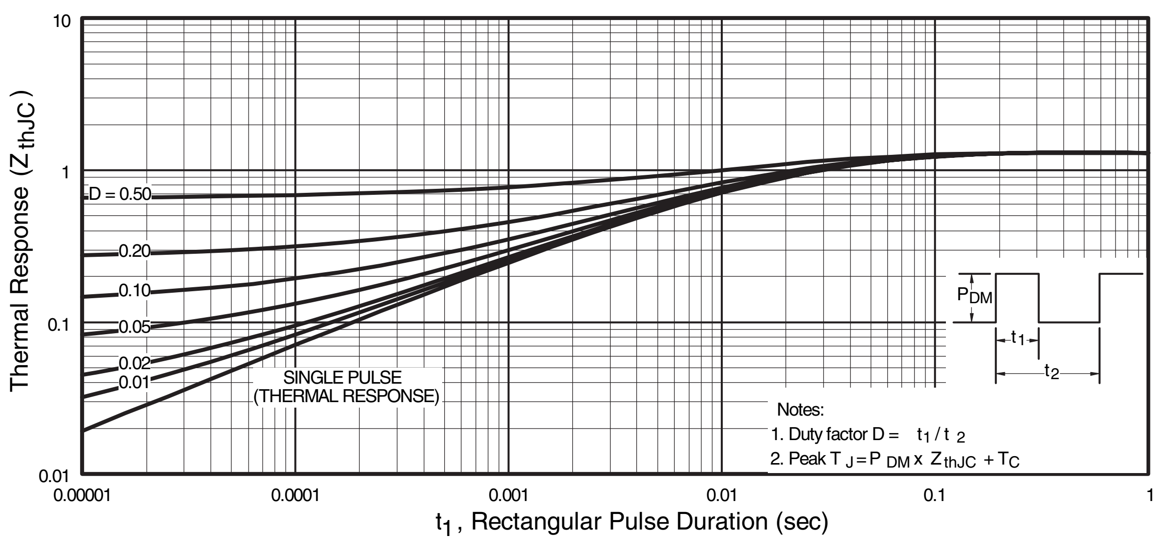


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

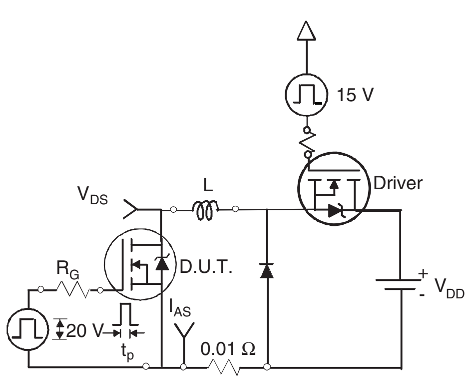


Fig. 12a - Unclamped Inductive Test Circuit

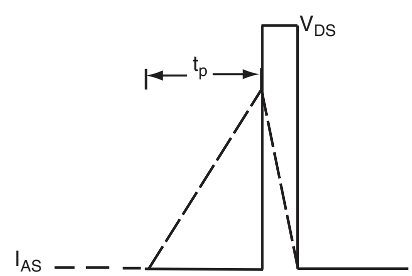


Fig. 12b - Unclamped Inductive Waveforms

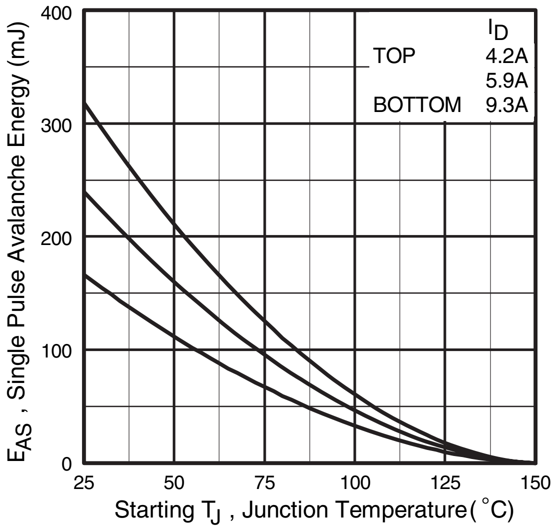


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

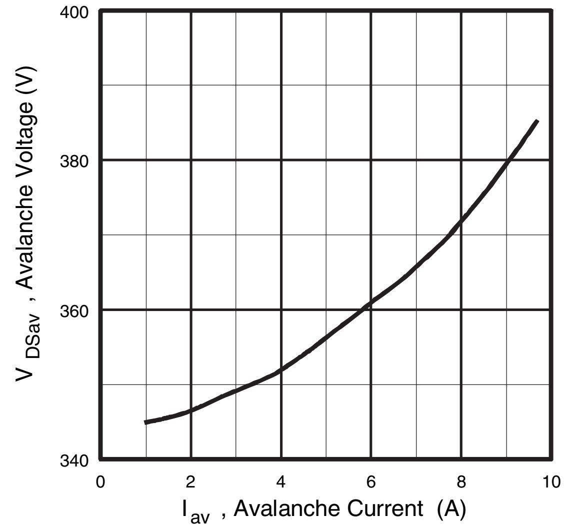


Fig. 12d - Typical Drain-to-Source Voltage vs. Avalanche Current

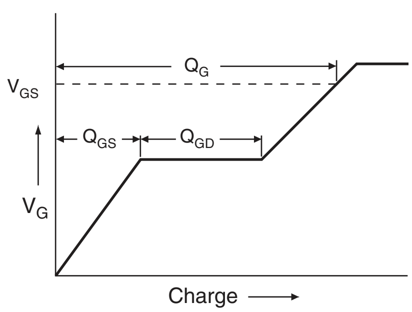


Fig. 13a - Basic Gate Charge Waveform

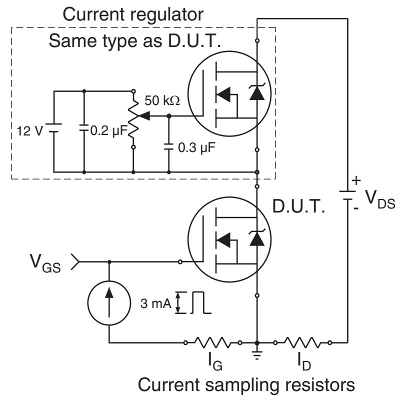
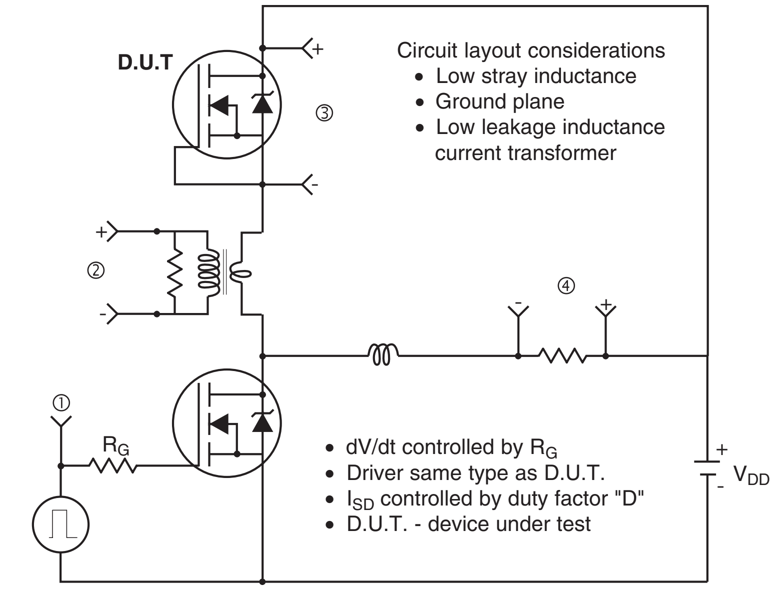
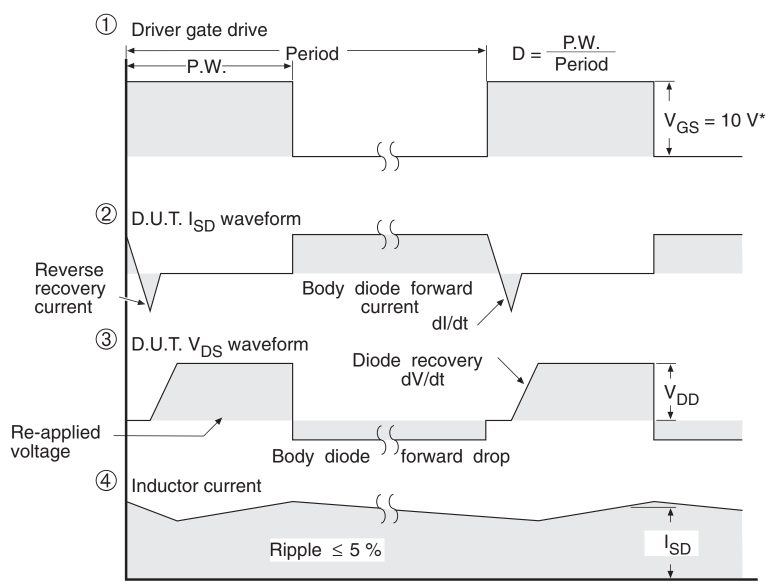


Fig. 13b - Gate Charge Test Circuit

Peak Diode Recovery dV/dt Test Circuit





* V_{GS} = 5 V for logic level devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see www.vishay.com/ppg?91102.

Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, “Vishay”), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay’s terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.