

# BUK95/9608-55A

TrenchMOS™ logic level FET

Rev. 03 — 6 May 2002

Product data

## 1. Description

N-channel enhancement mode field-effect power transistor in a plastic package using TrenchMOS™ technology, featuring very low on-state resistance.

Product availability:

BUK9508-55A in SOT78 (TO-220AB)

BUK9608-55A in SOT404 (D<sup>2</sup>-PAK).

## 2. Features

- TrenchMOS™ technology
- Q101 compliant
- 175 °C rated
- Logic level compatible.

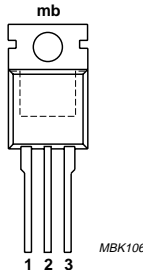
## 3. Applications

- Automotive and general purpose power switching:
  - ◆ 12 V and 24 V loads
  - ◆ Motors, lamps and solenoids.

## 4. Pinning information

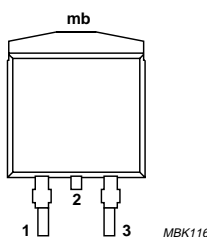
Table 1: Pinning - SOT78 and SOT404, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)		
2	drain (d) <span style="color: red;">[1]</span>		
3	source (s)		
mb	mounting base; connected to drain (d)		



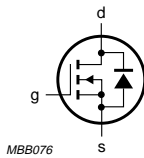
MBK106

**SOT78 (TO-220AB)**



MBK116

**SOT404 (D<sup>2</sup>-PAK)**



MBB076

[1] It is not possible to make connection to pin 2 of the SOT404 package.



**PHILIPS**

## 5. Quick reference data

**Table 2: Quick reference data**

Symbol	Parameter	Conditions	Typ	Max	Unit
$V_{DS}$	drain-source voltage (DC)		-	55	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V}$	-	125	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$	-	253	W
$T_j$	junction temperature		-	175	°C
$R_{DS(on)}$	drain-source on-state resistance	$T_j = 25\text{ °C}; V_{GS} = 5\text{ V}; I_D = 25\text{ A}$	6.8	8	mΩ
		$T_j = 25\text{ °C}; V_{GS} = 4.5\text{ V}; I_D = 25\text{ A}$	-	8.5	mΩ
		$T_j = 25\text{ °C}; V_{GS} = 10\text{ V}; I_D = 25\text{ A}$	6.4	7.5	mΩ

## 6. Limiting values

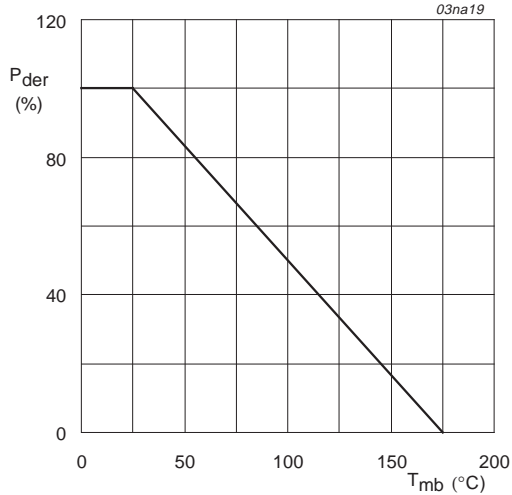
**Table 3: Limiting values**

In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)		-	55	V
$V_{DGR}$	drain-gate voltage (DC)	$R_{GS} = 20\text{ k}\Omega$	-	55	V
$V_{GS}$	gate-source voltage (DC)		-	±15	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2 and 3	[1] -	125	A
			[2] -	75	A
		$T_{mb} = 100\text{ °C}; V_{GS} = 5\text{ V};$ Figure 2	[2] -	75	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s};$ Figure 3	-	503	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C};$ Figure 1	-	253	W
$T_{stg}$	storage temperature		-55	+175	°C
$T_j$	junction temperature		-55	+175	°C
<b>Source-drain diode</b>					
$I_{DR}$	reverse drain current (DC)	$T_{mb} = 25\text{ °C}$	[1] -	125	A
			[2] -	75	A
$I_{DRM}$	peak reverse drain current	$T_{mb} = 25\text{ °C};$ pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	503	A
<b>Avalanche ruggedness</b>					
$E_{DS(AL)S}$	non-repetitive drain-source avalanche energy	unclamped inductive load; $I_D = 75\text{ A};$ $V_{DS} \leq 55\text{ V}; V_{GS} = 5\text{ V}; R_{GS} = 50\text{ }\Omega;$ starting $T_{mb} = 25\text{ °C}$	-	670	mJ

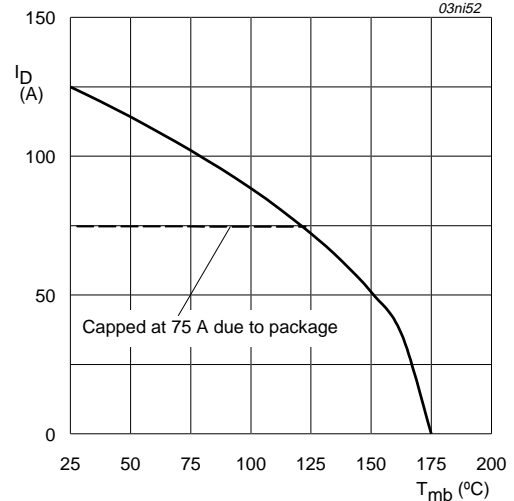
[1] Current is limited by power dissipation chip rating

[2] Continuous current is limited by package.



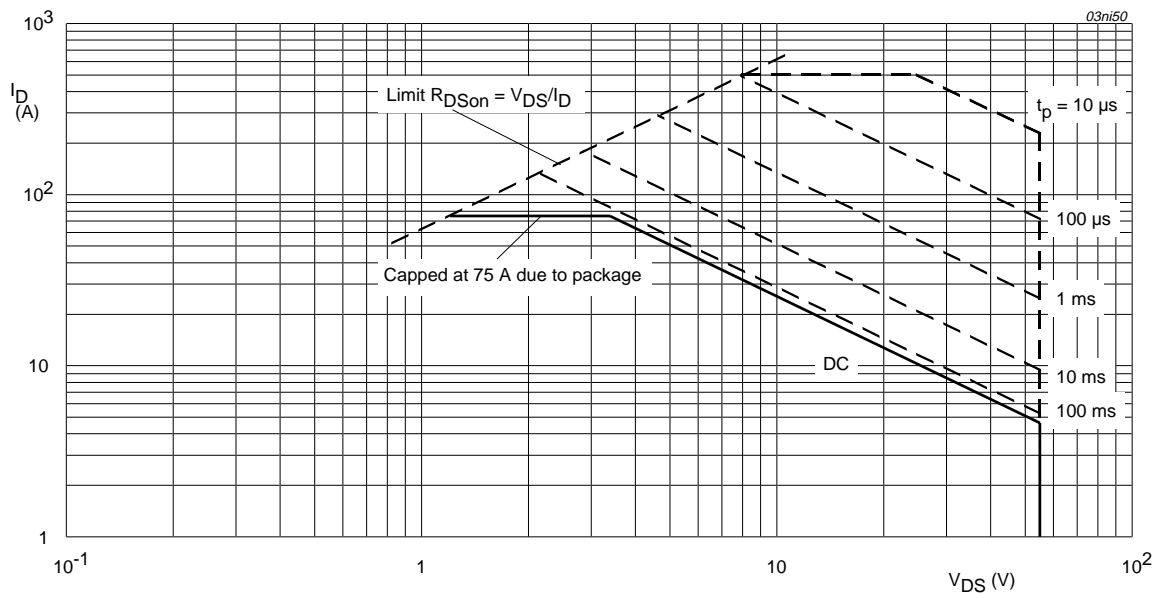
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

**Fig 1. Normalized total power dissipation as a function of mounting base temperature.**



$V_{GS} \geq 4.5 V$

**Fig 2. Continuous drain current as a function of mounting base temperature.**



$T_{mb} = 25^{\circ}C$ ;  $I_{DM}$  single pulse.

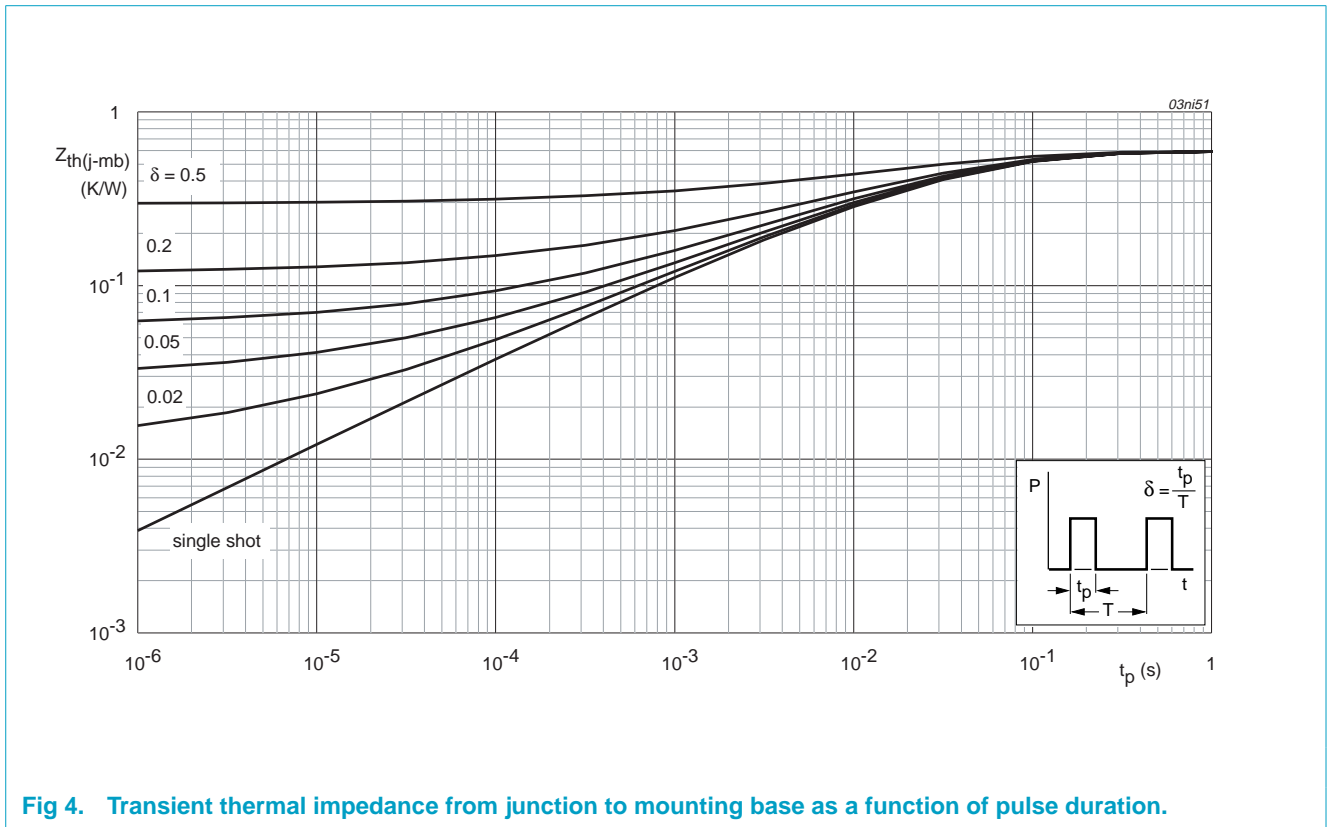
**Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.**

## 7. Thermal characteristics

**Table 4: Thermal characteristics**

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	0.59	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient					
	SOT78	vertical in still air	-	60	-	K/W
	SOT404	mounted on a printed circuit board; minimum footprint	-	50	-	K/W

### 7.1 Transient thermal impedance



**Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.**

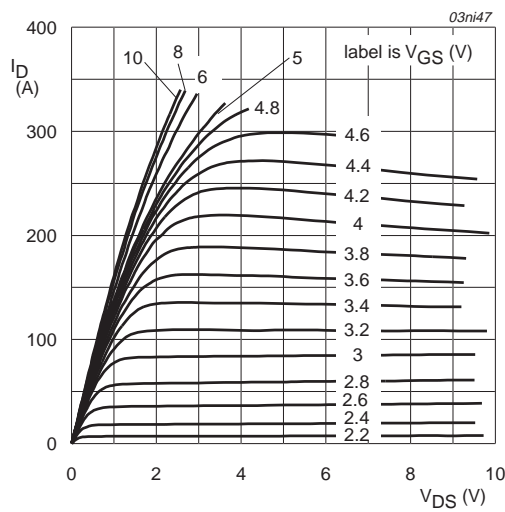
## 8. Characteristics

**Table 5: Characteristics**
*T<sub>j</sub> = 25 °C unless otherwise specified.*

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
V <sub>(BR)DSS</sub>	drain-source breakdown voltage	I <sub>D</sub> = 0.25 mA; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	55	-	-	V
		T <sub>j</sub> = -55 °C	50	-	-	V
V <sub>GS(th)</sub>	gate-source threshold voltage	I <sub>D</sub> = 1 mA; V <sub>DS</sub> = V <sub>GS</sub> ; Figure 9				
		T <sub>j</sub> = 25 °C	1	1.5	2	V
		T <sub>j</sub> = 175 °C	0.5	-	-	V
		T <sub>j</sub> = -55 °C	-	-	2.3	V
I <sub>DSS</sub>	drain-source leakage current	V <sub>DS</sub> = 55 V; V <sub>GS</sub> = 0 V				
		T <sub>j</sub> = 25 °C	-	0.05	10	μA
		T <sub>j</sub> = 175 °C	-	-	500	μA
I <sub>GSS</sub>	gate-source leakage current	V <sub>GS</sub> = ±10 V; V <sub>DS</sub> = 0 V	-	2	100	nA
R <sub>DS(on)</sub>	drain-source on-state resistance	V <sub>GS</sub> = 5 V; I <sub>D</sub> = 25 A; Figure 7 and 8				
		T <sub>j</sub> = 25 °C	-	6.8	8	mΩ
		T <sub>j</sub> = 175 °C	-	-	16	mΩ
		V <sub>GS</sub> = 4.5 V; I <sub>D</sub> = 25 A	-	-	8.5	mΩ
		V <sub>GS</sub> = 10 V; I <sub>D</sub> = 25 A	-	6.4	7.5	mΩ
<b>Dynamic characteristics</b>						
Q <sub>g(tot)</sub>	total gate charge	V <sub>GS</sub> = 5 V; V <sub>DD</sub> = 44 V; I <sub>D</sub> = 25 A; Figure 14	-	92	-	nC
Q <sub>gs</sub>	gate-to-source charge		-	11	-	nC
Q <sub>gd</sub>	gate-to-drain (Miller) charge		-	43	-	nC
C <sub>iss</sub>	input capacitance	V <sub>GS</sub> = 0 V; V <sub>DS</sub> = 25 V; f = 1 MHz; Figure 12	-	4551	6021	pF
C <sub>oss</sub>	output capacitance		-	760	900	pF
C <sub>rss</sub>	reverse transfer capacitance		-	500	687	pF
t <sub>d(on)</sub>	turn-on delay time	V <sub>DD</sub> = 30 V; R <sub>L</sub> = 1.2 Ω; V <sub>GS</sub> = 5 V; R <sub>G</sub> = 10 Ω	-	40	-	ns
t <sub>r</sub>	rise time		-	175	-	ns
t <sub>d(off)</sub>	turn-off delay time		-	280	-	ns
t <sub>f</sub>	fall time		-	167	-	ns
L <sub>d</sub>	internal drain inductance	from drain lead 6 mm from package to centre of die	-	4.5	-	nH
		from contact screw on mounting base to centre of die SOT78	-	3.5	-	nH
		from upper edge of drain mounting base to centre of die SOT404	-	2.5	-	nH
L <sub>s</sub>	internal source inductance	from source lead to source bond pad	-	7.5	-	nH

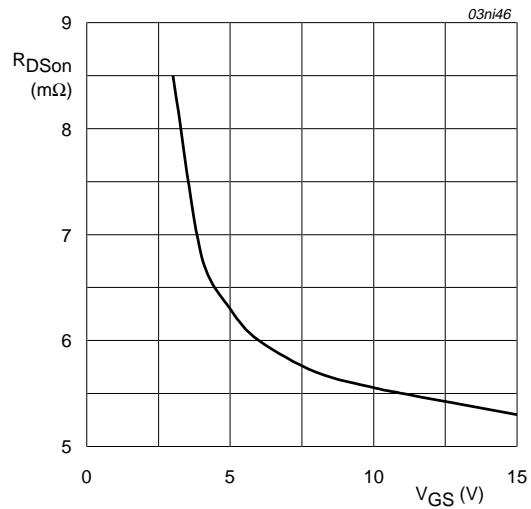
**Table 5: Characteristics...continued**  
 $T_j = 25\text{ }^\circ\text{C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 25\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; Figure 15	-	0.85	1.2	V
$t_{rr}$	reverse recovery time	$I_S = 75\text{ A}$ ; $dI_S/dt = -100\text{ A}/\mu\text{s}$	-	70	-	ns
$Q_r$	recovered charge	$V_{GS} = -10\text{ V}$ ; $V_{DS} = 25\text{ V}$	-	170	-	nC



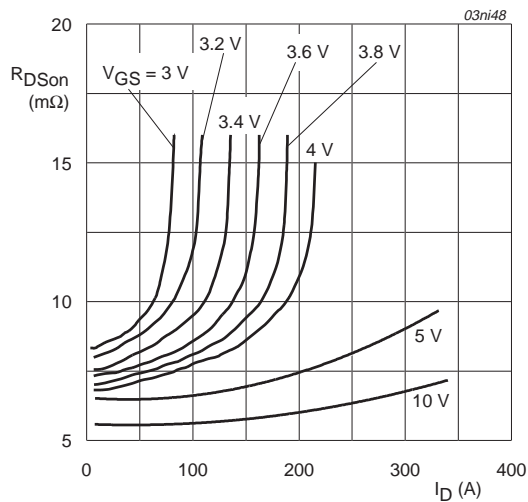
$T_j = 25\text{ }^\circ\text{C}$ ;  $t_p = 300\text{ }\mu\text{s}$

**Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.**



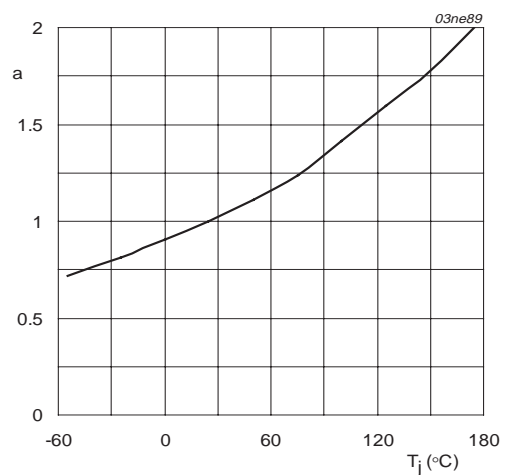
$T_j = 25\text{ }^\circ\text{C}$ ;  $I_D = 25\text{ A}$

**Fig 6. Drain-source on-state resistance as a function of gate-source voltage; typical values.**



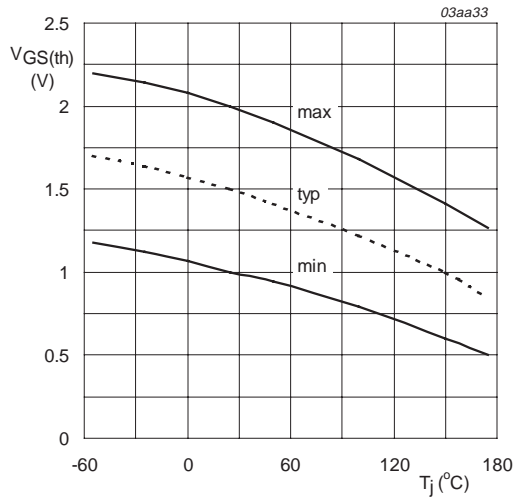
$T_j = 25\text{ }^\circ\text{C}$

**Fig 7. Drain-source on-state resistance as a function of drain current; typical values.**



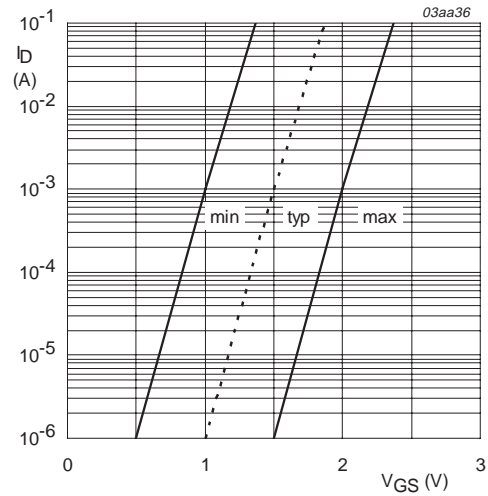
$a = R_{DSon}/R_{DSon}(25\text{ }^\circ\text{C})$

**Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.**



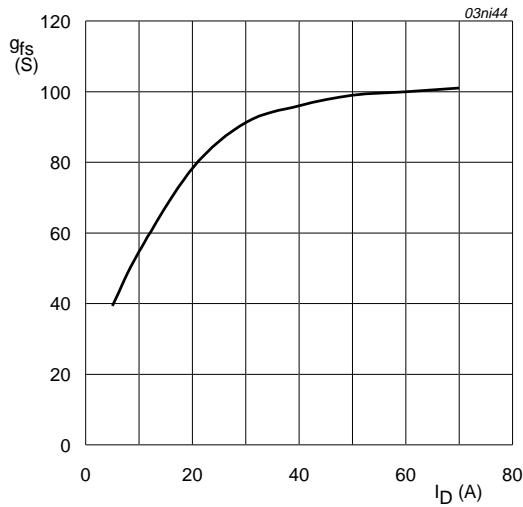
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

**Fig 9. Gate-source threshold voltage as a function of junction temperature.**



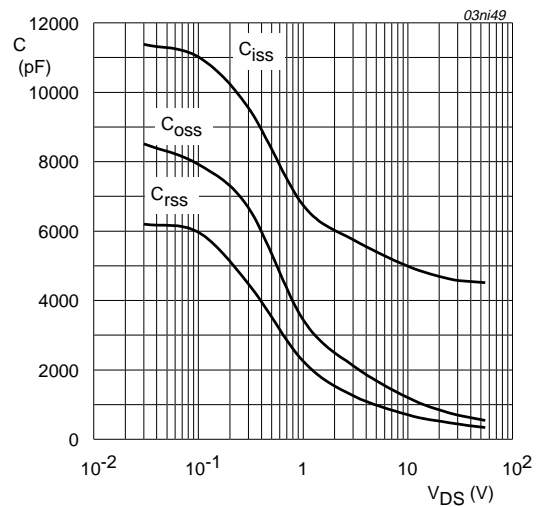
$T_j = 25 \text{ °C}; V_{DS} = V_{GS}$

**Fig 10. Sub-threshold drain current as a function of gate-source voltage.**



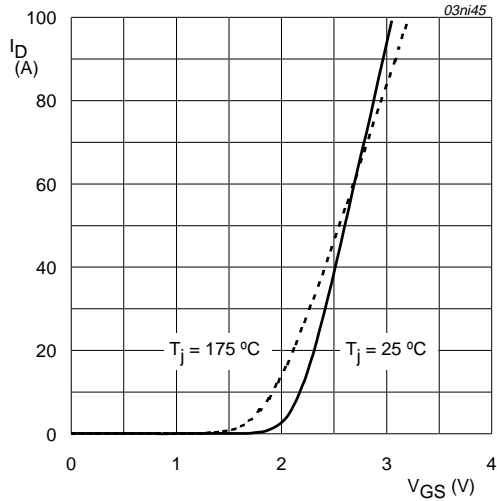
$T_j = 25 \text{ °C}; V_{DS} = 25 \text{ V}$

**Fig 11. Forward transconductance as a function of drain current; typical values.**



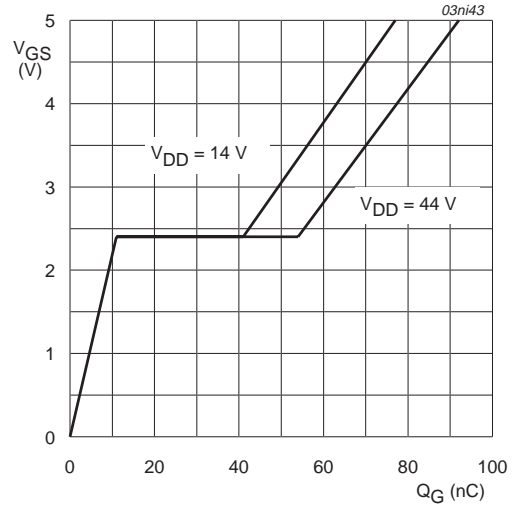
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

**Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.**



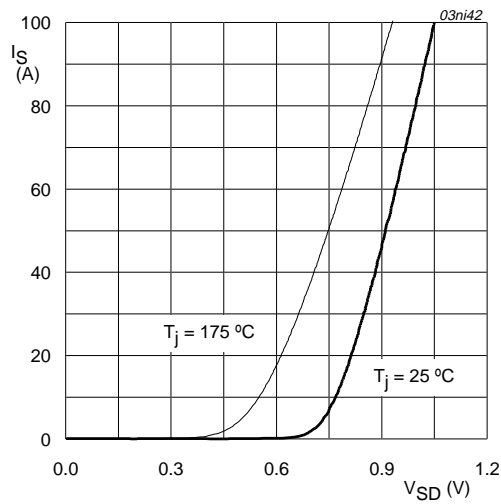
$V_{DS} = 25 \text{ V}$

**Fig 13. Transfer characteristics: drain current as a function of gate-source voltage; typical values.**



$T_j = 25 \text{ }^\circ\text{C}; I_D = 25 \text{ A}$

**Fig 14. Gate-source voltage as a function of turn-on gate charge; typical values.**



$V_{GS} = 0 \text{ V}$

**Fig 15. Reverse diode current as a function of reverse diode voltage; typical values.**

**9. Package outline**

Plastic single-ended package; heatsink mounted; 1 mounting hole; 3-lead TO-220AB

SOT78

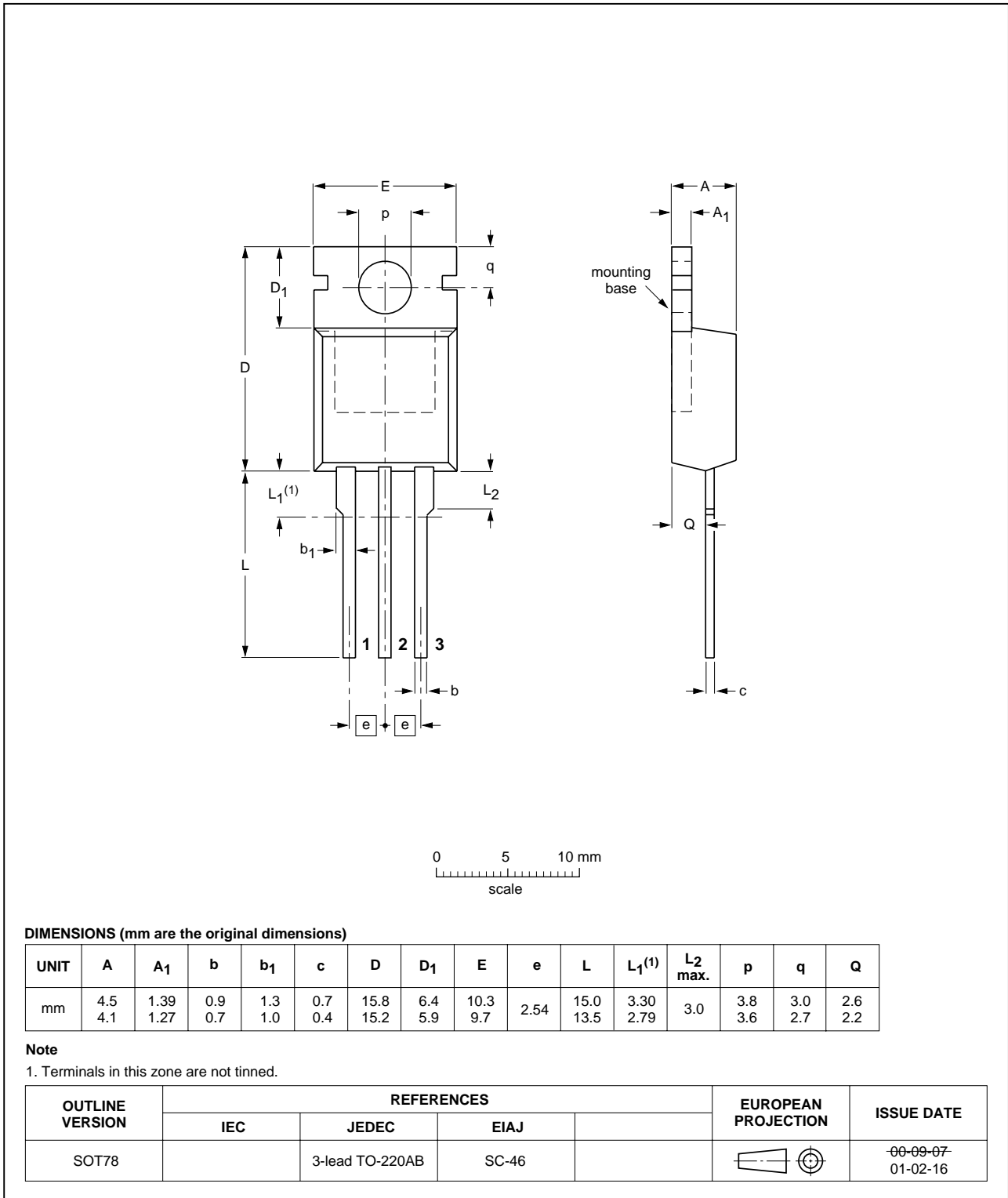


Fig 16. SOT78 (TO-220AB).

Plastic single-ended surface mounted package (Philips version of D<sup>2</sup>-PAK); 3 leads  
(one lead cropped)

SOT404

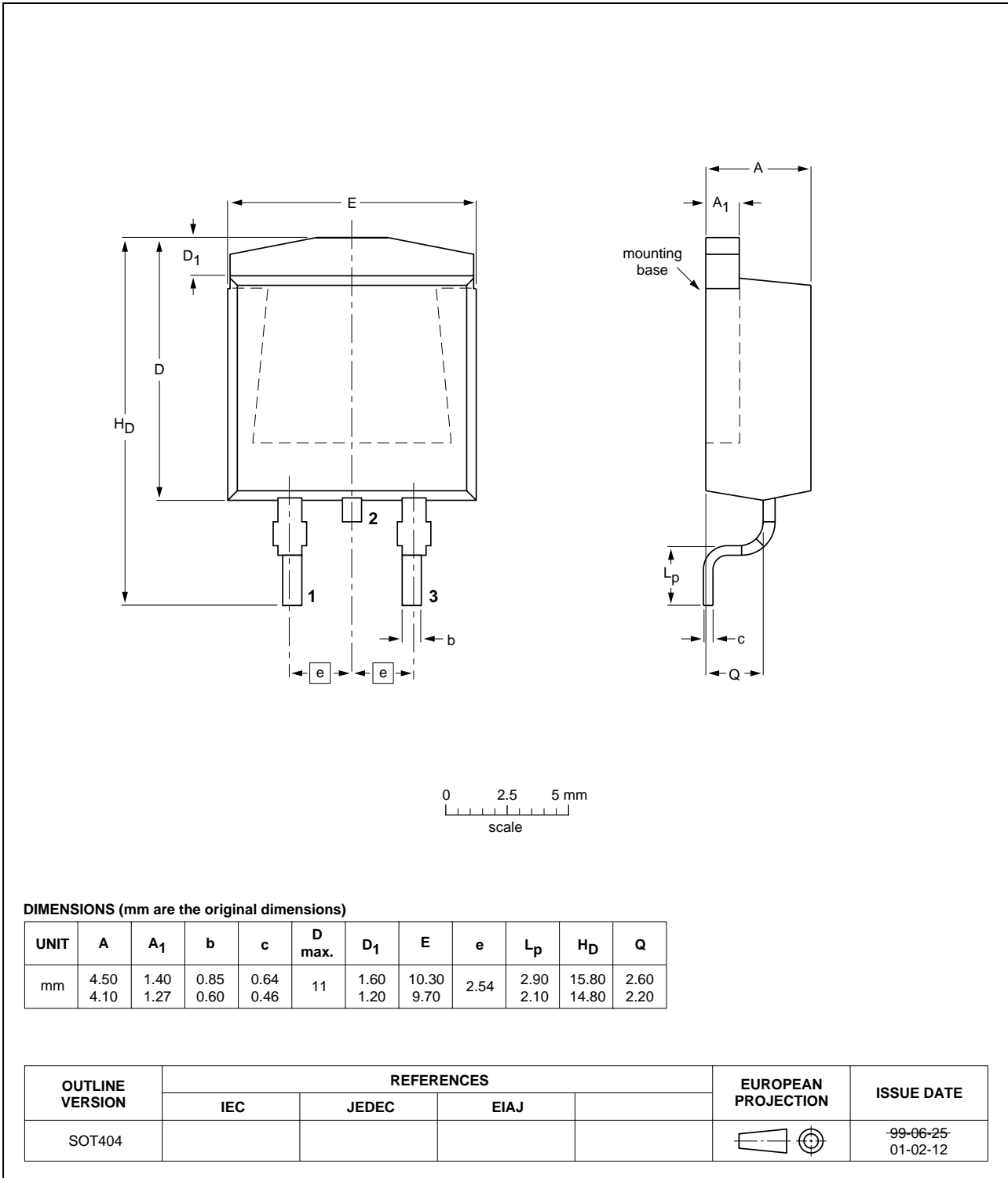
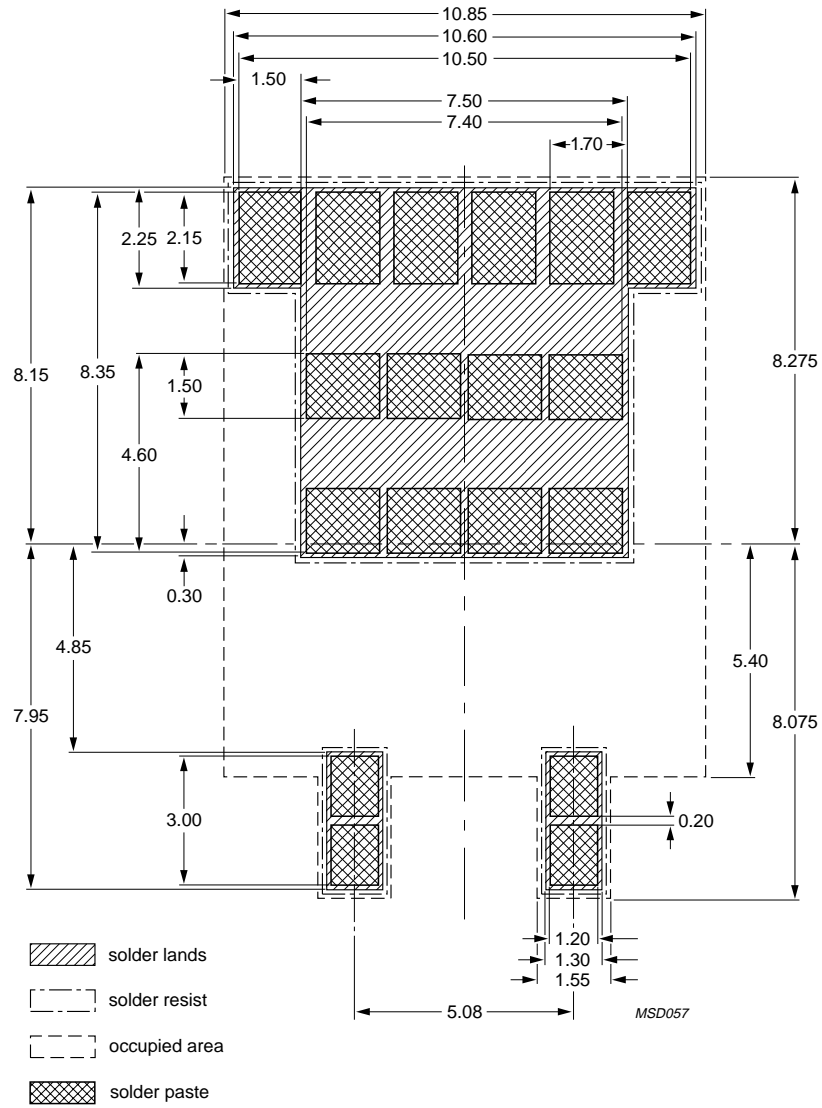


Fig 17. SOT404 (D<sup>2</sup>-PAK).

**10. Soldering**



Dimensions in mm.

**Fig 18. Reflow soldering footprint for SOT404.**

## 11. Revision history

Table 6: Revision history

Rev	Date	CPCN	Description
03	20020506	-	<p><b>Product data (9397 750 09573); supersedes Product data of BUK9508_9608-55A_2 of 4 of September 2000.</b></p> <p>Modifications:</p> <ul style="list-style-type: none"><li>• The format of this specification has been redesigned to comply with Philips Semiconductors' new presentation and information standard.</li><li>• Thermal resistance figure lowered (j-mb) <a href="#">Section 7</a>. This has a knock on effect on the devices current and power handling capabilities (See <a href="#">Section 5</a> and <a href="#">Section 6</a>).</li><li>• Maximum gate-source voltage increased from <math>\pm 10</math> to <math>\pm 15</math> V (<a href="#">Section 6</a>).</li><li>• Switching speeds re-measured in dynamic characteristics <a href="#">Section 8</a>.</li></ul>

## 12. Data sheet status

Data sheet status <sup>[1]</sup>	Product status <sup>[2]</sup>	Definition
Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
Preliminary data	Qualification	This data sheet contains data from the preliminary specification. Supplementary data will be published at a later date. Philips Semiconductors reserves the right to change the specification without notice, in order to improve the design and supply the best possible product.
Product data	Production	This data sheet contains data from the product specification. Philips Semiconductors reserves the right to make changes at any time in order to improve the design, manufacturing and supply. Changes will be communicated according to the Customer Product/Process Change Notification (CPCN) procedure SNW-SQ-650A.

[1] Please consult the most recently issued data sheet before initiating or completing a design.

[2] The product status of the device(s) described in this data sheet may have changed since this data sheet was published. The latest information is available on the Internet at URL <http://www.semiconductors.philips.com>.

## 13. Definitions

**Short-form specification** — The data in a short-form specification is extracted from a full data sheet with the same type number and title. For detailed information see the relevant data sheet or data handbook.

**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

**Application information** — Applications that are described herein for any of these products are for illustrative purposes only. Philips Semiconductors make no representation or warranty that such applications will be suitable for the specified use without further testing or modification.

## 14. Disclaimers

**Life support** — These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Philips Semiconductors customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Philips Semiconductors for any damages resulting from such application.

**Right to make changes** — Philips Semiconductors reserves the right to make changes, without notice, in the products, including circuits, standard cells, and/or software, described or contained herein in order to improve design and/or performance. Philips Semiconductors assumes no responsibility or liability for the use of any of these products, conveys no licence or title under any patent, copyright, or mask work right to these products, and makes no representations or warranties that these products are free from patent, copyright, or mask work right infringement, unless otherwise specified.

## 15. Trademarks

**TrenchMOS** — is a trademark of Koninklijke Philips Electronics N.V.

## Contact information

For additional information, please visit <http://www.semiconductors.philips.com>.

For sales office addresses, send e-mail to: [sales.addresses@www.semiconductors.philips.com](mailto:sales.addresses@www.semiconductors.philips.com).

Fax: +31 40 27 24825

## Contents

1	Description . . . . .	1
2	Features . . . . .	1
3	Applications . . . . .	1
4	Pinning information . . . . .	1
5	Quick reference data . . . . .	2
6	Limiting values . . . . .	2
7	Thermal characteristics . . . . .	4
7.1	Transient thermal impedance . . . . .	4
8	Characteristics . . . . .	5
9	Package outline . . . . .	9
10	Soldering . . . . .	11
11	Revision history . . . . .	12
12	Data sheet status . . . . .	13
13	Definitions . . . . .	13
14	Disclaimers . . . . .	13
15	Trademarks . . . . .	13

© Koninklijke Philips Electronics N.V. 2002.  
Printed in The Netherlands

All rights are reserved. Reproduction in whole or in part is prohibited without the prior written consent of the copyright owner.

The information presented in this document does not form part of any quotation or contract, is believed to be accurate and reliable and may be changed without notice. No liability will be accepted by the publisher for any consequence of its use. Publication thereof does not convey nor imply any license under patent- or other industrial or intellectual property rights.

Date of release: 6 May 2002

Document order number: 9397 750 09573





# PHILIPS

*Let's make things better.*

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View BUK9508-55A,127 on WIN SOURCE](#)
-  [NXP / Nexperia Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management