THE DATASHEET OF

NTB75N06LT4G

NTP75N06L, NTB75N06L

Power MOSFET 75 Amps, 60 Volts, Logic Level

N−Channel TO−220 and D²PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

Features

- Pb−Free Packages are Available

Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

MAXIMUM RATINGS (T_J = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain−to−Source Voltage	V_{DSS}	60	Vdc
Drain−to−Gate Voltage (R_{GS} = 10 MΩ)	V_{DGR}	60	Vdc
Gate−to−Source Voltage − Continuous − Non−Repetitive ($t_p \le 10$ ms)	 V_{GS} V_{GS}	 ±20 ±15	Vdc
Drain Current − Continuous @ T_A = 25°C − Continuous @ T_A = 100°C − Single Pulse ($t_p \le 10$ μs)	 I_D I_D I_{DM}	 75 50 225	 Adc Apk
Total Power Dissipation @ T_A = 25°C Derate above 25°C Total Power Dissipation @ T_A = 25°C (Note 1)	P_D	214 1.4 2.4	W W/°C W
Operating and Storage Temperature Range	T_J, T_{stg}	−55 to +175	°C
Single Pulse Drain−to−Source Avalanche Energy − Starting T_J = 25°C (V_{DD} = 50 Vdc, V_{GS} = 5.0 Vdc, L = 0.3 mH $I_{L(pk)}$ = 75 A, V_{DS} = 60 Vdc)	E_{AS}	844	mJ
Thermal Resistance − Junction−to−Case − Junction−to−Ambient (Note 1)	 $R_{\theta JC}$ $R_{\theta JA}$	 0.7 62.5	°C/W
Maximum Lead Temperature for Soldering Purposes, 1/8″ from case for 10 seconds	T_L	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in²).

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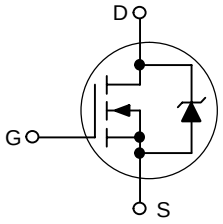
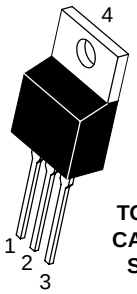
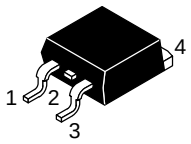
75 AMPERES, 60 VOLTS
$R_{DS(on)}$ = 11 mΩ

N−Channel



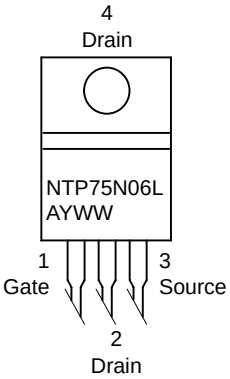


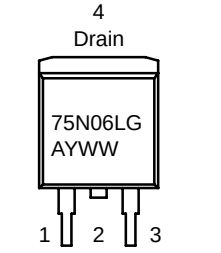
TO−220AB
CASE 221A
STYLE 5



D²PAK
CASE 418B
STYLE 2

MARKING DIAGRAMS & PIN ASSIGNMENTS





A	= Assembly Location
Y	= Year
WW	= Work Week
G	= Pb−Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

ELECTRICAL CHARACTERISTICS (T_J = 25°C unless otherwise noted)

Characteristic		Symbol	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain−to−Source Breakdown Voltage (Note 2) (V_{GS} = 0 Vdc, I_D = 250 μAdc) Temperature Coefficient (Positive)		$V_{(BR)DSS}$	 60 −	 72 74	 − −	Vdc mV/°C
Zero Gate Voltage Drain Current (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc) (V_{DS} = 60 Vdc, V_{GS} = 0 Vdc, T_J = 150°C)		I_{DSS}	 − −	 − −	 10 100	μAdc
Gate−Body Leakage Current (V_{GS} = ±15 Vdc, V_{DS} = 0 Vdc)		I_{GSS}	−	−	±100	nAdc
ON CHARACTERISTICS (Note 2)						
Gate Threshold Voltage (Note 2) (V_{DS} = V_{GS}, I_D = 250 μAdc) Threshold Temperature Coefficient (Negative)		$V_{GS(th)}$	 1.0 −	 1.58 6.0	 2.0 −	Vdc mV/°C
Static Drain−to−Source On−Resistance (Note 2) (V_{GS} = 5.0 Vdc, I_D = 37.5 Adc)		$R_{DS(on)}$	 −	 9.0	 11	mΩ
Static Drain−to−Source On−Voltage (Note 2) (V_{GS} = 5.0 Vdc, I_D = 75 Adc) (V_{GS} = 5.0 Vdc, I_D = 37.5 Adc, T_J = 150°C)		$V_{DS(on)}$	 − −	 0.75 0.61	 0.99 −	Vdc
Forward Transconductance (Note 2) (V_{DS} = 15 Vdc, I_D = 37.5 Adc)		g_{FS}	−	55	−	mhos
DYNAMIC CHARACTERISTICS						
Input Capacitance	(V_{DS} = 25 Vdc, V_{GS} = 0 Vdc, f = 1.0 MHz)	C_{iss}	−	3122	4370	pF
Output Capacitance		C_{oss}	−	1029	1440	
Transfer Capacitance		C_{rss}	−	276	390	
SWITCHING CHARACTERISTICS (Note 3)						
Turn−On Delay Time	(V_{DD} = 30 Vdc, I_D = 75 Adc, V_{GS} = 5.0 Vdc, R_G = 9.1 Ω) (Note 2)	$t_{d(on)}$	−	22	32	ns
Rise Time		t_r	−	265	370	
Turn−Off Delay Time		$t_{d(off)}$	−	113	160	
Fall Time		t_f	−	170	240	
Gate Charge	(V_{DS} = 48 Vdc, I_D = 75 Adc, V_{GS} = 5.0 Vdc) (Note 2)	Q_T	−	66	92	nC
		Q_1	−	9.0	−	
		Q_2	−	47	−	
SOURCE−DRAIN DIODE CHARACTERISTICS						
Forward On−Voltage	(I_S = 75 Adc, V_{GS} = 0 Vdc) (Note 2) (I_S = 75 Adc, V_{GS} = 0 Vdc, T_J = 150°C)	V_{SD}	 −	 1.0 0.9	 1.15 −	Vdc
Reverse Recovery Time	(I_S = 75 Adc, V_{GS} = 0 Vdc, dI_S/dt = 100 A/μs) (Note 2)	t_{rr}	−	70	−	ns
		t_a	−	43	−	
		t_b	−	27	−	
Reverse Recovery Stored Charge		Q_{RR}	−	0.16	−	μC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

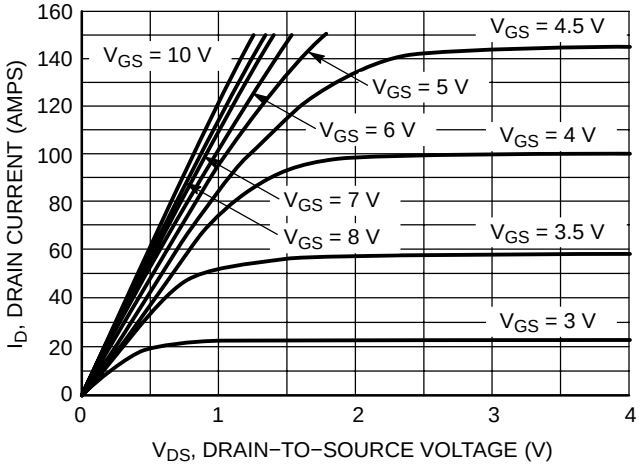


Figure 1. On−Region Characteristics

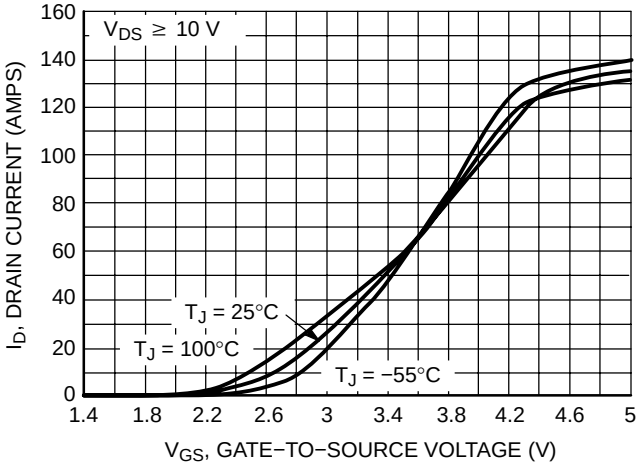


Figure 2. Transfer Characteristics

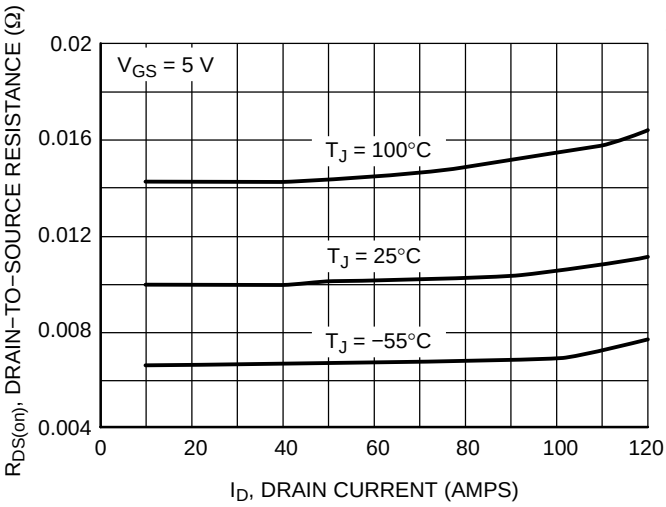


Figure 3. On−Resistance vs. Gate−to−Source Voltage

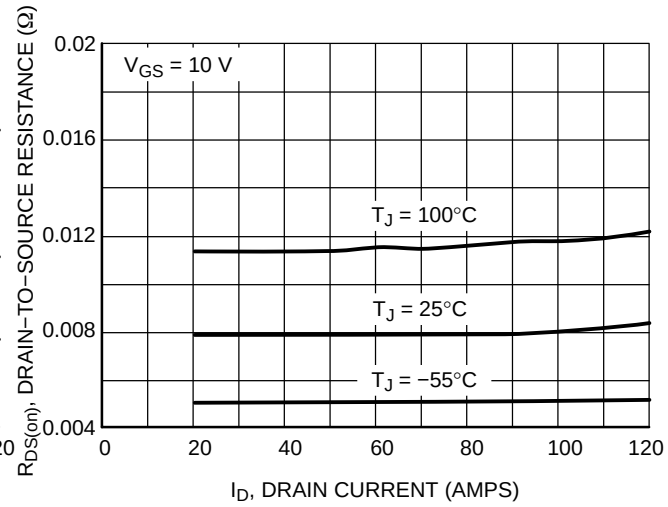


Figure 4. On−Resistance vs. Drain Current and Gate Voltage

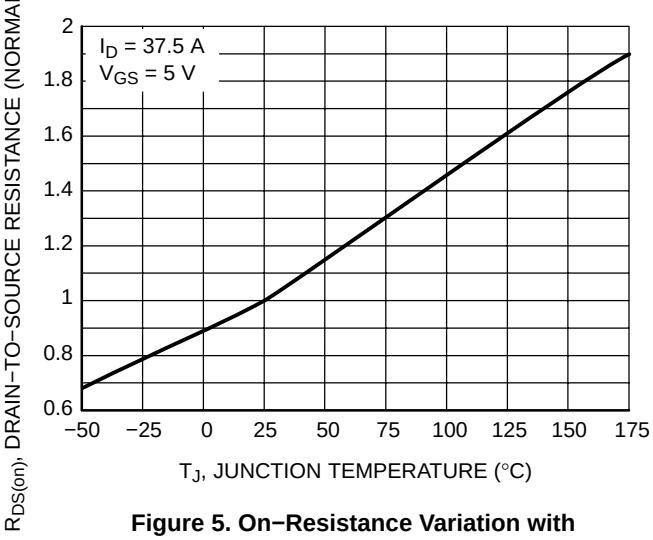


Figure 5. On−Resistance Variation with Temperature

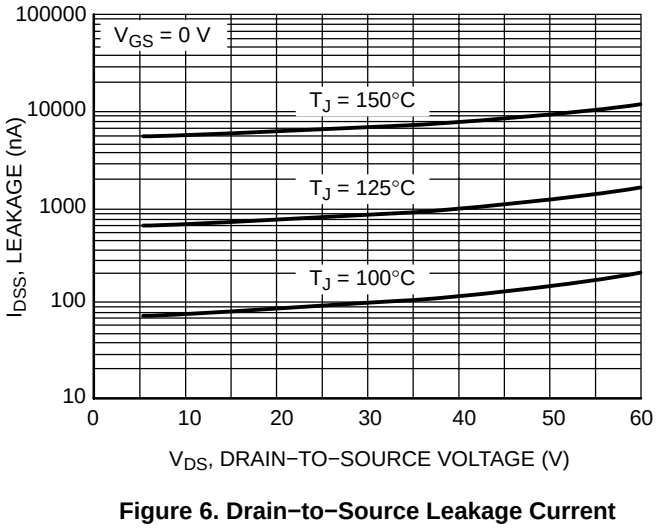


Figure 6. Drain−to−Source Leakage Current vs. Voltage

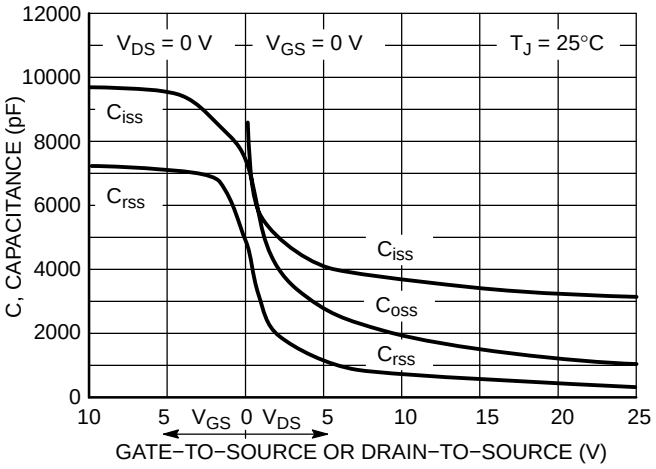


Figure 7. Capacitance Variation

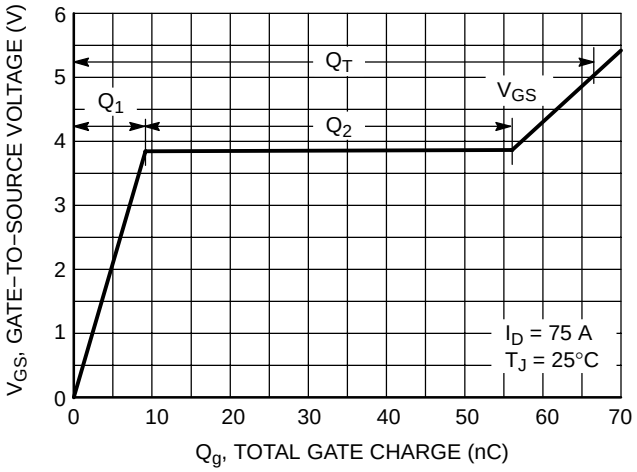


Figure 8. Gate−to−Source and Drain−to−Source Voltage vs. Total Charge

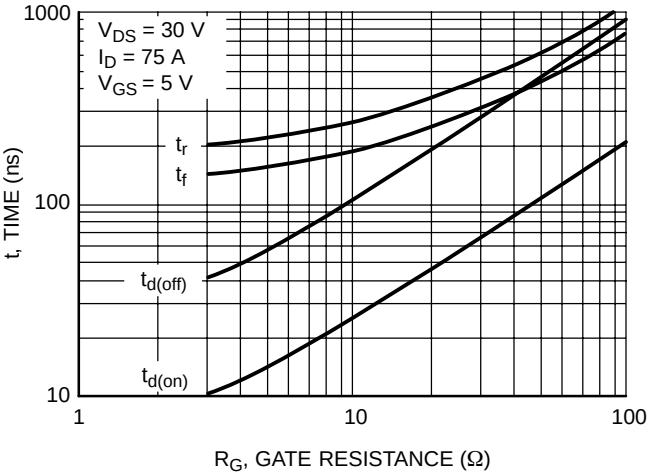


Figure 9. Resistive Switching Time Variations vs. Gate Resistance

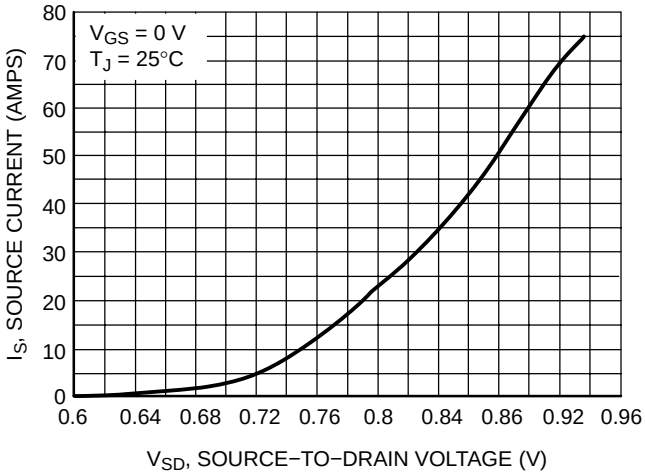


Figure 10. Diode Forward Voltage vs. Current

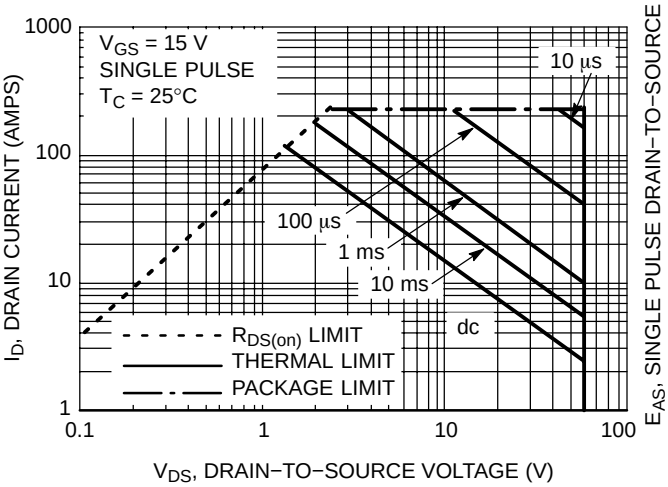


Figure 11. Maximum Rated Forward Biased Safe Operating Area

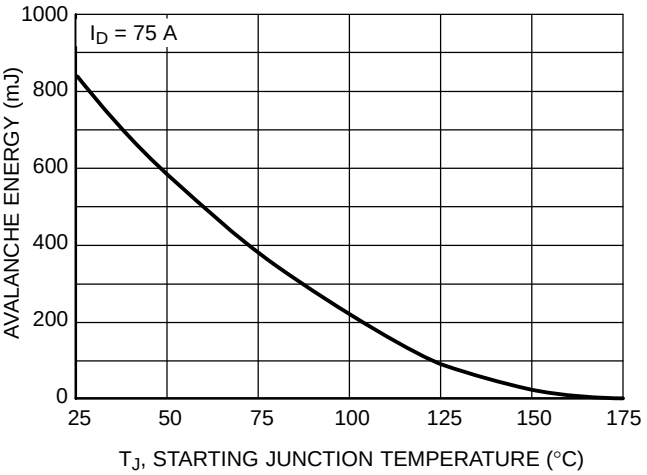


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

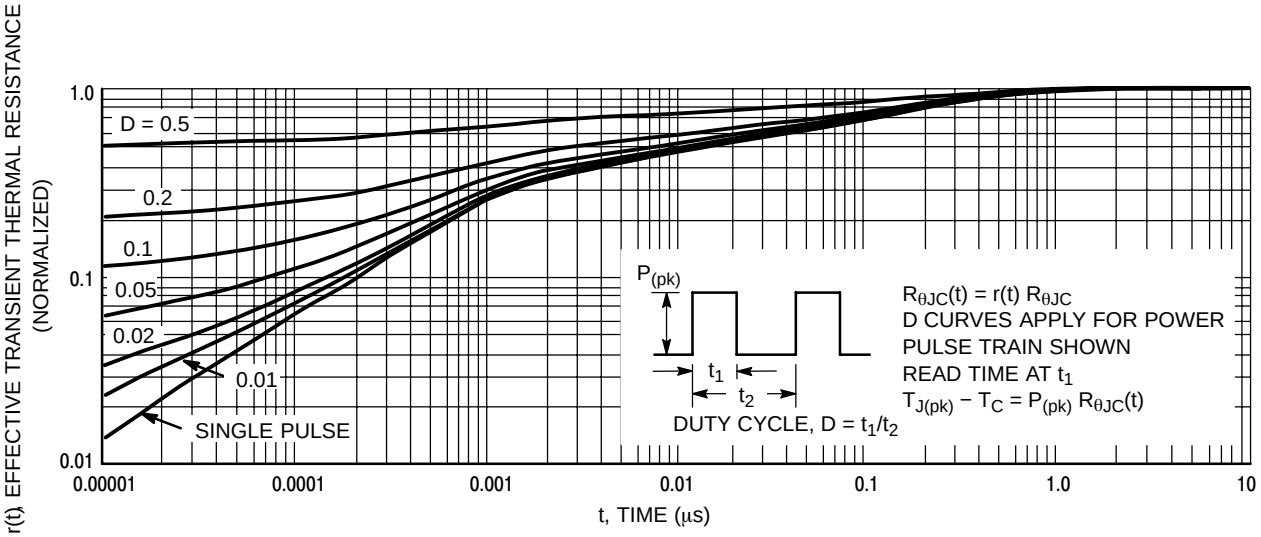


Figure 13. Thermal Response

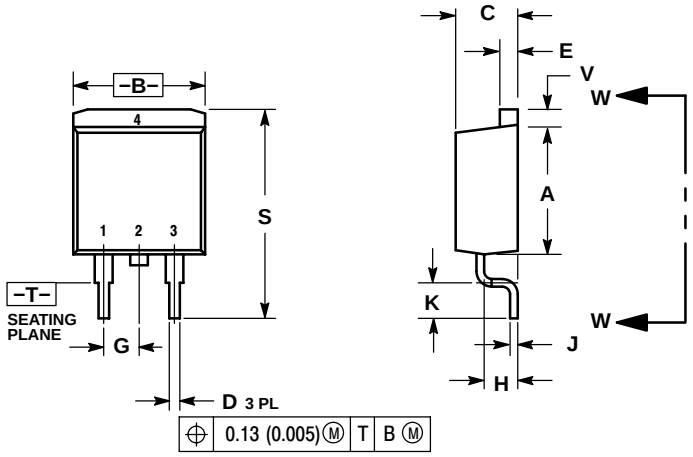
ORDERING INFORMATION

Device	Package	Shipping†
NTP75N06L	TO−220AB	50 Units / Rail
NTB75N06L	D^2PAK	50 Units / Rail
NTB75N06LG	D^2PAK (Pb−Free)	50 Units / Rail
NTB75N06LT4	D^2PAK	800 Units / Tape & Reel
NTB75N06LT4G	D^2PAK (Pb−Free)	800 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

PACKAGE DIMENSIONS

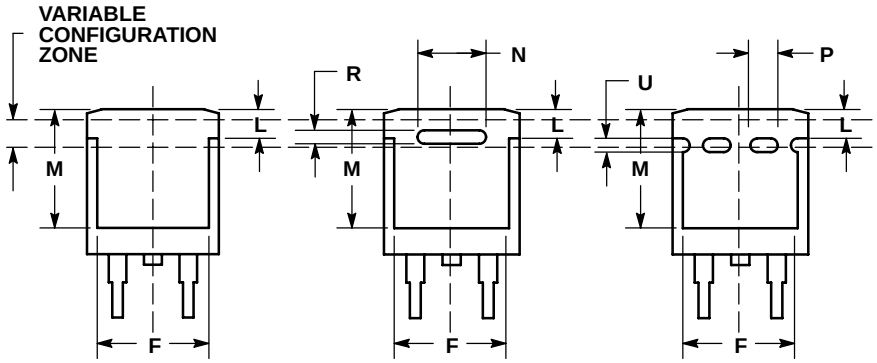
D²PAK
CASE 418B−04
ISSUE J



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B−01 THRU 418B−03 OBSOLETE, NEW STANDARD 418B−04.

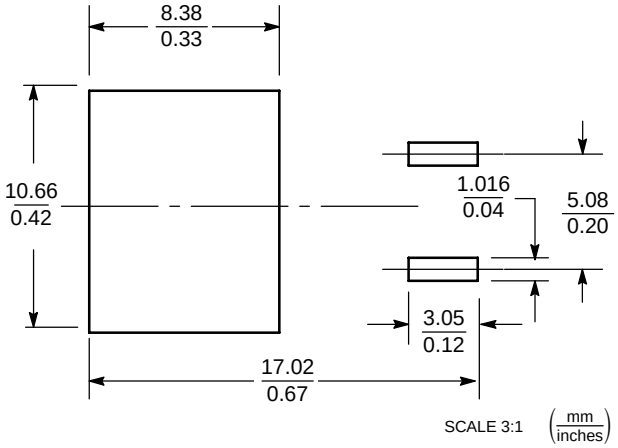
	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40

STYLE 2:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN



VIEW W−W 1 | VIEW W−W 2 | VIEW W−W 3

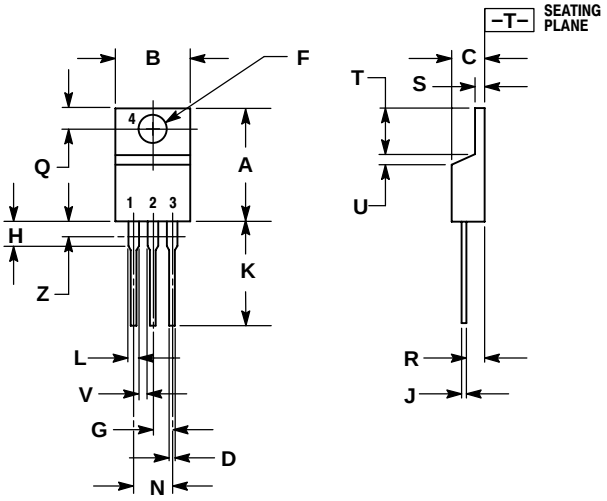
SOLDERING FOOTPRINT*



*For additional information on our Pb−Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

PACKAGE DIMENSIONS

TO−220
CASE 221A−09
ISSUE AA



NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

	INCHES		MILLIMETERS	
DIM	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:
PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

PUBLICATION ORDERING INFORMATION

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