



**THE DATASHEET OF  
NTB75N06LT4G**



# NTP75N06L, NTB75N06L

## Power MOSFET 75 Amps, 60 Volts, Logic Level

### N-Channel TO-220 and D<sup>2</sup>PAK

Designed for low voltage, high speed switching applications in power supplies, converters and power motor controls and bridge circuits.

#### Features

- Pb-Free Packages are Available

#### Typical Applications

- Power Supplies
- Converters
- Power Motor Controls
- Bridge Circuits

#### MAXIMUM RATINGS (T<sub>J</sub> = 25°C unless otherwise noted)

Rating	Symbol	Value	Unit
Drain-to-Source Voltage	V <sub>DSS</sub>	60	Vdc
Drain-to-Gate Voltage (R <sub>GS</sub> = 10 MΩ)	V <sub>DGR</sub>	60	Vdc
Gate-to-Source Voltage	V <sub>GS</sub>	±20	Vdc
– Continuous	V <sub>GS</sub>	±15	
– Non-Repetitive (t <sub>p</sub> ≤ 10 ms)			
Drain Current	I <sub>D</sub>	75	A dc
– Continuous @ T <sub>A</sub> = 25°C	I <sub>D</sub>	50	
– Continuous @ T <sub>A</sub> = 100°C	I <sub>DM</sub>	225	A pk
– Single Pulse (t <sub>p</sub> ≤ 10 μs)			
Total Power Dissipation @ T <sub>A</sub> = 25°C	P <sub>D</sub>	214	W
Derate above 25°C		1.4	W/°C
Total Power Dissipation @ T <sub>A</sub> = 25°C (Note 1)		2.4	W
Operating and Storage Temperature Range	T <sub>J</sub> , T <sub>stg</sub>	–55 to +175	°C
Single Pulse Drain-to-Source Avalanche Energy – Starting T <sub>J</sub> = 25°C (V <sub>DD</sub> = 50 Vdc, V <sub>GS</sub> = 5.0 Vdc, L = 0.3 mH I <sub>L(pk)</sub> = 75 A, V <sub>DS</sub> = 60 Vdc)	E <sub>AS</sub>	844	mJ
Thermal Resistance	R <sub>θJC</sub>	0.7	°C/W
– Junction-to-Case	R <sub>θJA</sub>	62.5	
– Junction-to-Ambient (Note 1)			
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 10 seconds	T <sub>L</sub>	260	°C

Maximum ratings are those values beyond which device damage can occur. Maximum ratings applied to the device are individual stress limit values (not normal operating conditions) and are not valid simultaneously. If these limits are exceeded, device functional operation is not implied, damage may occur and reliability may be affected.

1. When surface mounted to an FR4 board using minimum recommended pad size, (Cu Area 0.412 in<sup>2</sup>).

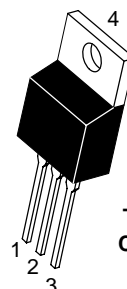
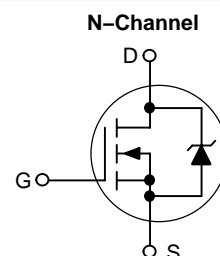


ON Semiconductor®

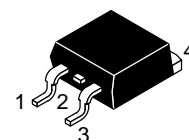
<http://onsemi.com>

75 AMPERES, 60 VOLTS

R<sub>DS(on)</sub> = 11 mΩ

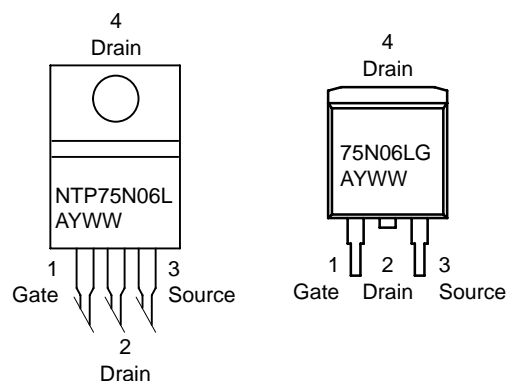


TO-220AB  
CASE 221A  
STYLE 5



D<sup>2</sup>PAK  
CASE 418B  
STYLE 2

#### MARKING DIAGRAMS & PIN ASSIGNMENTS



A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Package

#### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 5 of this data sheet.

# NTP75N06L, NTB75N06L

## ELECTRICAL CHARACTERISTICS (T<sub>J</sub> = 25°C unless otherwise noted)

Characteristic	Symbol	Min	Typ	Max	Unit
----------------	--------	-----	-----	-----	------

### OFF CHARACTERISTICS

Drain-to-Source Breakdown Voltage (Note 2) (V <sub>GS</sub> = 0 Vdc, I <sub>D</sub> = 250 μAdc) Temperature Coefficient (Positive)	V <sub>(BR)DSS</sub>	60 –	72 74	– –	Vdc mV/°C
Zero Gate Voltage Drain Current (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc) (V <sub>DS</sub> = 60 Vdc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	I <sub>DSS</sub>	– –	– –	10 100	μAdc
Gate-Body Leakage Current (V <sub>GS</sub> = ±15 Vdc, V <sub>DS</sub> = 0 Vdc)	I <sub>GSS</sub>	–	–	±100	nAdc

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage (Note 2) (V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250 μAdc) Threshold Temperature Coefficient (Negative)	V <sub>GS(th)</sub>	1.0 –	1.58 6.0	2.0 –	Vdc mV/°C
Static Drain-to-Source On-Resistance (Note 2) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 37.5 Adc)	R <sub>DS(on)</sub>	–	9.0	11	mΩ
Static Drain-to-Source On-Voltage (Note 2) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 75 Adc) (V <sub>GS</sub> = 5.0 Vdc, I <sub>D</sub> = 37.5 Adc, T <sub>J</sub> = 150°C)	V <sub>DS(on)</sub>	– –	0.75 0.61	0.99 –	Vdc
Forward Transconductance (Note 2) (V <sub>DS</sub> = 15 Vdc, I <sub>D</sub> = 37.5 Adc)	g <sub>FS</sub>	–	55	–	mhos

### DYNAMIC CHARACTERISTICS

Input Capacitance	(V <sub>DS</sub> = 25 Vdc, V <sub>GS</sub> = 0 Vdc, f = 1.0 MHz)	C <sub>iss</sub>	–	3122	4370	pF
Output Capacitance		C <sub>oss</sub>	–	1029	1440	
Transfer Capacitance		C <sub>rss</sub>	–	276	390	

### SWITCHING CHARACTERISTICS (Note 3)

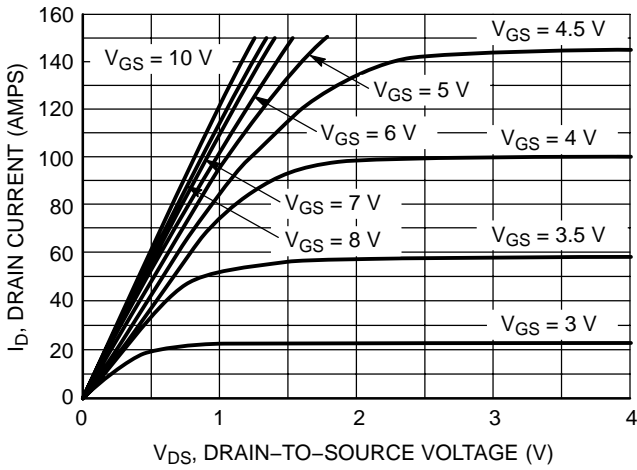
Turn-On Delay Time	(V <sub>DD</sub> = 30 Vdc, I <sub>D</sub> = 75 Adc, V <sub>GS</sub> = 5.0 Vdc, R <sub>G</sub> = 9.1 Ω) (Note 2)	t <sub>d(on)</sub>	–	22	32	ns
Rise Time		t <sub>r</sub>	–	265	370	
Turn-Off Delay Time		t <sub>d(off)</sub>	–	113	160	
Fall Time		t <sub>f</sub>	–	170	240	
Gate Charge	(V <sub>DS</sub> = 48 Vdc, I <sub>D</sub> = 75 Adc, V <sub>GS</sub> = 5.0 Vdc) (Note 2)	Q <sub>T</sub>	–	66	92	nC
	Q <sub>1</sub>	–	9.0	–		
	Q <sub>2</sub>	–	47	–		

### SOURCE-DRAIN DIODE CHARACTERISTICS

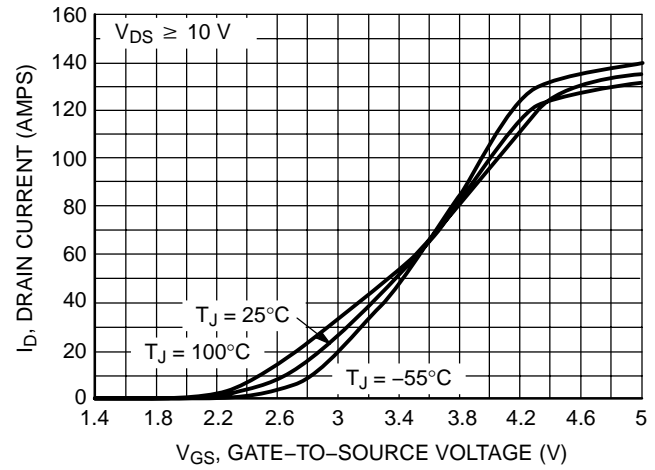
Forward On-Voltage	(I <sub>S</sub> = 75 Adc, V <sub>GS</sub> = 0 Vdc) (Note 2) (I <sub>S</sub> = 75 Adc, V <sub>GS</sub> = 0 Vdc, T <sub>J</sub> = 150°C)	V <sub>SD</sub>	– –	1.0 0.9	1.15 –	Vdc
Reverse Recovery Time	(I <sub>S</sub> = 75 Adc, V <sub>GS</sub> = 0 Vdc, di <sub>S</sub> /dt = 100 A/μs) (Note 2)	t <sub>rr</sub>	–	70	–	ns
	t <sub>a</sub>	–	43	–		
	t <sub>b</sub>	–	27	–		
Reverse Recovery Stored Charge		Q <sub>RR</sub>	–	0.16	–	μC

2. Pulse Test: Pulse Width ≤ 300 μs, Duty Cycle ≤ 2%.
3. Switching characteristics are independent of operating junction temperatures.

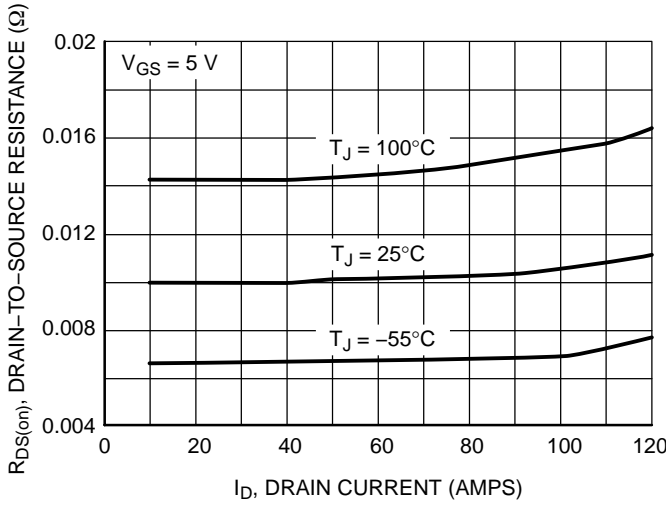
# NTP75N06L, NTB75N06L



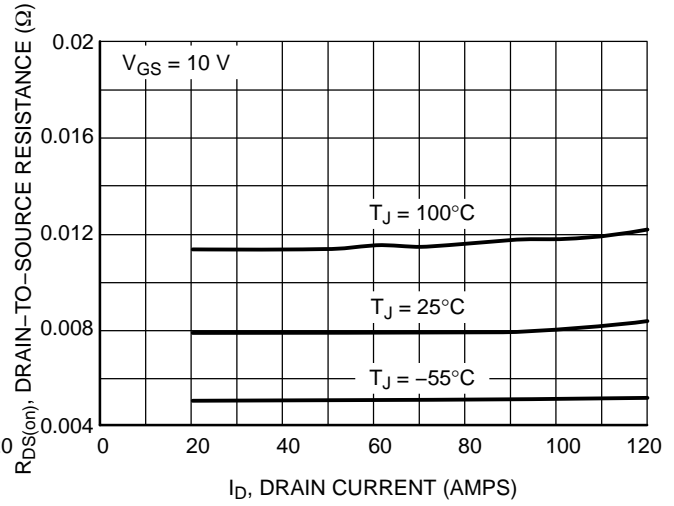
**Figure 1. On-Region Characteristics**



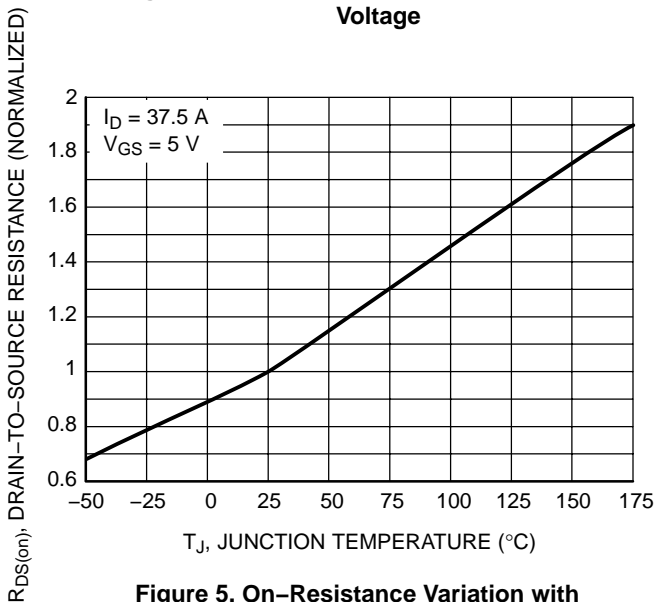
**Figure 2. Transfer Characteristics**



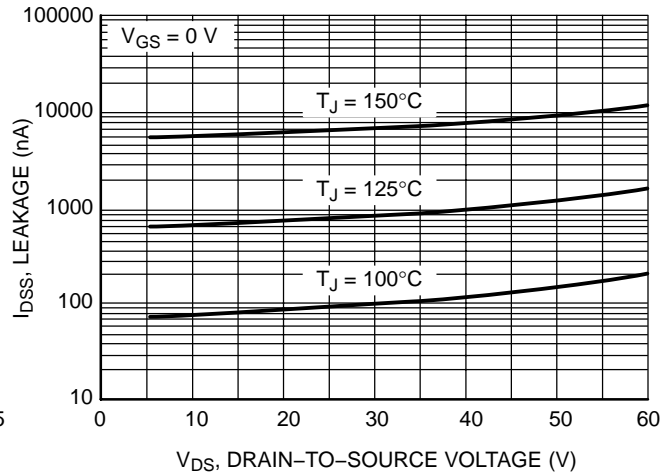
**Figure 3. On-Resistance vs. Gate-to-Source Voltage**



**Figure 4. On-Resistance vs. Drain Current and Gate Voltage**



**Figure 5. On-Resistance Variation with Temperature**



**Figure 6. Drain-to-Source Leakage Current vs. Voltage**

# NTP75N06L, NTB75N06L

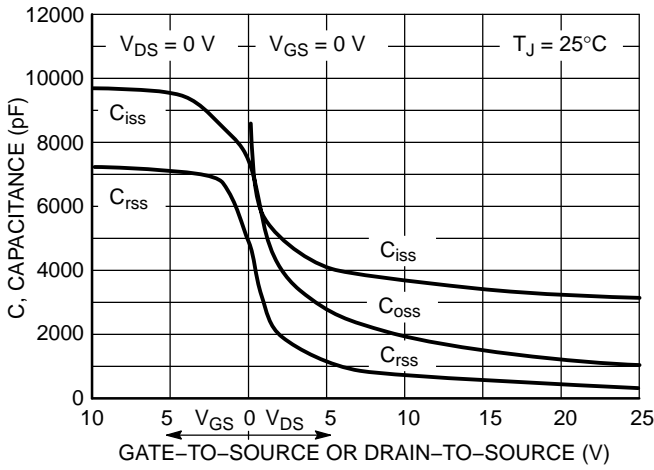


Figure 7. Capacitance Variation

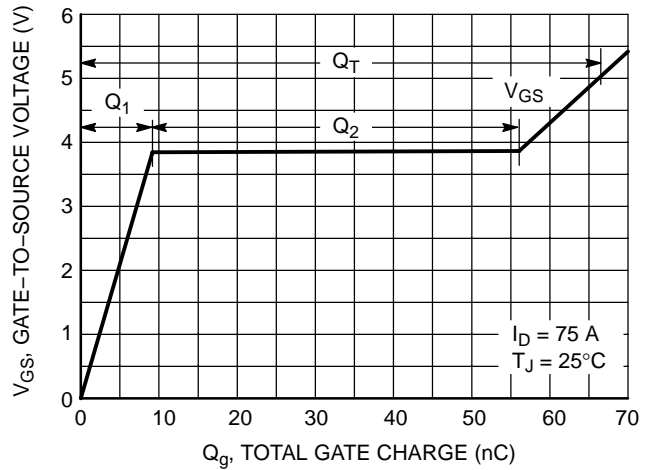


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

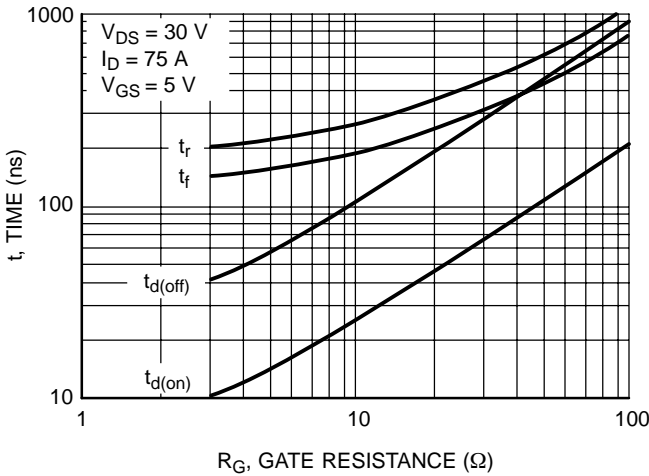


Figure 9. Resistive Switching Time Variations vs. Gate Resistance

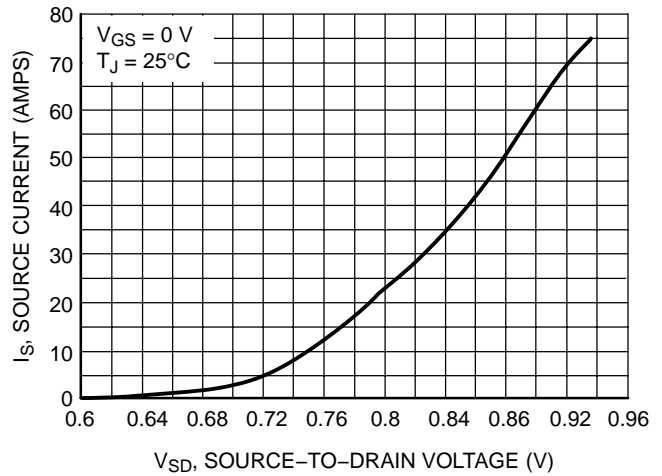


Figure 10. Diode Forward Voltage vs. Current

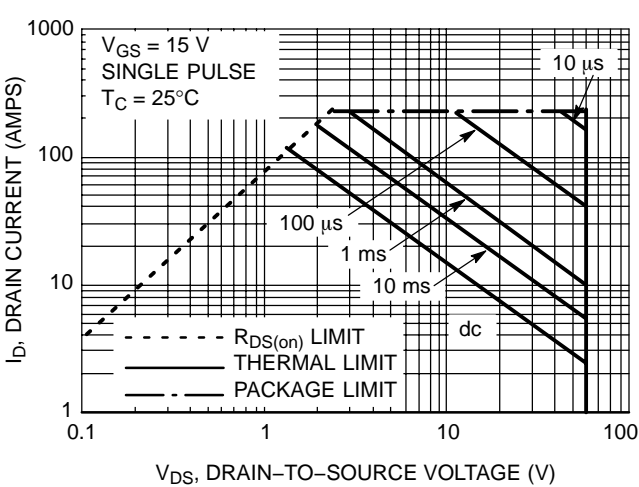


Figure 11. Maximum Rated Forward Biased Safe Operating Area

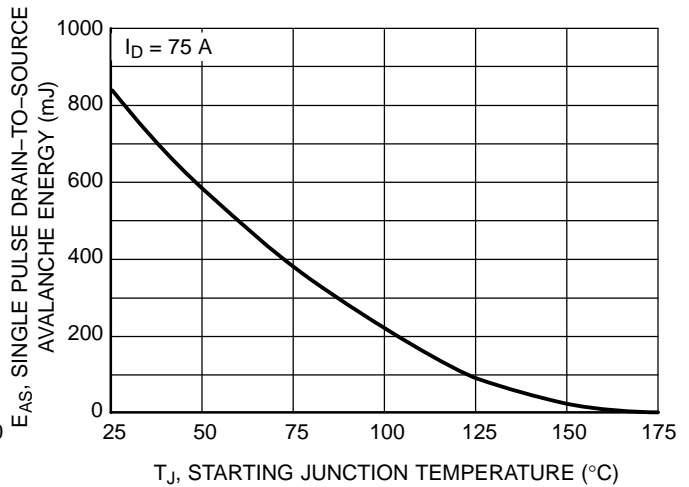


Figure 12. Maximum Avalanche Energy vs. Starting Junction Temperature

# NTP75N06L, NTB75N06L

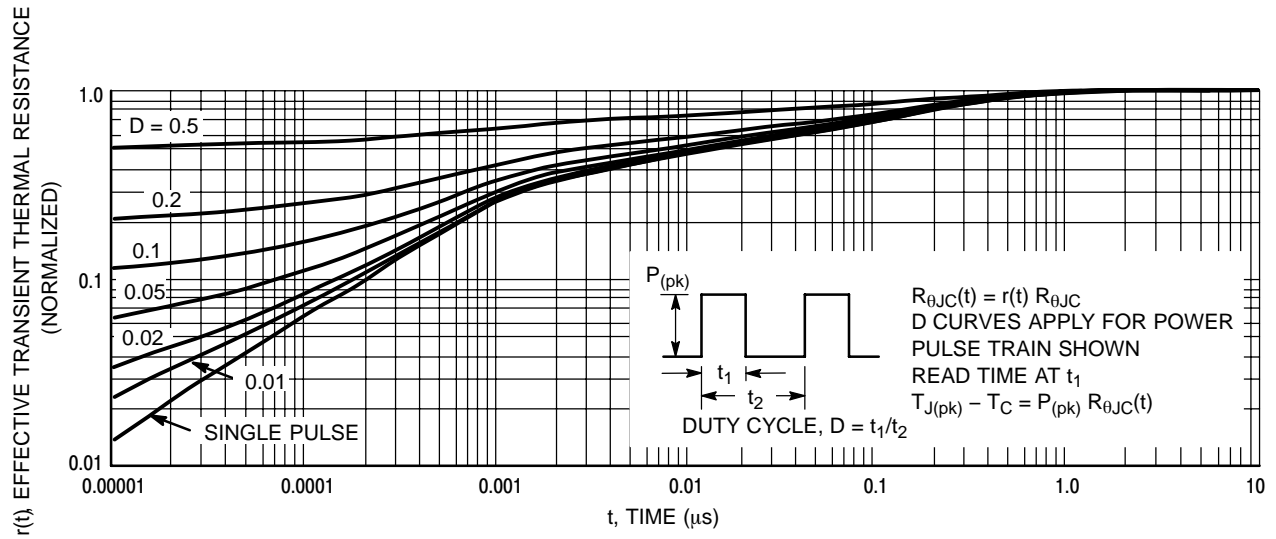


Figure 13. Thermal Response

## ORDERING INFORMATION

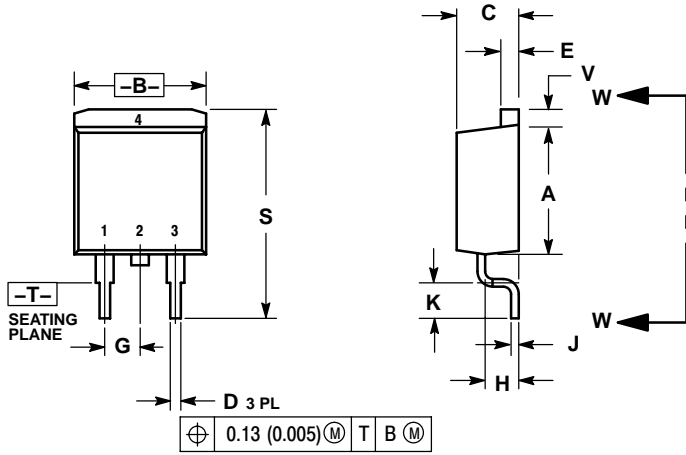
Device	Package	Shipping†
NTP75N06L	TO-220AB	50 Units / Rail
NTB75N06L	D <sup>2</sup> PAK	50 Units / Rail
NTB75N06LG	D <sup>2</sup> PAK (Pb-Free)	50 Units / Rail
NTB75N06LT4	D <sup>2</sup> PAK	800 Units / Tape & Reel
NTB75N06LT4G	D <sup>2</sup> PAK (Pb-Free)	800 Units / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NTP75N06L, NTB75N06L

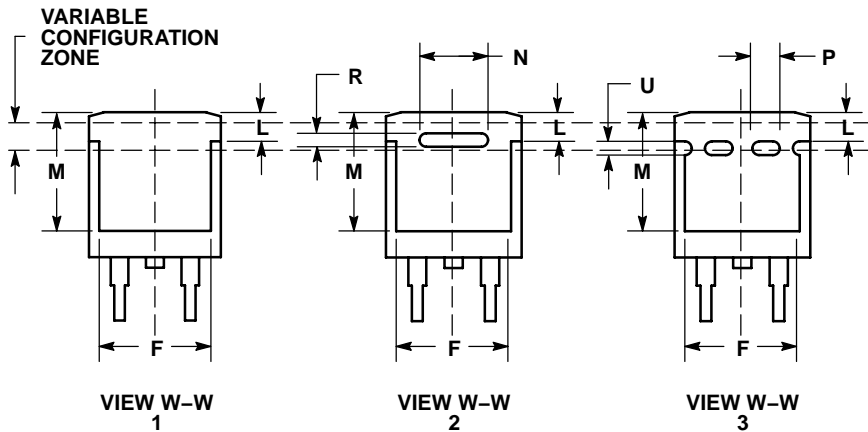
## PACKAGE DIMENSIONS

**D<sup>2</sup>PAK**  
CASE 418B-04  
ISSUE J



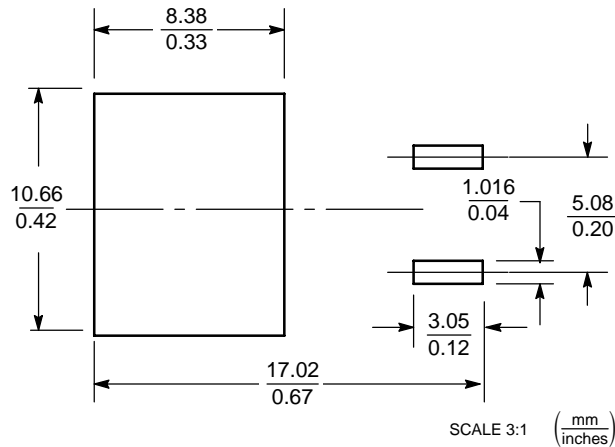
- NOTES:
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
  2. CONTROLLING DIMENSION: INCH.
  3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



- STYLE 2:
- PIN 1. GATE
  - DRAIN
  - SOURCE
  - DRAIN

### SOLDERING FOOTPRINT\*

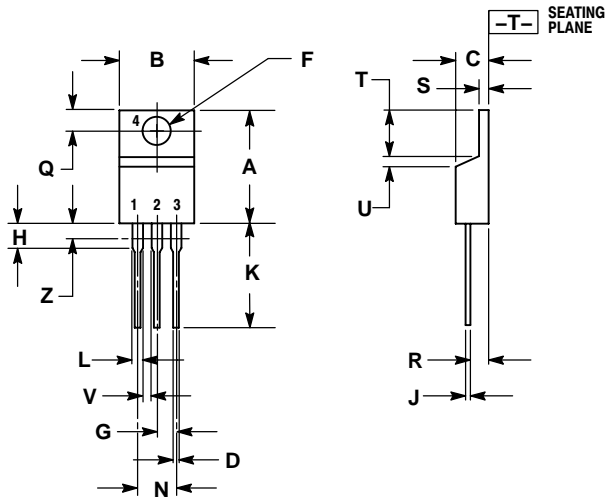


\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NTP75N06L, NTB75N06L

## PACKAGE DIMENSIONS

TO-220  
CASE 221A-09  
ISSUE AA



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.147	3.61	3.73
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.018	0.025	0.46	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 5:

- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 61312, Phoenix, Arizona 85082-1312 USA  
**Phone:** 480-829-7710 or 800-344-3860 Toll Free USA/Canada  
**Fax:** 480-829-7709 or 800-344-3867 Toll Free USA/Canada  
**Email:** orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada

**Japan:** ON Semiconductor, Japan Customer Focus Center  
2-9-1 Kamimeguro, Meguro-ku, Tokyo, Japan 153-0051  
**Phone:** 81-3-5773-3850

**ON Semiconductor Website:** <http://onsemi.com>

**Order Literature:** <http://www.onsemi.com/litorder>

For additional information, please contact your local Sales Representative.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View NTB75N06LT4G on WIN SOURCE](#)

 [ON Semiconductor](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management