



THE DATASHEET OF PMN50UPE,115



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PMN50UPE

20 V, single P-channel Trench MOSFET

20 July 2012

Product data sheet

1. Product profile

1.1 General description

P-channel enhancement mode Field-Effect Transistor (FET) in a small SOT457 (SC-74) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

1.2 Features and benefits

- 3 kV ESD protected
- Trench MOSFET technology
- Low threshold voltage

1.3 Applications

- Relay driver
- High-side loadswitch
- Switching circuits

1.4 Quick reference data

Table 1. Quick reference data

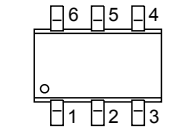
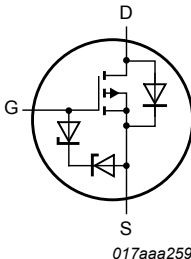
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ °C}$	-	-	-20	V
V_{GS}	gate-source voltage		-8	-	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	-4	A
Static characteristics						
R_{DSon}	drain-source on-state resistance	$V_{GS} = -4.5\text{ V}; I_D = -3.6\text{ A}; T_j = 25\text{ °C}$	-	50	66	m Ω

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².



2. Pinning information

Table 2. Pinning information

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	D	drain	 <p>TSOP6 (SOT457)</p>	 <p>017aaa259</p>
2	D	drain		
3	G	gate		
4	S	source		
5	D	drain		
6	D	drain		

3. Ordering information

Table 3. Ordering information

Type number	Package		
	Name	Description	Version
PMN50UPE	TSOP6	plastic surface-mounted package (TSOP6); 6 leads	SOT457

4. Marking

Table 4. Marking codes

Type number	Marking code
PMN50UPE	WH

5. Limiting values

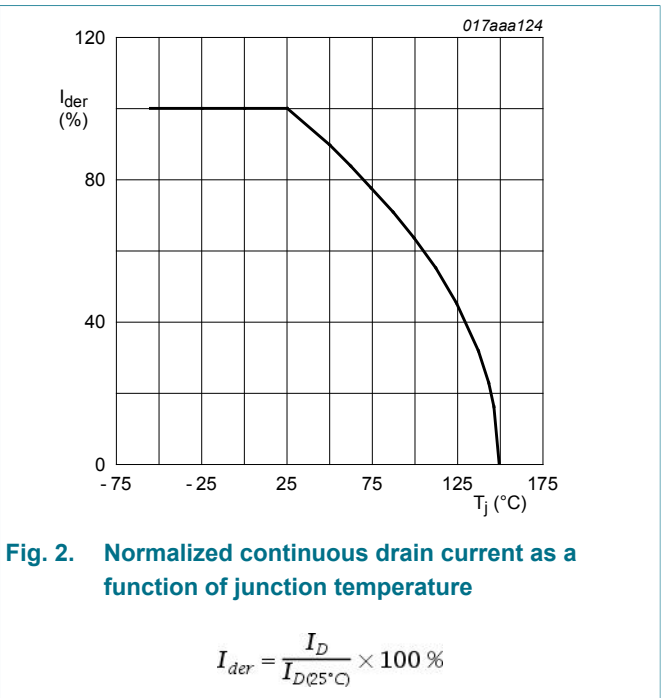
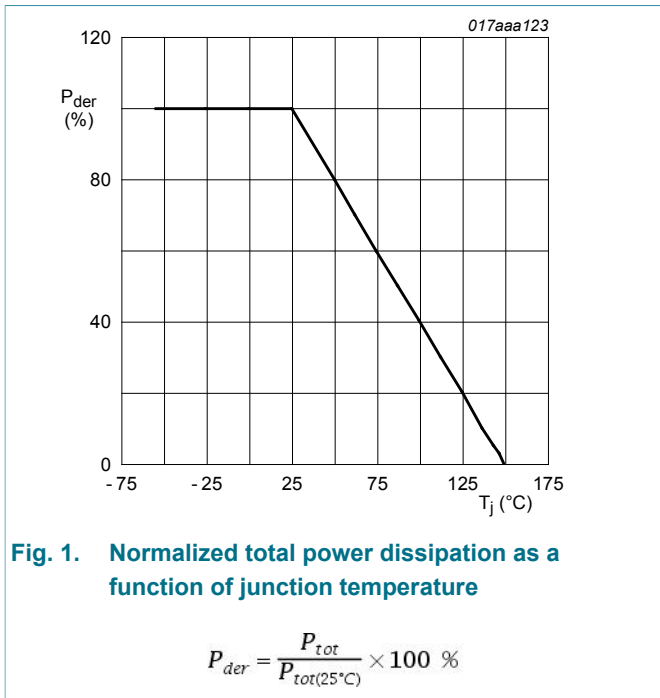
Table 5. Limiting values

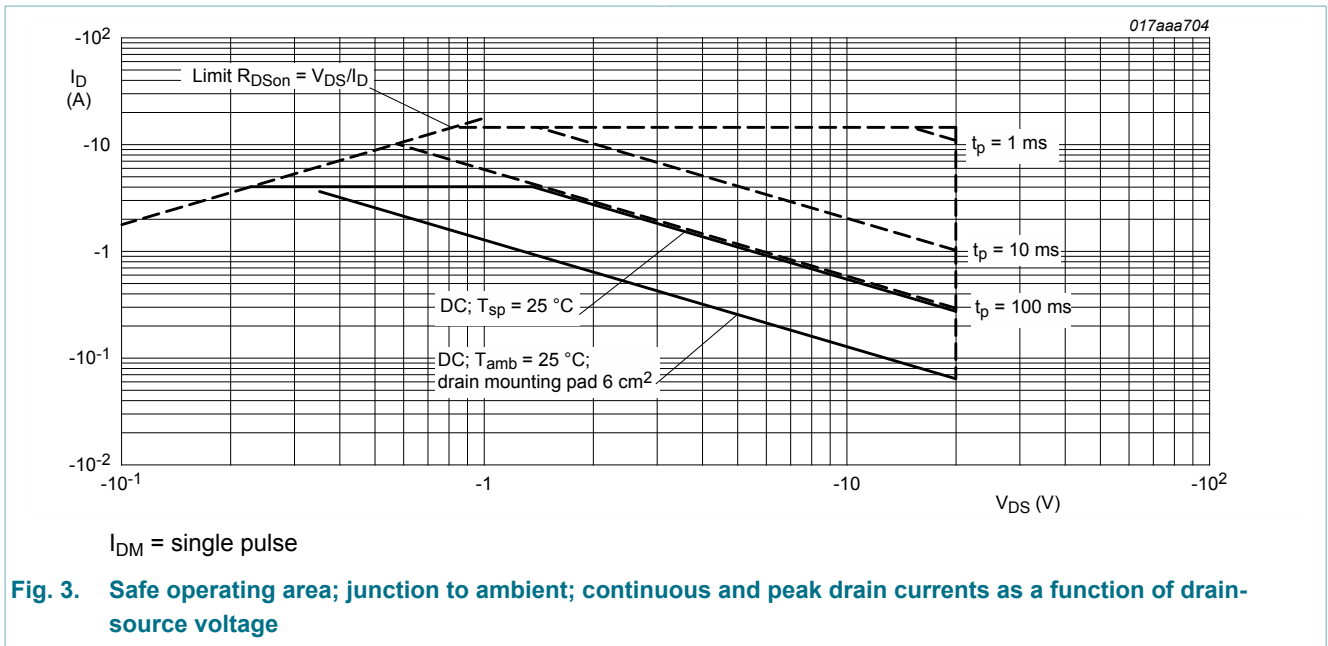
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions		Min	Max	Unit
V_{DS}	drain-source voltage	$T_j = 25\text{ }^\circ\text{C}$		-	-20	V
V_{GS}	gate-source voltage			-8	8	V
I_D	drain current	$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}; t \leq 5\text{ s}$	[1]	-	-4	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 25\text{ }^\circ\text{C}$	[1]	-	-3.6	A
		$V_{GS} = -4.5\text{ V}; T_{amb} = 100\text{ }^\circ\text{C}$	[1]	-	-2.3	A
I_{DM}	peak drain current	$T_{amb} = 25\text{ }^\circ\text{C}; \text{single pulse}; t_p \leq 10\text{ }\mu\text{s}$		-	-14.4	A
P_{tot}	total power dissipation	$T_{amb} = 25\text{ }^\circ\text{C}$	[2]	-	510	mW
			[1]	-	1235	mW
		$T_{sp} = 25\text{ }^\circ\text{C}$		-	5000	mW

Symbol	Parameter	Conditions		Min	Max	Unit
T _j	junction temperature			-55	150	°C
T _{amb}	ambient temperature			-55	150	°C
T _{stg}	storage temperature			-65	150	°C
Source-drain diode						
I _s	source current	T _{amb} = 25 °C	[1]	-	-1.3	A
ESD maximum rating						
V _{ESD}	electrostatic discharge voltage	HBM	[3]	-	3000	V

- [1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm².
- [2] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated and standard footprint.
- [3] Measured between all pins.





6. Thermal characteristics

Table 6. Thermal characteristics

Symbol	Parameter	Conditions		Min	Typ	Max	Unit
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	213	245	K/W
			[2]	-	88	100	K/W
			[3]	-	70	81	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	21	25	K/W	

[1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm².

[3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain 6 cm², t ≤ 5 s.

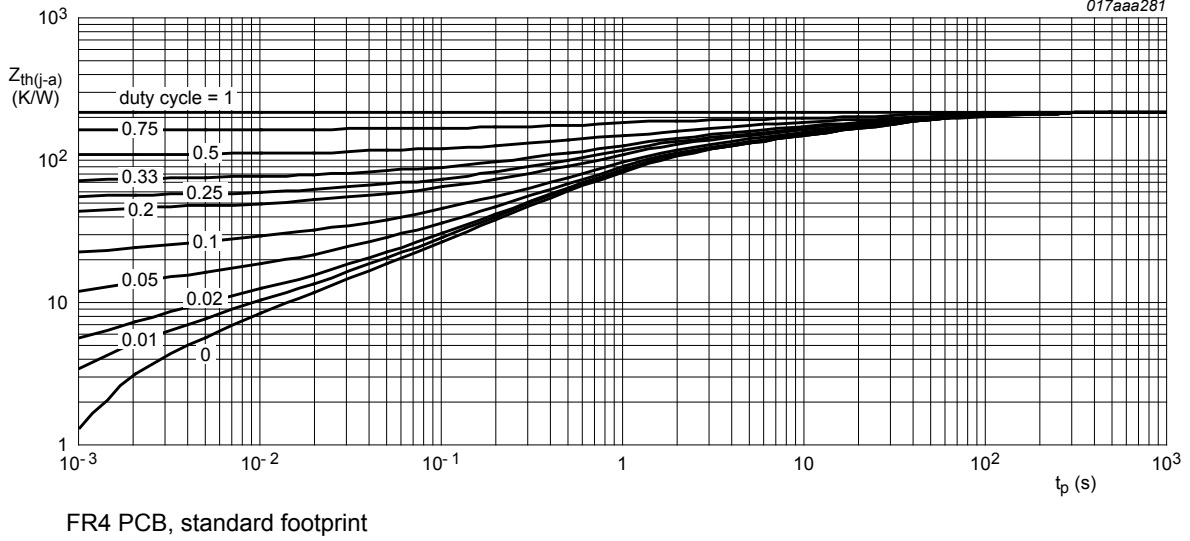


Fig. 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

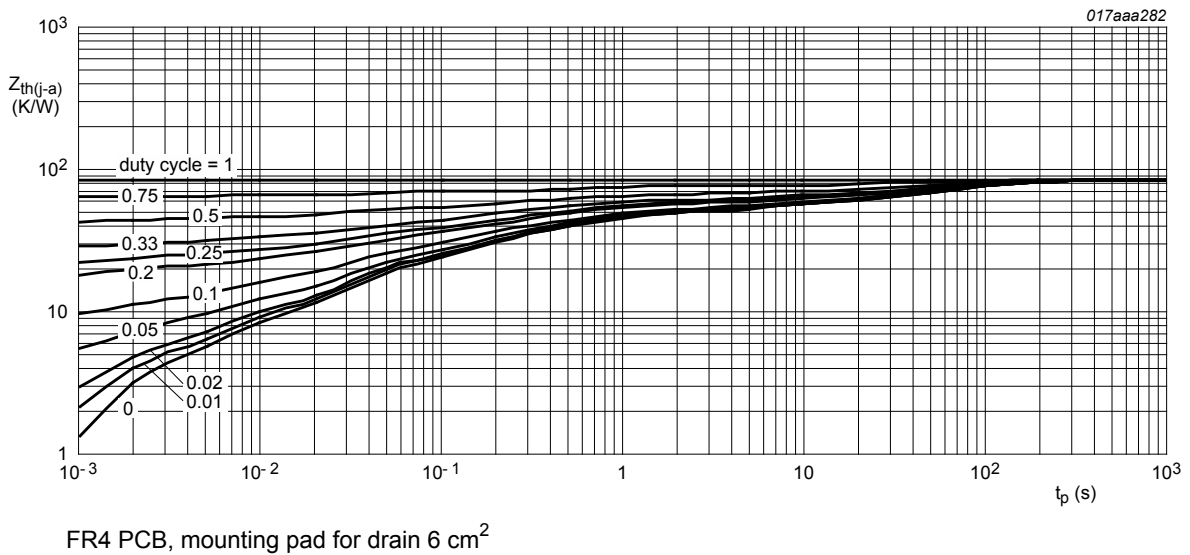


Fig. 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

7. Characteristics

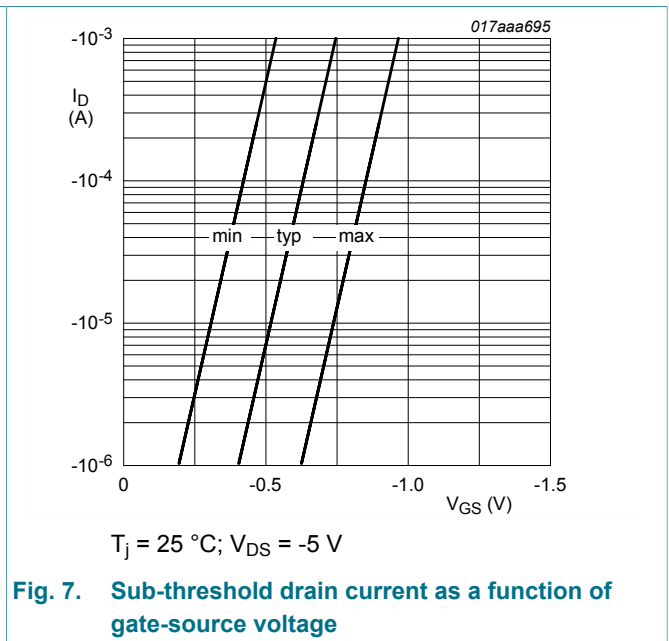
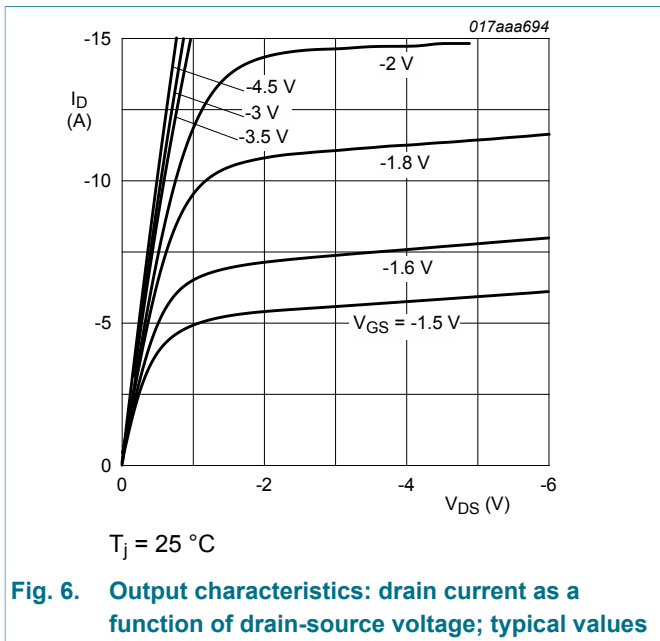
Table 7. Characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = -250 \mu A; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-20	-	-	V
V_{GSth}	gate-source threshold voltage	$I_D = -250 \mu A; V_{DS} = V_{GS}; T_j = 25 \text{ }^\circ C$	-0.47	-0.6	-0.9	V
I_{DSS}	drain leakage current	$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 25 \text{ }^\circ C$	-	-	-1	μA
		$V_{DS} = -20 V; V_{GS} = 0 V; T_j = 150 \text{ }^\circ C$	-	-	-10	μA

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
I _{GSS}	gate leakage current	V _{GS} = -8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	10	μA
		V _{GS} = 8 V; V _{DS} = 0 V; T _j = 25 °C	-	-	-10	μA
R _{DSon}	drain-source on-state resistance	V _{GS} = -4.5 V; I _D = -3.6 A; T _j = 25 °C	-	50	66	mΩ
		V _{GS} = -4.5 V; I _D = -3.6 A; T _j = 150 °C	-	73	96	mΩ
		V _{GS} = -2.5 V; I _D = -2.1 A; T _j = 25 °C	-	57	81	mΩ
		V _{GS} = -1.8 V; I _D = -2.1 A; T _j = 25 °C	-	70	110	mΩ
g _{fs}	forward transconductance	V _{DS} = -5 V; I _D = -3.6 A; T _j = 25 °C	-	18	-	S

Dynamic characteristics						
Q _{G(tot)}	total gate charge	V _{DS} = -10 V; I _D = -3.2 A; V _{GS} = -4.5 V; T _j = 25 °C	-	10.5	15.7	nC
Q _{GS}	gate-source charge		-	2.2	-	nC
Q _{GD}	gate-drain charge		-	2.7	-	nC
C _{iss}	input capacitance	V _{DS} = -10 V; f = 1 MHz; V _{GS} = 0 V; T _j = 25 °C	-	24	-	pF
C _{oss}	output capacitance		-	106	-	pF
C _{rss}	reverse transfer capacitance		-	14.6	-	pF
t _{d(on)}	turn-on delay time	V _{DS} = -10 V; I _D = -3.6 A; V _{GS} = -4.5 V; R _{G(ext)} = 6 Ω; T _j = 25 °C	-	400	-	ns
t _r	rise time		-	700	-	ns
t _{d(off)}	turn-off delay time		-	2180	-	ns
t _f	fall time		-	8800	-	ns

Source-drain diode						
V _{SD}	source-drain voltage	I _S = -1.3 A; V _{GS} = 0 V; T _j = 25 °C	-	-0.8	-1.2	V



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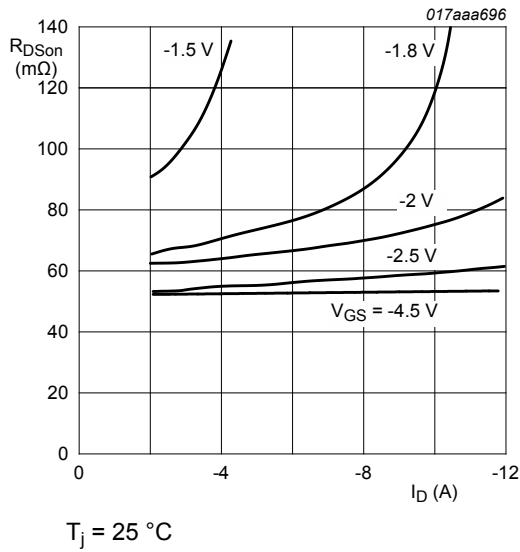


Fig. 8. Drain-source on-state resistance as a function of drain current; typical values

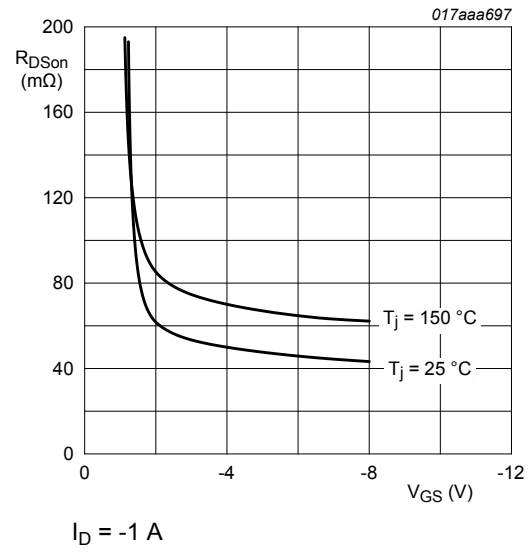


Fig. 9. Drain-source on-state resistance as a function of gate-source voltage; typical values

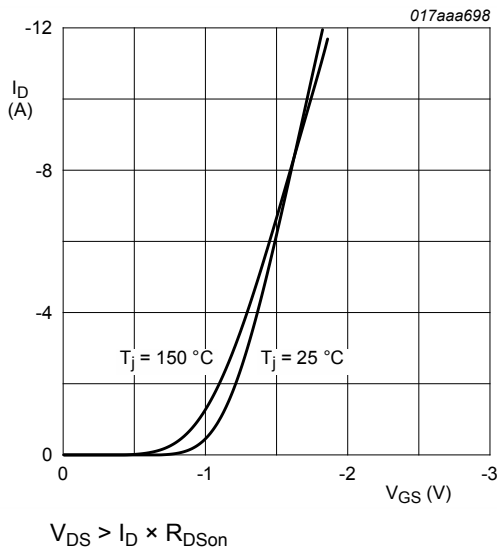


Fig. 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values

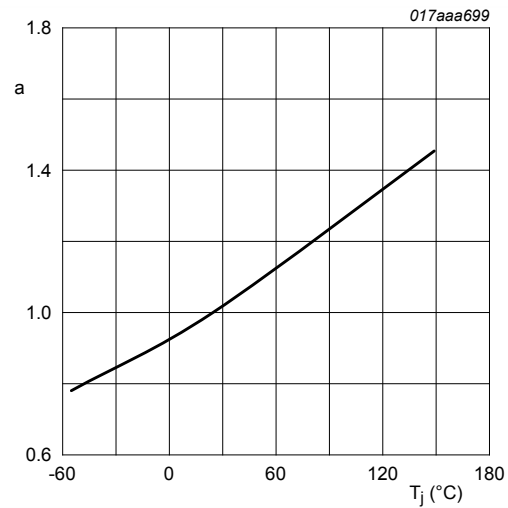


Fig. 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values

$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

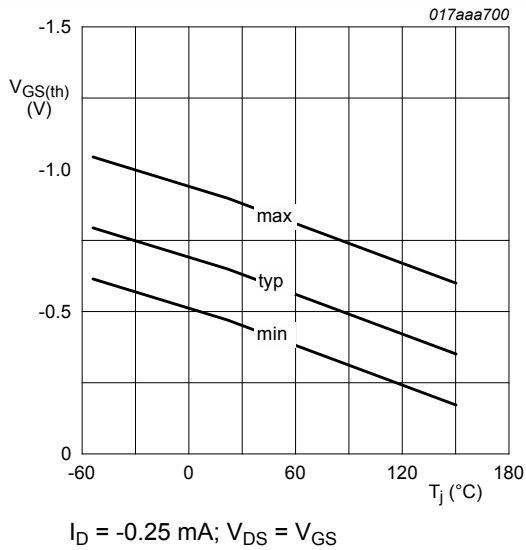


Fig. 12. Gate-source threshold voltage as a function of junction temperature

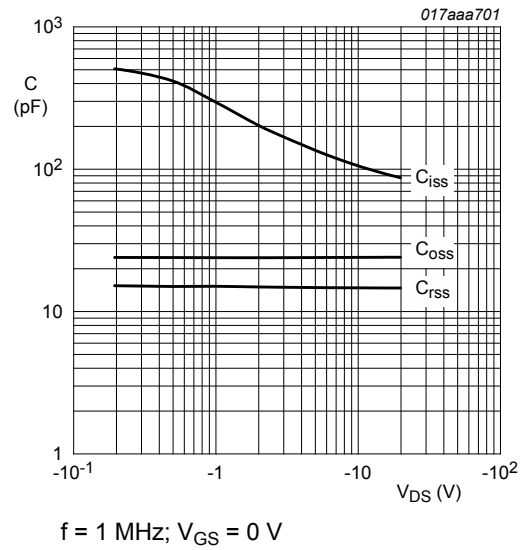


Fig. 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values

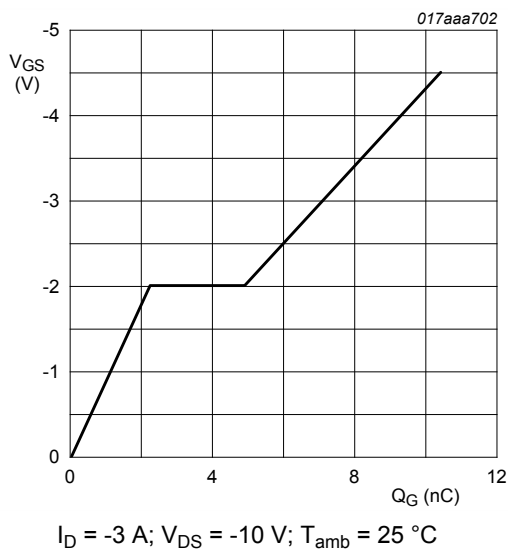


Fig. 14. Gate-source voltage as a function of gate charge; typical values

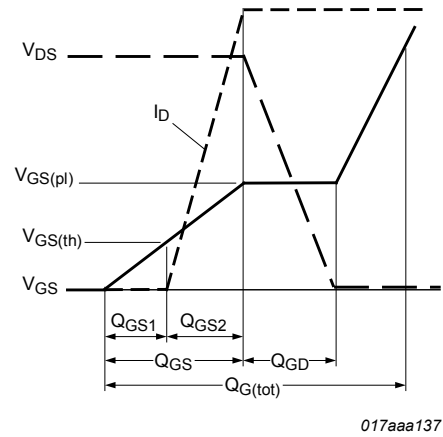
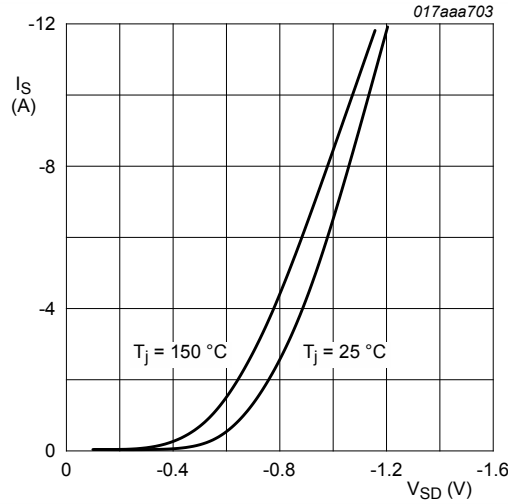


Fig. 15. Gate charge waveform definitions



$V_{GS} = 0\text{ V}$

Fig. 16. Source current as a function of source-drain voltage; typical values

8. Test information

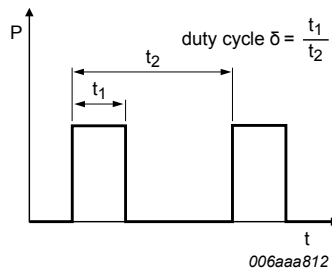


Fig. 17. Duty cycle definition

9. Package outline

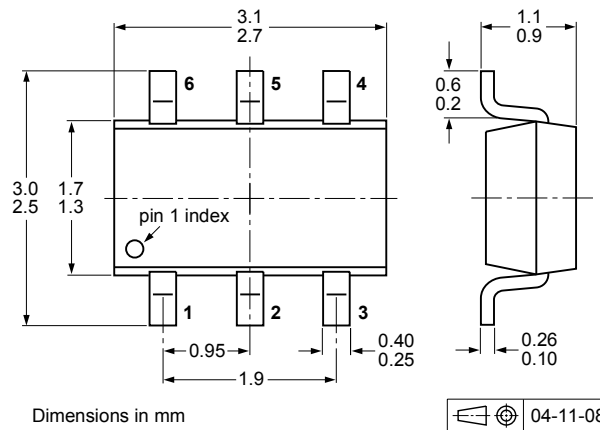


Fig. 18. TSOP6 (SOT457)

10. Soldering

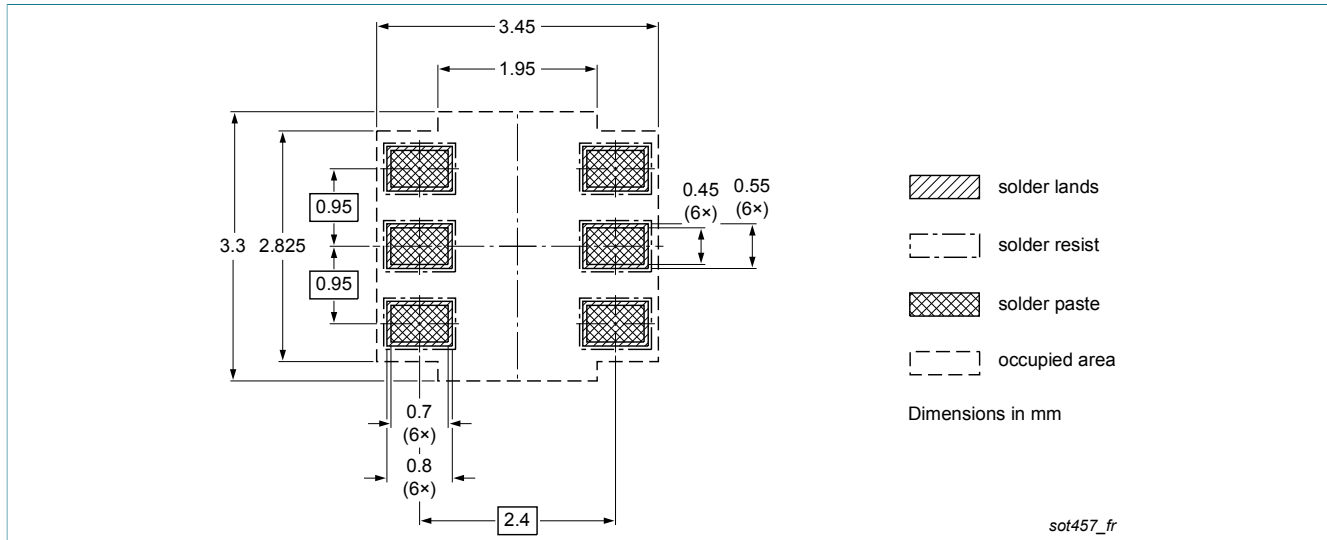


Fig. 19. Reflow soldering footprint for SOT457 (TSOP6)

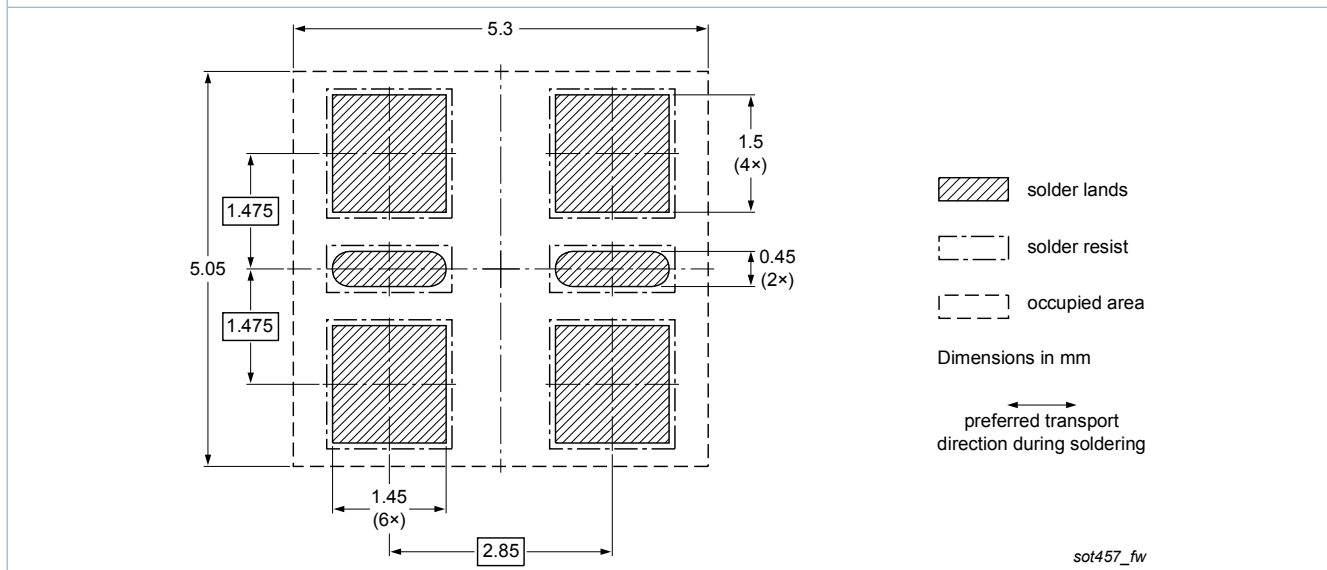


Fig. 20. Wave soldering footprint for SOT457 (TSOP6)

11. Revision history

Table 8. Revision history

Data sheet ID	Release date	Data sheet status	Change notice	Supersedes
PMN50UPE v.1	20120720	Product data sheet	-	-

12. Legal information

12.1 Data sheet status

Document status [1][2]	Product status [3]	Definition
Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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Date of release: 20 July 2012

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