



# THE DATASHEET OF IRF644NS





**Power MOSFET**

PRODUCT SUMMARY	
V <sub>DS</sub> (V)	250 V
R <sub>DS(on)</sub> (Ω)	V <sub>GS</sub> = 10 V      0.240
Q <sub>g</sub> (Max.) (nC)	54
Q <sub>gs</sub> (nC)	9.2
Q <sub>gd</sub> (nC)	26
Configuration	Single

**FEATURES**

- Advanced Process Technology
- Dynamic dV/dt Rating
- 175 °C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Ease of Paralleling
- Simple Drive Requirements
- Lead (Pb)-free Available

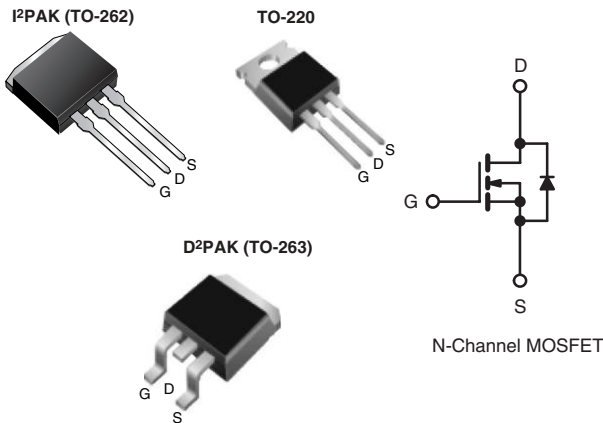


**DESCRIPTION**

Fifth generation Power MOSFETs from Vishay utilize advanced processing techniques to achieve extremely low on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that Power MOSFETs are well known for, provides the designer with an extremely efficient and reliable device for use in a wide variety of applications.

The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 W. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

The D<sup>2</sup>PAK is a surface mount power package capable of accommodating die sizes up to HEX-4. It provides the highest power capability and the lowest possible on resistance in any existing surface mount package. The D<sup>2</sup>PAK is suitable for high current applications because of its low internal connection resistance and can dissipate up to 2.0 W in a typical surface mount application.



ORDERING INFORMATION					
Package	TO-220	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	D <sup>2</sup> PAK (TO-263)	I <sup>2</sup> PAK (TO-262)
Lead (Pb)-free	IRF644NPbF	IRF644NSPbF	IRF644NSTRLPbF <sup>a</sup>	IRF644NSTRRPbF <sup>a</sup>	IRF644NLPbF
	SiHF644N-E3	SiHF644NS-E3	SiHF644NSTL-E3 <sup>a</sup>	SiHF644NSTR-E3 <sup>a</sup>	SiHF644NL-E3
SnPb	IRF644N	IRF644NS	IRF644NSTRL <sup>a</sup>	IRF644NSTR <sup>a</sup>	IRF644NL
	SiHF644N	SiHF644NS	SiHF644NSTL <sup>a</sup>	SiHF644NSTR <sup>a</sup>	SiHF644NL

**Note**

a. See device orientation.

\* Pb containing terminations are not RoHS compliant, exemptions may apply



ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted					
PARAMETER		SYMBOL	LIMIT	UNIT	
Drain-Source Voltage		$V_{DS}$	250	V	
Gate-Source Voltage		$V_{GS}$	$\pm 20$		
Continuous Drain Current	$V_{GS}$ at 10 V	$I_D$	$T_C = 25\text{ }^\circ\text{C}$	14	A
			$T_C = 100\text{ }^\circ\text{C}$	9.9	
Pulsed Drain Current <sup>a</sup>		$I_{DM}$	56		
Linear Derating Factor			1.0	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>		$E_{AS}$	180 <sup>e</sup>	mJ	
Avalanche Current		$I_{AR}$	8.4	A	
Repetitive Avalanche Energy		$E_{AR}$	15	mJ	
Maximum Power Dissipation		$P_D$	150	W	
Peak Diode Recovery $dV/dt^c$		$dV/dt$	7.9	V/ns	
Operating Junction and Storage Temperature Range		$T_J, T_{stg}$	- 55 to + 175	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)		for 10 s	300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw		10	lbf · in	
			1.1	N · m	

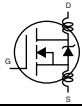

**Notes**

- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 5.0\text{ }\mu\text{H}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 8.4\text{ A}$  (see fig. 12).
- c.  $I_{SD} \leq 8.4\text{ A}$ ,  $dl/dt \leq 378\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 175\text{ }^\circ\text{C}$ .
- d. 1.6 mm from case.
- e. This is a calculated value limited to  $T_J = 175\text{ }^\circ\text{C}$ .

THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient <sup>c</sup>	$R_{thJA}$	-	62	$^\circ\text{C}/\text{W}$
Case-to-Sink, Flat, Greased Surface <sup>c</sup>	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	1.0	
Maximum Junction-to-Ambient (PCB Mount) <sup>d</sup>	$R_{thJA}$	-	40	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted						
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
<b>Static</b>						
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}$ , $I_D = 250\text{ }\mu\text{A}$	250	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$	-	0.33	-	V/ $^\circ\text{C}$
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}$ , $I_D = 250\text{ }\mu\text{A}$	2.0	-	4.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = 20\text{ V}$	-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 250\text{ V}$ , $V_{GS} = 0\text{ V}$	-	-	25	$\mu\text{A}$
		$V_{DS} = 200\text{ V}$ , $V_{GS} = 0\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$	-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$ , $I_D = 8.4\text{ A}^b$	-	-	0.240	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}$ , $I_D = 8.4\text{ A}^b$	8.8	-	-	S

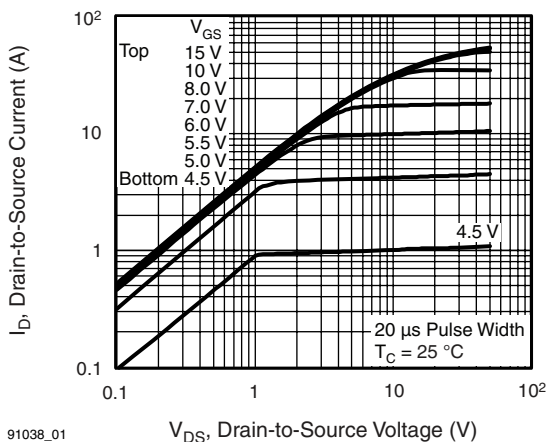


SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX. UNIT	
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V}$ , $V_{DS} = 25\text{ V}$ , $f = 1.0\text{ MHz}$ , see fig. 5		-	1060	-	pF
Output Capacitance	$C_{oss}$			-	140	-	
Reverse Transfer Capacitance	$C_{rss}$			-	38	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 8.4\text{ A}$ , $V_{DS} = 200\text{ V}$ , see fig. 6 and 13 <sup>b</sup>	-	-	54	nC
Gate-Source Charge	$Q_{gs}$			-	-	9.2	
Gate-Drain Charge	$Q_{gd}$			-	-	26	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 125\text{ V}$ , $I_D = 8.4\text{ A}$ , $R_G = 6.2\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ , see fig. 10 <sup>b</sup>		-	10	-	ns
Rise Time	$t_r$			-	21	-	
Turn-Off Delay Time	$t_{d(off)}$			-	30	-	
Fall Time	$t_f$			-	17	-	
Internal Drain Inductance	$L_D$	Between lead, 6 mm (0.25") from package and center of die contact 		-	4.5	-	nH
Internal Source Inductance	$L_S$			-	7.5	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	14	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	56	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_S = 14\text{ A}$ , $V_{GS} = 0\text{ V}$ <sup>b</sup>		-	-	1.3	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}$ , $I_F = 14\text{ A}$ , $dI/dt = 100\text{ A}/\mu\text{s}$ <sup>b</sup>		-	165	250	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	1.0	1.6	$\mu\text{C}$
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

**Notes**

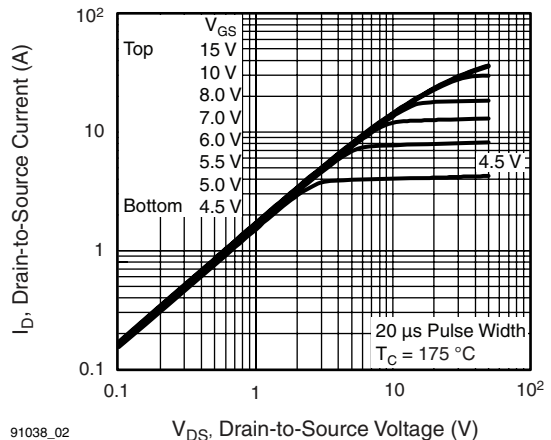
- a. Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .
- c. This is only applied to TO-220 package.
- d. When mounted on 1" square PCB (fr-4 or G-10 material).

**TYPICAL CHARACTERISTICS**  $25\text{ }^\circ\text{C}$ , unless otherwise noted



91038\_01

Fig. 1 - Typical Output Characteristics



91038\_02

Fig. 2 - Typical Output Characteristics

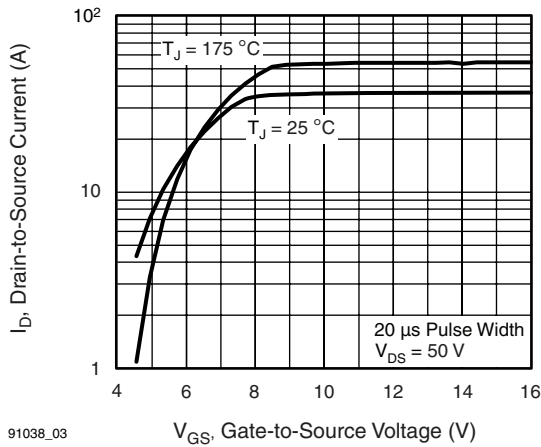


Fig. 3 - Typical Transfer Characteristics

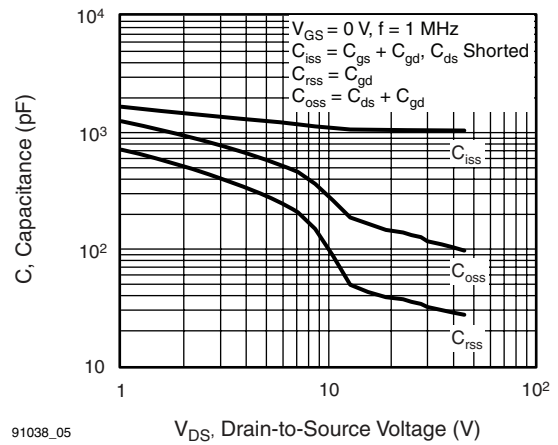


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

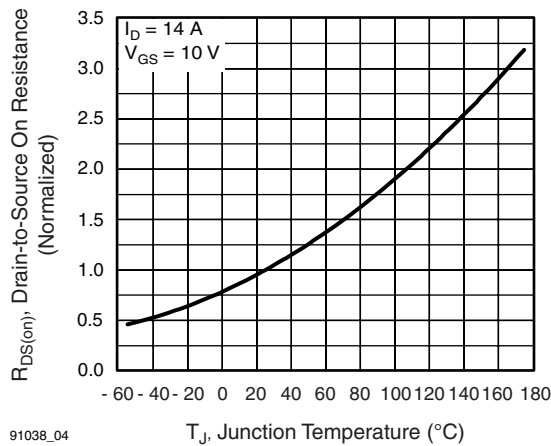


Fig. 4 - Normalized On-Resistance vs. Temperature

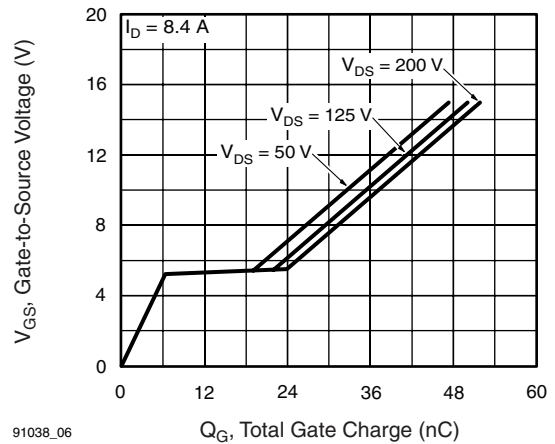
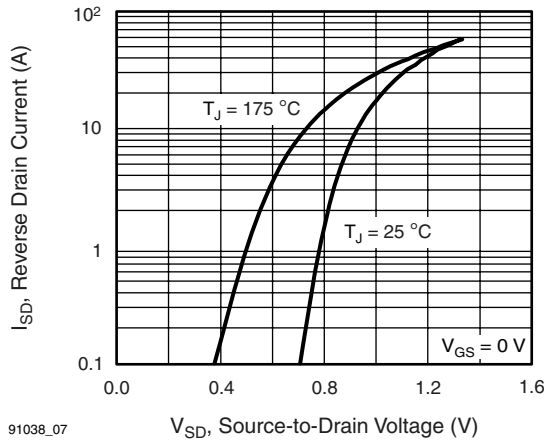
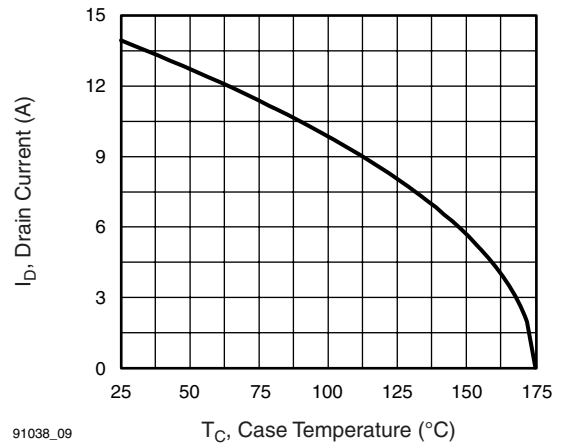


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage



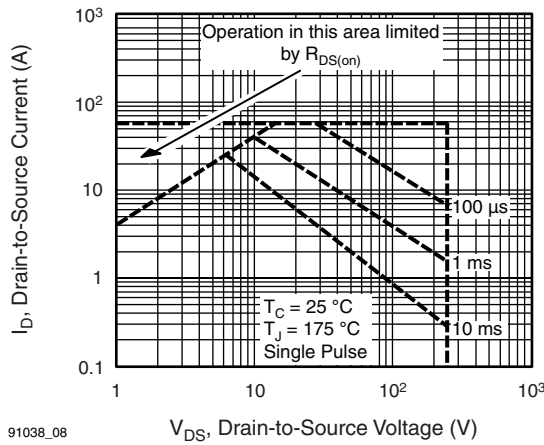
91038\_07

**Fig. 7 - Typical Source-Drain Diode Forward Voltage**



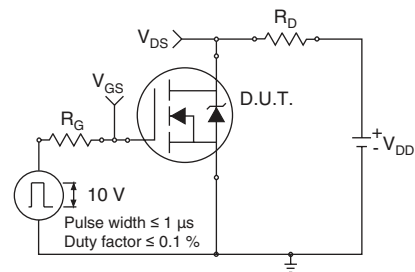
91038\_09

**Fig. 9 - Maximum Drain Current vs. Case Temperature**

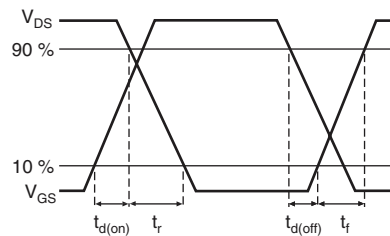


91038\_08

**Fig. 8 - Maximum Safe Operating Area**



**Fig. 10a - Switching Time Test Circuit**



**Fig. 10b - Switching Time Waveforms**

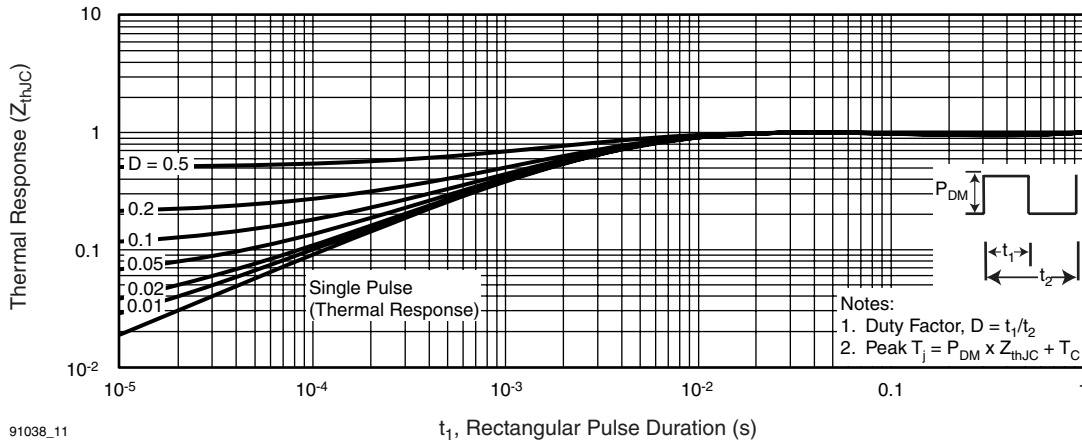


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

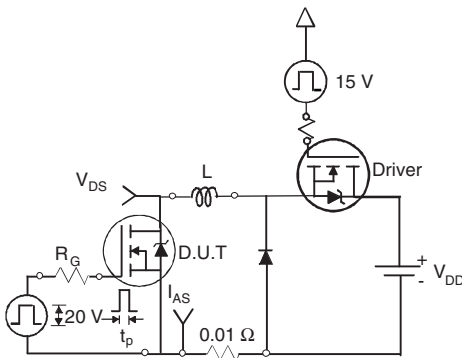


Fig. 12a - Unclamped Inductive Test Circuit

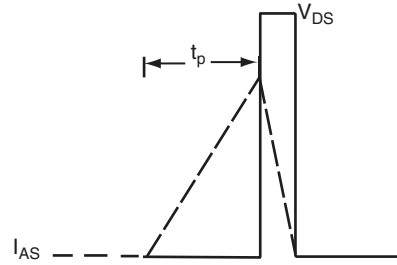


Fig. 12b - Unclamped Inductive Waveforms

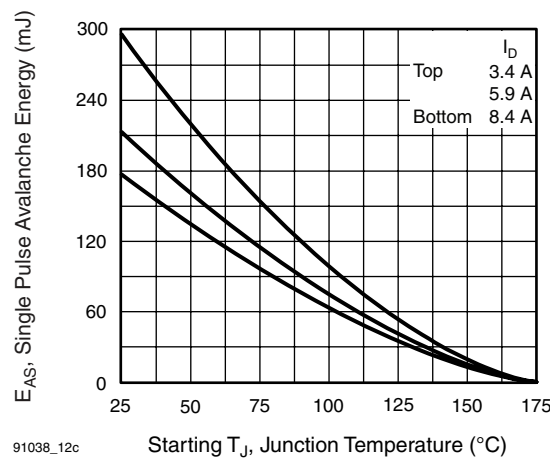


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

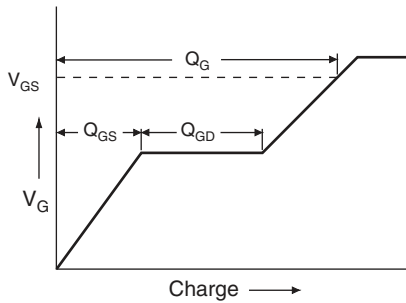


Fig. 13a - Basic Gate Charge Waveform

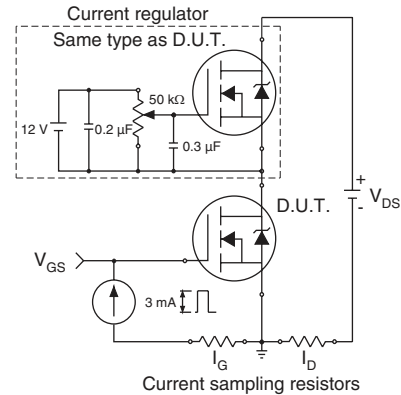
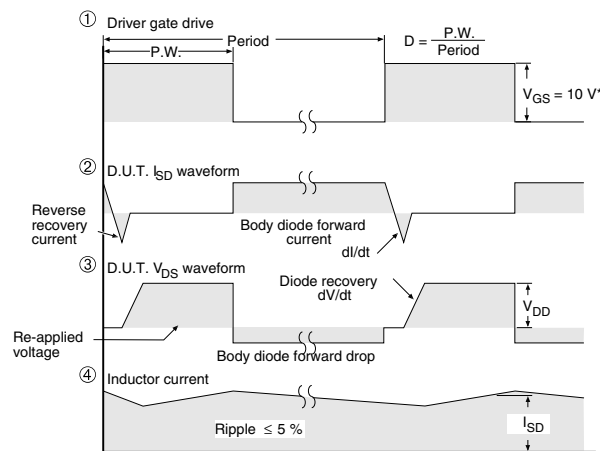
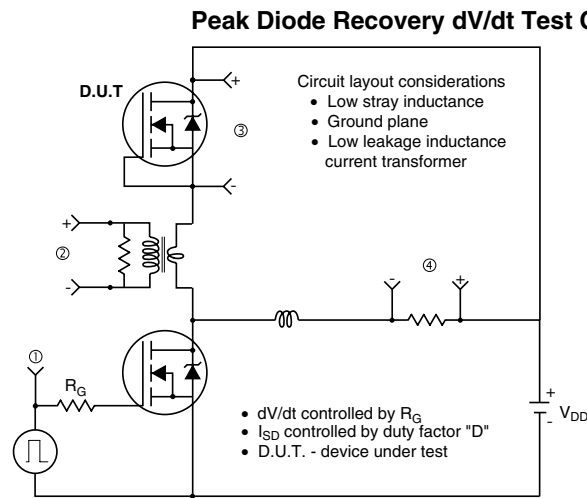


Fig. 13b - Gate Charge Test Circuit



\*  $V_{GS} = 5\text{ V}$  for logic level devices and  $3\text{ V}$  drive devices

Fig. 14 - For N-Channel

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see [www.vishay.com/ppg?91038](http://www.vishay.com/ppg?91038).



## Disclaimer

All product specifications and data are subject to change without notice.

Vishay Intertechnology, Inc., its affiliates, agents, and employees, and all persons acting on its or their behalf (collectively, "Vishay"), disclaim any and all liability for any errors, inaccuracies or incompleteness contained herein or in any other disclosure relating to any product.

Vishay disclaims any and all liability arising out of the use or application of any product described herein or of any information provided herein to the maximum extent permitted by law. The product specifications do not expand or otherwise modify Vishay's terms and conditions of purchase, including but not limited to the warranty expressed therein, which apply to these products.

No license, express or implied, by estoppel or otherwise, to any intellectual property rights is granted by this document or by any conduct of Vishay.

The products shown herein are not designed for use in medical, life-saving, or life-sustaining applications unless otherwise expressly indicated. Customers using or selling Vishay products not expressly indicated for use in such applications do so entirely at their own risk and agree to fully indemnify Vishay for any damages arising or resulting from such use or sale. Please contact authorized Vishay personnel to obtain written terms and conditions regarding products designed for such applications.

Product names and markings noted herein may be trademarks of their respective owners.

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

 [View IRF644NS on WIN SOURCE](#)

 [Vishay Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management