



# THE DATASHEET OF IRF4104GPBF



# IRF4104GPbF

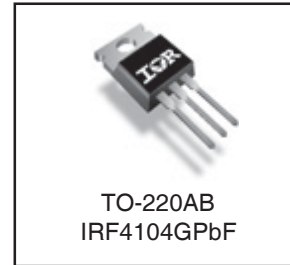
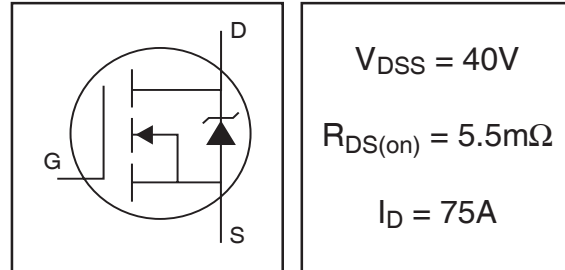
HEXFET® Power MOSFET

## Features

- Advanced Process Technology
- Ultra Low On-Resistance
- 175°C Operating Temperature
- Fast Switching
- Repetitive Avalanche Allowed up to Tjmax
- Lead-Free
- Halogen-Free

## Description

This HEXFET® Power MOSFET utilizes the latest processing techniques to achieve extremely low on-resistance per silicon area. Additional features of this design are a 175°C junction operating temperature, fast switching speed and improved repetitive avalanche rating. These features combine to make this design an extremely efficient and reliable device for use in a wide variety of applications.



## Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Silicon Limited)	120	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	84	
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$ (Package limited)	75	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	470	
$P_D @ T_C = 25^\circ C$	Power Dissipation	140	W
	Linear Derating Factor	0.95	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
$E_{AS}$ (Thermally limited)	Single Pulse Avalanche Energy <sup>②</sup>	120	mJ
$E_{AS}$ (Tested)	Single Pulse Avalanche Energy Tested Value <sup>③</sup>	220	
$I_{AR}$	Avalanche Current <sup>①</sup>	See Fig.12a, 12b, 15, 16	A
$E_{AR}$	Repetitive Avalanche Energy <sup>②</sup>		mJ
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to + 175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting Torque, 6-32 or M3 screw <sup>④</sup>	10 lbf*in (1.1N*m)	

## Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	1.05	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat Greased Surface <sup>⑤</sup>	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient <sup>⑥</sup>	—	62	

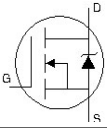
# IRF4104GPbF

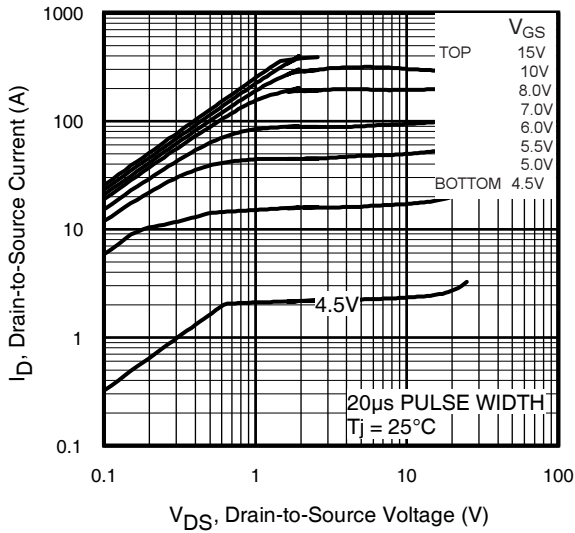
International  
**IR** Rectifier

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

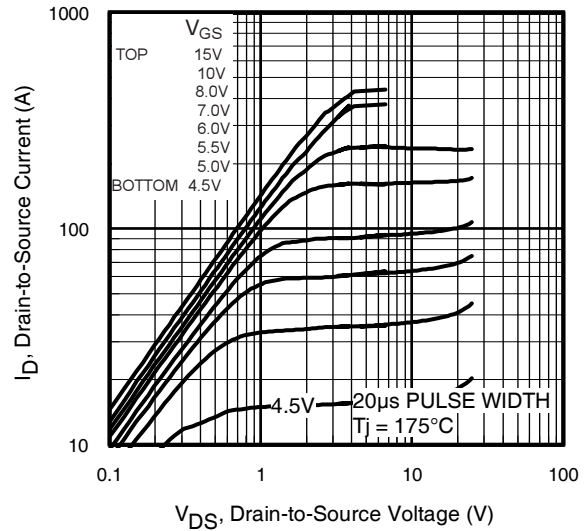
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	40	—	—	V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	0.032	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = 1\text{mA}$
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	—	4.3	5.5	m $\Omega$	$V_{GS} = 10V, I_D = 75A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	2.0	—	4.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
$g_{fs}$	Forward Transconductance	63	—	—	V	$V_{DS} = 10V, I_D = 75A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	20	$\mu A$	$V_{DS} = 40V, V_{GS} = 0V$
		—	—	250		$V_{DS} = 40V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	200	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage	—	—	-200		$V_{GS} = -20V$
$Q_g$	Total Gate Charge	—	68	100		$I_D = 75A$
$Q_{gs}$	Gate-to-Source Charge	—	21	—	nC	$V_{DS} = 32V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	27	—		$V_{GS} = 10V$ ③
$t_{d(on)}$	Turn-On Delay Time	—	16	—		$V_{DD} = 20V$
$t_r$	Rise Time	—	130	—		$I_D = 75A$
$t_{d(off)}$	Turn-Off Delay Time	—	38	—	ns	$R_G = 6.8\ \Omega$
$t_f$	Fall Time	—	77	—		$V_{GS} = 10V$ ③
$L_D$	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
$L_S$	Internal Source Inductance	—	7.5	—		
$C_{iss}$	Input Capacitance	—	3000	—		$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	660	—		$V_{DS} = 25V$
$C_{riss}$	Reverse Transfer Capacitance	—	380	—	pF	$f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	2160	—		$V_{GS} = 0V, V_{DS} = 1.0V, f = 1.0\text{MHz}$
$C_{oss}$	Output Capacitance	—	560	—		$V_{GS} = 0V, V_{DS} = 32V, f = 1.0\text{MHz}$
$C_{oss\ eff.}$	Effective Output Capacitance	—	850	—		$V_{GS} = 0V, V_{DS} = 0V\ \text{to}\ 32V$ ④

## Source-Drain Ratings and Characteristics

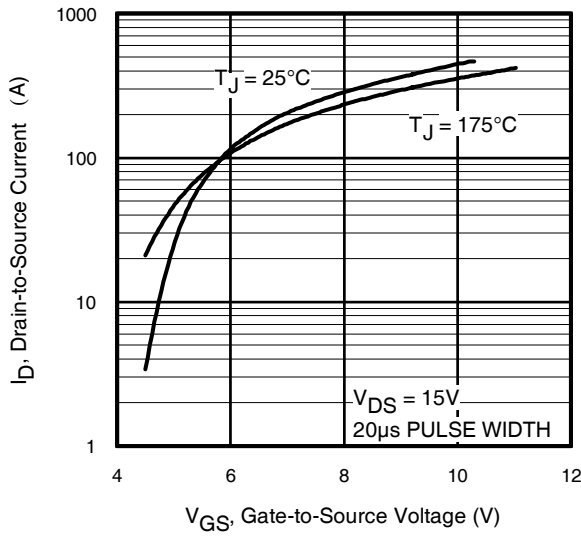
	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	75	A	MOSFET symbol showing the integral reverse p-n junction diode.
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	470		
$V_{SD}$	Diode Forward Voltage	—	—	1.3	V	$T_J = 25^\circ\text{C}, I_S = 75A, V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	23	35	ns	$T_J = 25^\circ\text{C}, I_F = 75A, V_{DD} = 20V$
$Q_{rr}$	Reverse Recovery Charge	—	6.8	10	nC	$di/dt = 100A/\mu s$ ③
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S+L_D$ )				



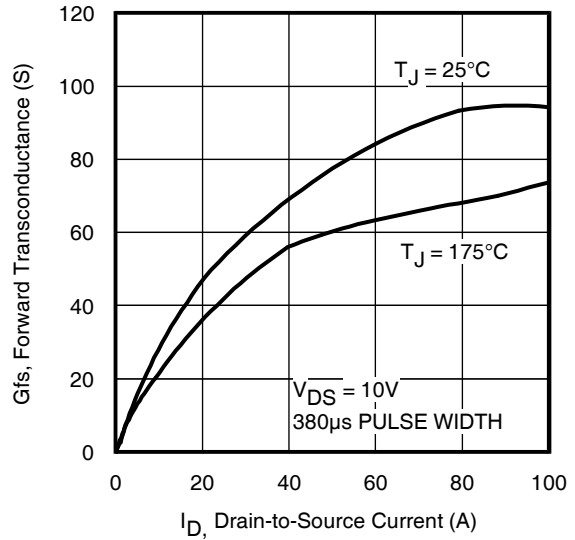
**Fig 1.** Typical Output Characteristics



**Fig 2.** Typical Output Characteristics

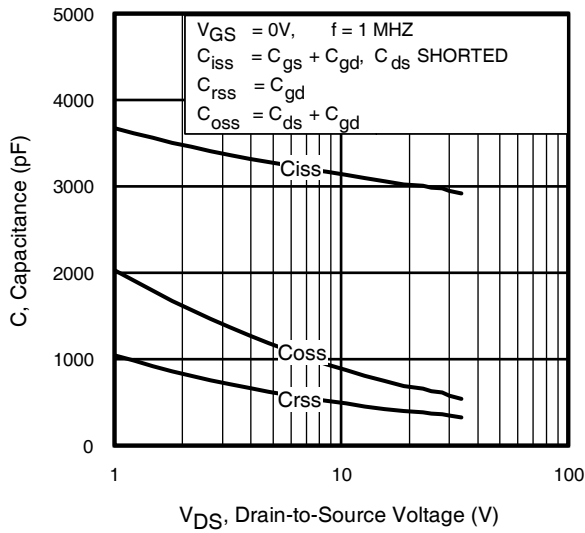


**Fig 3.** Typical Transfer Characteristics

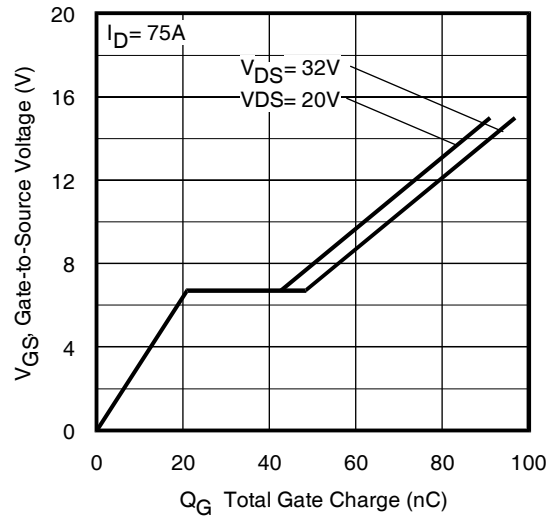


**Fig 4.** Typical Forward Transconductance Vs. Drain Current

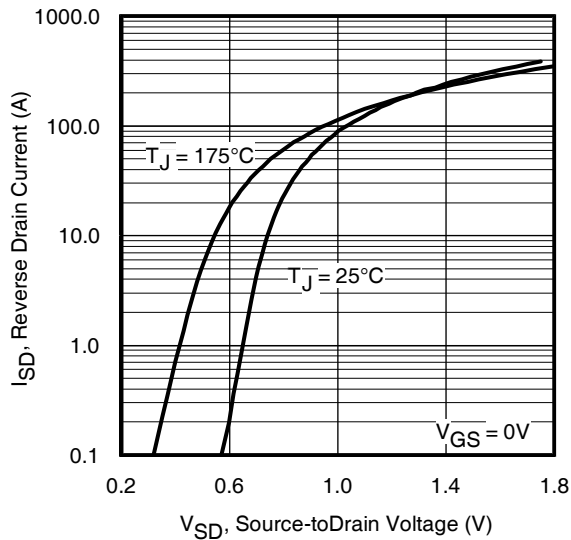
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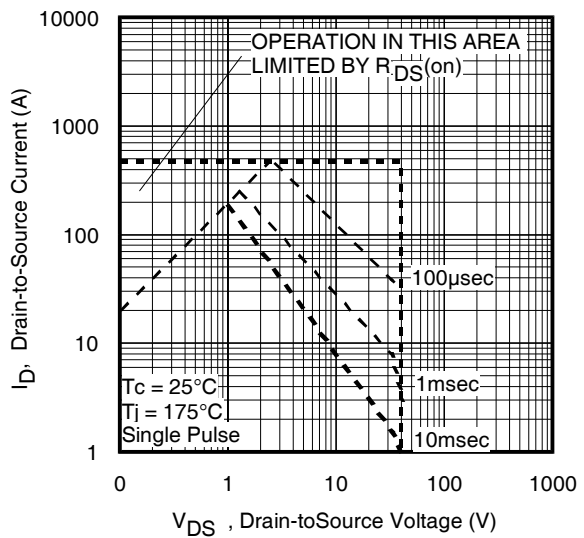
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



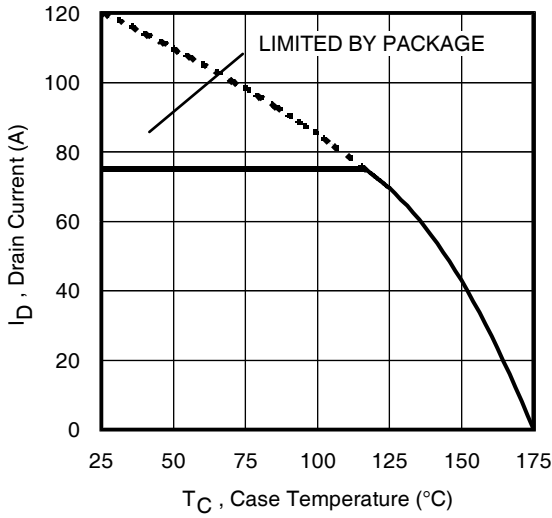
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



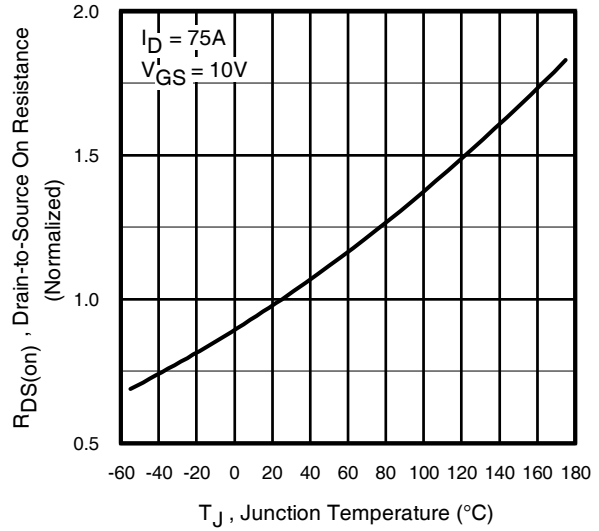
**Fig 7.** Typical Source-Drain Diode Forward Voltage



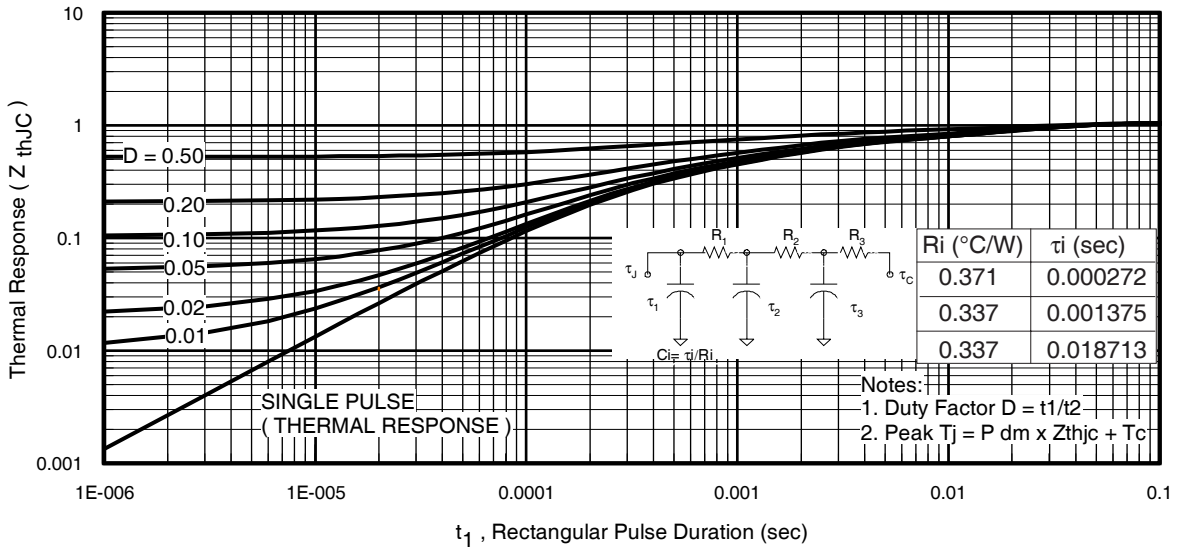
**Fig 8.** Maximum Safe Operating Area



**Fig 9.** Maximum Drain Current Vs. Case Temperature



**Fig 10.** Normalized On-Resistance Vs. Temperature



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Case

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**Fig 12a.** Unclamped Inductive Test Circuit



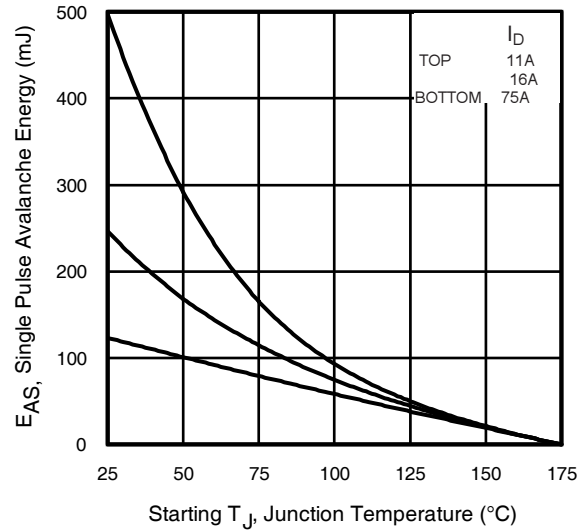
**Fig 12b.** Unclamped Inductive Waveforms



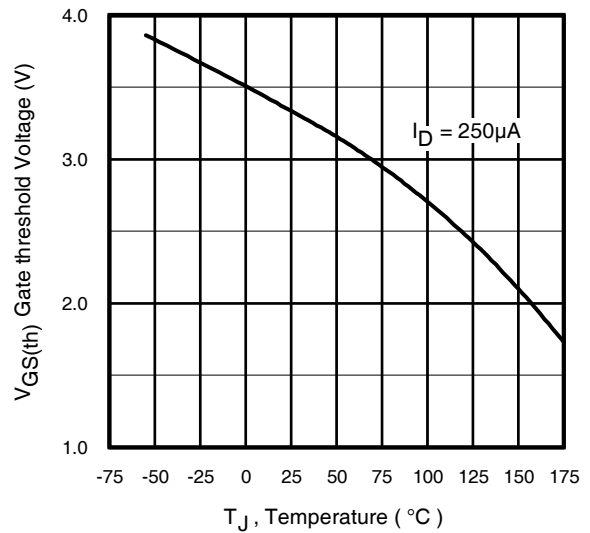
**Fig 13a.** Basic Gate Charge Waveform



**Fig 13b.** Gate Charge Test Circuit



**Fig 12c.** Maximum Avalanche Energy Vs. Drain Current



**Fig 14.** Threshold Voltage Vs. Temperature

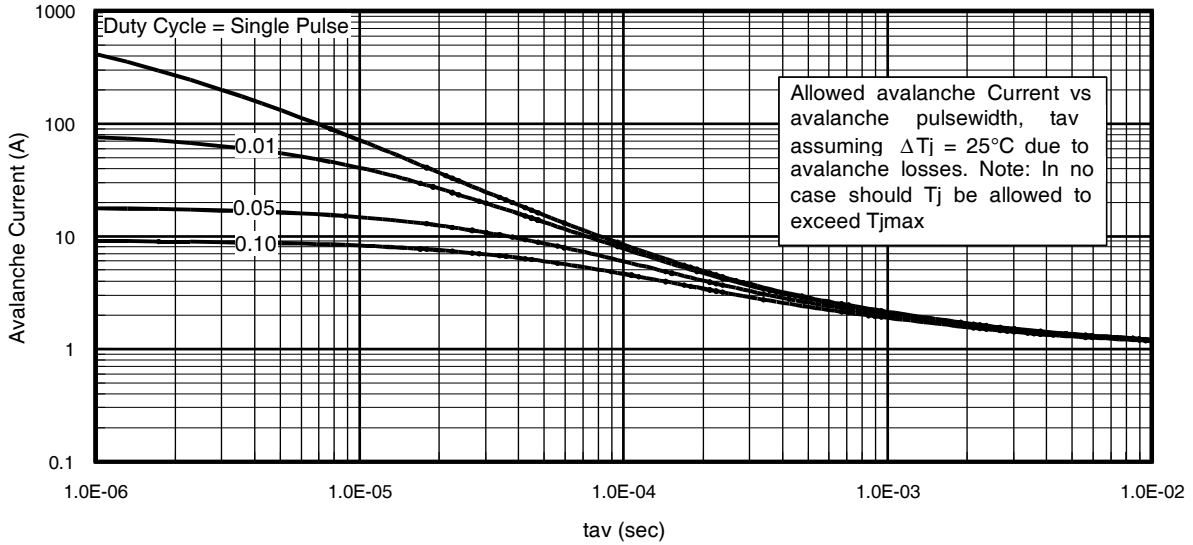


Fig 15. Typical Avalanche Current Vs.Pulsewidth

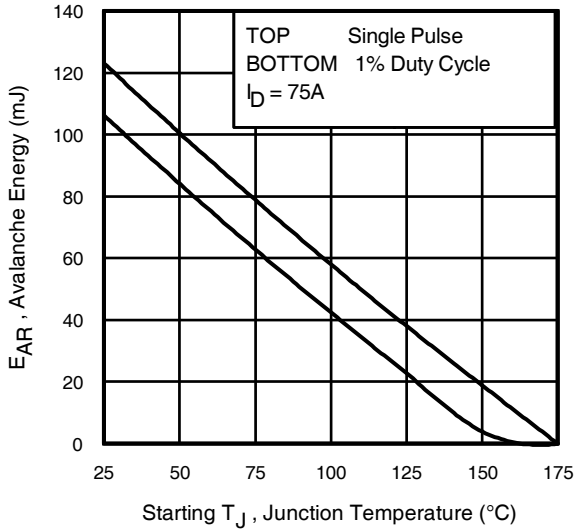


Fig 16. Maximum Avalanche Energy Vs. Temperature

**Notes on Repetitive Avalanche Curves , Figures 15, 16: (For further info, see AN-1005 at www.irf.com)**

1. Avalanche failures assumption: Purely a thermal phenomenon and failure occurs at a temperature far in excess of  $T_{jmax}$ . This is validated for every part type.
2. Safe operation in Avalanche is allowed as long as  $T_{jmax}$  is not exceeded.
3. Equation below based on circuit and waveforms shown in Figures 12a, 12b.
4.  $P_{D(ave)}$  = Average power dissipation per single avalanche pulse.
5.  $BV$  = Rated breakdown voltage (1.3 factor accounts for voltage increase during avalanche).
6.  $I_{av}$  = Allowable avalanche current.
7.  $\Delta T$  = Allowable rise in junction temperature, not to exceed  $T_{jmax}$  (assumed as 25°C in Figure 15, 16).  
 $t_{av}$  = Average time in avalanche.  
 $D$  = Duty cycle in avalanche =  $t_{av} \cdot f$   
 $Z_{thJC}(D, t_{av})$  = Transient thermal resistance, see figure 11)

$$P_{D(ave)} = 1/2 ( 1.3 \cdot BV \cdot I_{av} ) = \Delta T / Z_{thJC}$$

$$I_{av} = 2\Delta T / [1.3 \cdot BV \cdot Z_{th}]$$

$$E_{AS(AR)} = P_{D(ave)} \cdot t_{av}$$



**Fig 17. Peak Diode Recovery  $dv/dt$  Test Circuit for N-Channel HEXFET® Power MOSFETs**



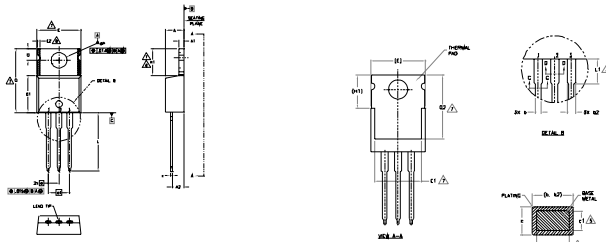
**Fig 18a. Switching Time Test Circuit**



**Fig 18b. Switching Time Waveforms**

## TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



- NOTES
- 1 - DIMENSIONS AND TOLERANCING AS PER ASME Y14.5 M - 1994.
  - 2 - DIMENSIONS ARE SHOWN IN INCHES (MILLIMETERS).
  - 3 - LEAD DIMENSION AND FINISH UNCONTROLLED IN L1.
  - 4 - DIMENSION D, D1 & E DO NOT INCLUDE MOLD FLASH; MOLD FLASH SHALL NOT EXCEED .002" (0.077) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMITY OF THE PLASTIC BODY.
  - 5 - DIMENSION D1, S3 & c1 APPLY TO BASE METAL ONLY.
  - 6 - CONTROLLING DIMENSION - INCHES.
  - 7 - THERMAL PAD CONTOUR OPTIONAL. OTHER DIMENSIONS EXH103 & E1.
  - 8 - DIMENSION E2 X H IDENTIFY A ZONE WHERE STAMPING AND SIMULATION FERRULES ARE ALLOWED.
  - 9 - OUTLINE CONFORMS TO JEDEC TO-220 EXCEPT A2 (MIN.) AND D2 (MAX.) WHERE DIMENSIONS ARE DERIVED FROM THE ACTUAL PACKAGE OUTLINE.

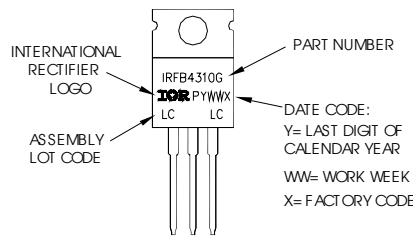
SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
A	3.56	4.83	140	190	
A1	0.51	1.40	020	.055	
A2	2.03	2.92	080	.115	
B	0.38	1.01	.015	.040	
b1	0.38	0.97	.015	.038	5
b2	1.14	1.78	.045	.070	
b3	1.14	1.73	.045	.068	
c	0.36	0.61	.014	.024	5
c1	0.36	0.56	.014	.022	5
D	14.22	16.51	560	650	4
D1	8.59	9.02	330	355	
D2	11.68	12.88	460	507	7
E	9.65	10.67	380	420	4,7
E1	6.89	8.89	270	350	7
E2	-	0.76	-	.030	8
φ	7.50 BSC	-	290 BSC	-	
e1	5.08 BSC	-	200 BSC	-	
H	5.84	6.86	230	270	7,8
L	12.70	14.73	500	580	
L1	3.56	4.06	140	160	3
φP	3.54	4.08	139	161	
D	2.54	3.42	100	135	

- LEAD FINISHES
- 1 - GALT
  - 2 - SOLDER
  - 3 - TINNED
  - 4 - NONE
- SEMI-CONDUCTOR
- 1 - GALT
  - 2 - SOLDER
  - 3 - TINNED
  - 4 - NONE

## TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRFB4310GPBF

- Note: "G" suffix in part number indicates "Halogen - Free"
- Note: "P" in ass embly line position indicates "Lead - Free"



TO-220AB package is not recommended for Surface Mount Application

### Notes:

1. For an Automotive Qualified version of this part please see <http://www.irf.com/product-info/datasheets/data/auirf4104.pdf>
2. For the most current drawing please refer to IR website at <http://www.irf.com/package/>

### Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11).
- ② Limited by  $T_{Jmax}$ , starting  $T_J = 25^\circ C$ ,  $L = 0.04mH$   
 $R_G = 25\Omega$ ,  $I_{AS} = 75A$ ,  $V_{GS} = 10V$ . Part not recommended for use above this value.
- ③ Pulse width  $\leq 1.0ms$ ; duty cycle  $\leq 2\%$ .
- ④  $C_{OSS}$  eff. is a fixed capacitance that gives the same charging time as  $C_{OSS}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .
- ⑤ Limited by  $T_{Jmax}$ , see Fig.12a, 12b, 15, 16 for typical repetitive avalanche performance.
- ⑥ This value determined from sample failure population. 100% tested to this value in production.
- ⑦ This is only applied to TO-220AB package.

Data and specifications subject to change without notice.  
This product has been designed and qualified for the Industrial market.  
Qualification Standards can be found on IR's Web site.

## Looking for pricing, stock, or lifecycle information?

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 [Infineon Technologies](#) Information

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