



**THE DATASHEET OF
SUD50N04-37P-T4-E3**





N-Channel 40-V (D-S) MOSFET

PRODUCT SUMMARY			
V _{DS} (V)	r _{DS(on)} (Ω)	I _D (A) ^a	Q _g (Typ.)
40	0.037 at V _{GS} = 10 V	8	5.3 nC
	0.046 at V _{GS} = 4.5 V	8	

FEATURES

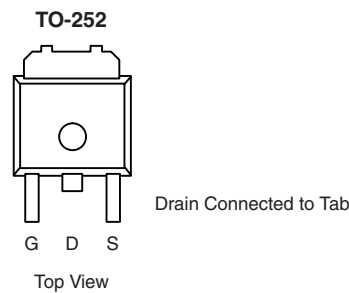
- TrenchFET[®] Power MOSFET
- 100 % UIS Tested



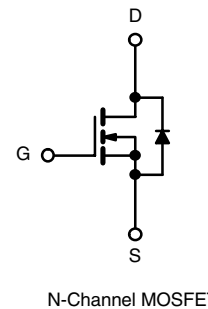
RoHS COMPLIANT

APPLICATIONS

- Backlight Inverter for LCD Display
- Full Bridge DC/DC Converter



Ordering Information:
SUD50N04-37P-E3 (Lead (Pb)-free)



ABSOLUTE MAXIMUM RATINGS T _A = 25 °C, unless otherwise noted				
Parameter	Symbol	Limit	Unit	
Drain-Source Voltage	V _{DS}	40	V	
Gate-Source Voltage	V _{GS}	± 20		
Continuous Drain Current (T _J = 150 °C)	I _D	T _C = 25 °C	8 ^a	A
		T _C = 70 °C	8 ^a	
		T _A = 25 °C	5.4 ^b	
		T _A = 70 °C	4.4 ^b	
Pulsed Drain Current	I _{DM}	30		
Continuous Source-Drain Diode Current	I _S	T _C = 25 °C	8 ^a	
		T _A = 25 °C	1.6 ^b	
Single Pulse Avalanche Current	I _{AS}	7		
Avalanche Energy	E _{AS}	2.45	mJ	
Maximum Power Dissipation	P _D	T _C = 25 °C	10.8	W
		T _C = 70 °C	6.9	
		T _A = 25 °C	2.0 ^b	
		T _A = 70 °C	1.3 ^b	
Operating Junction and Storage Temperature Range	T _J , T _{stg}	- 55 to 150	°C	

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Maximum Junction-to-Ambient ^b	R _{thJA}	49	60	°C/W	
Maximum Junction-to-Case	R _{thJC}	9.4	11.5		

Notes:

a. Package limited.

b. Surface mounted on 1" x 1" FR4 board.

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$, unless otherwise noted						
Parameter	Symbol	Test Conditions	Min.	Typ.	Max.	Unit
Static						
Drain-Source Breakdown Voltage	V_{DS}	$V_{GS} = 0\text{ V}, I_D = 1\text{ mA}$	40			V
V_{DS} Temperature Coefficient	$\Delta V_{DS}/T_J$	$I_D = 250\text{ }\mu\text{A}$		44		mV/ $^\circ\text{C}$
$V_{GS(th)}$ Temperature Coefficient	$\Delta V_{GS(th)}/T_J$			- 5.5		
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	1.4		2.5	V
Gate-Source Leakage	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}$			1	μA
		$V_{DS} = 40\text{ V}, V_{GS} = 0\text{ V}, T_J = 70\text{ }^\circ\text{C}$			20	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} \geq 5\text{ V}, V_{GS} = 10\text{ V}$	10			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		0.0305	0.037	Ω
		$V_{GS} = 4.5\text{ V}, I_D = 4\text{ A}$		0.037	0.046	
Forward Transconductance ^a	g_{fs}	$V_{DS} = 15\text{ V}, I_D = 5\text{ A}$		22		S
Dynamic^b						
Input Capacitance	C_{iss}	$V_{DS} = 20\text{ V}, V_{GS} = 0\text{ V}, f = 1\text{ MHz}$		640		pF
Output Capacitance	C_{oss}			73		
Reverse Transfer Capacitance	C_{rss}			41		
Total Gate Charge	Q_g	$V_{DS} = 20\text{ V}, V_{GS} = 10\text{ V}, I_D = 5\text{ A}$		11.7	20	nC
			$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$		5.3	
Gate-Source Charge	Q_{gs}	$V_{DS} = 20\text{ V}, V_{GS} = 4.5\text{ V}, I_D = 5\text{ A}$		1.9		nC
Gate-Drain Charge	Q_{gd}			1.7		
Gate Resistance	R_g		$f = 1\text{ MHz}$		2.2	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 4.5\text{ V}, R_g = 1\text{ }\Omega$		18	30	ns
Rise Time	t_r			14	25	
Turn-Off Delay Time	$t_{d(off)}$			14	25	
Fall Time	t_f			10	20	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 20\text{ V}, R_L = 4\text{ }\Omega$ $I_D \cong 5\text{ A}, V_{GEN} = 10\text{ V}, R_g = 1\text{ }\Omega$		9	18	ns
Rise Time	t_r			11	20	
Turn-Off Delay Time	$t_{d(off)}$			14	25	
Fall Time	t_f			8	18	
Drain-Source Body Diode Characteristics						
Continuous Source-Drain Diode Current	I_S	$T_C = 25\text{ }^\circ\text{C}$			8	A
Pulse Diode Forward Current ^a	I_{SM}				30	
Body Diode Voltage	V_{SD}	$I_S = 2\text{ A}$		0.805	1.2	V
Body Diode Reverse Recovery Time	t_{rr}	$I_F = 2\text{ A}, di/dt = 100\text{ A}/\mu\text{s}, T_J = 25\text{ }^\circ\text{C}$		19	30	ns
Body Diode Reverse Recovery Charge	Q_{rr}			14	25	nC
Reverse Recovery Fall Time	t_a			13		ns
Reverse Recovery Rise Time	t_b			6		

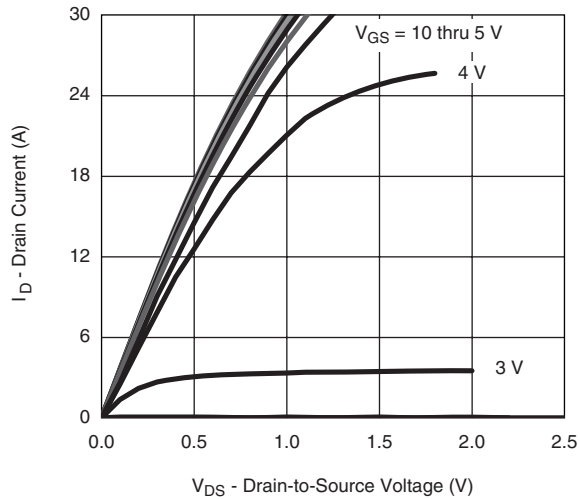
Notes:

- a. Pulse test; pulse width $\leq 300\text{ }\mu\text{s}$, duty cycle $\leq 2\%$.
b. Guaranteed by design, not subject to production testing.

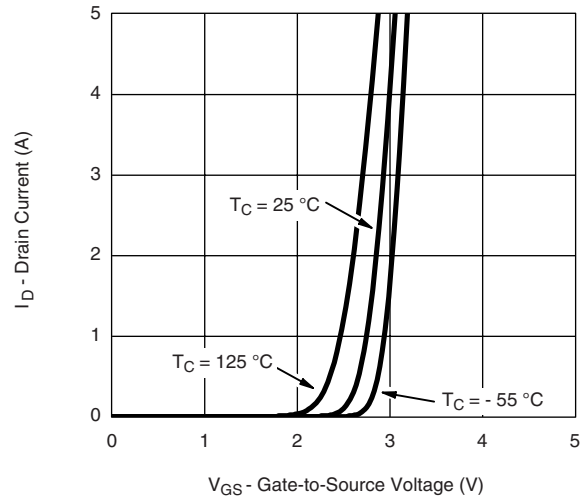
Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.



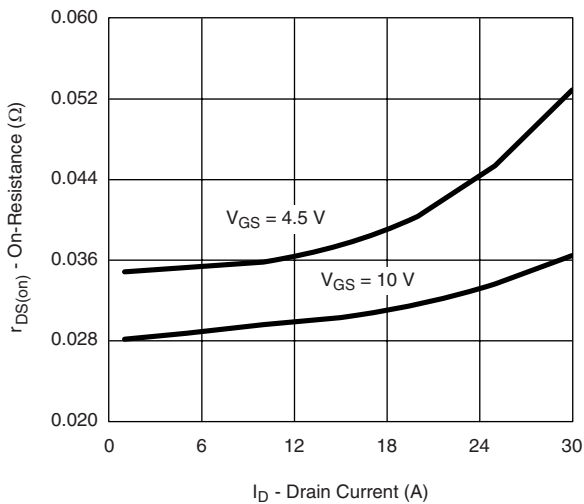
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



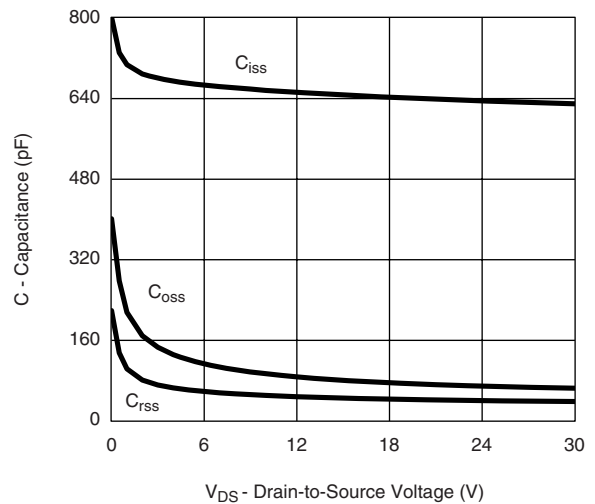
Output Characteristics



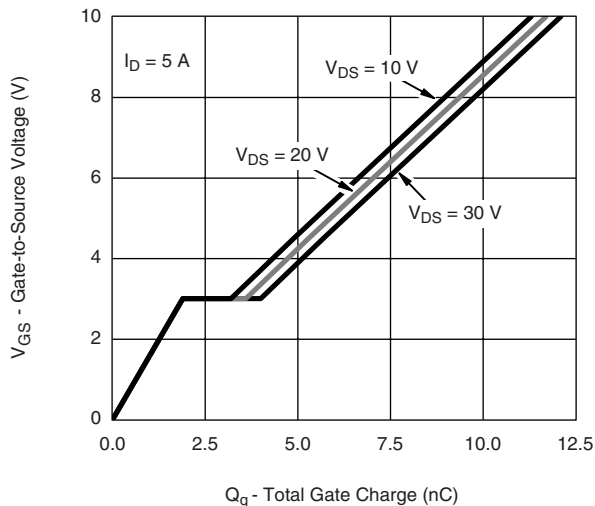
Transfer Characteristics



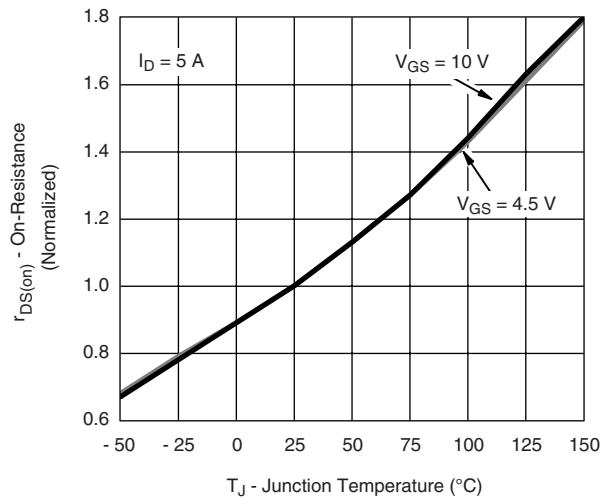
On-Resistance vs. Drain Current



Capacitance



Gate Charge



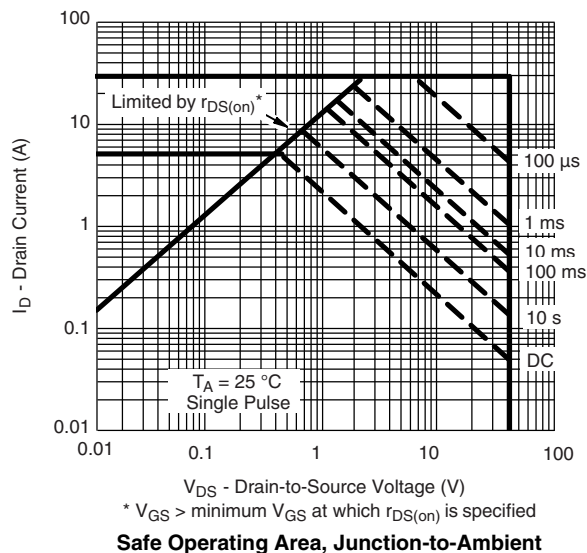
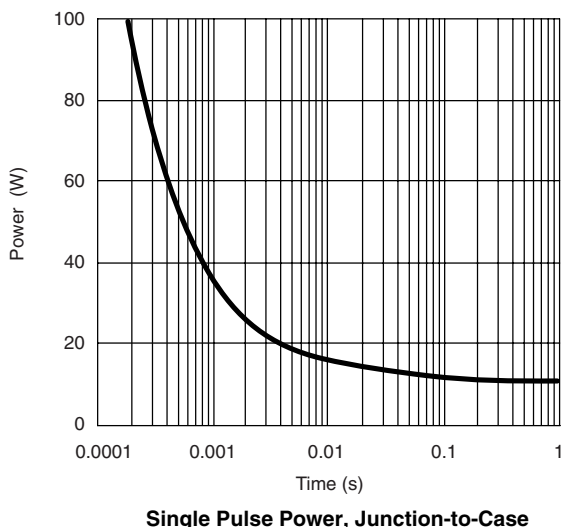
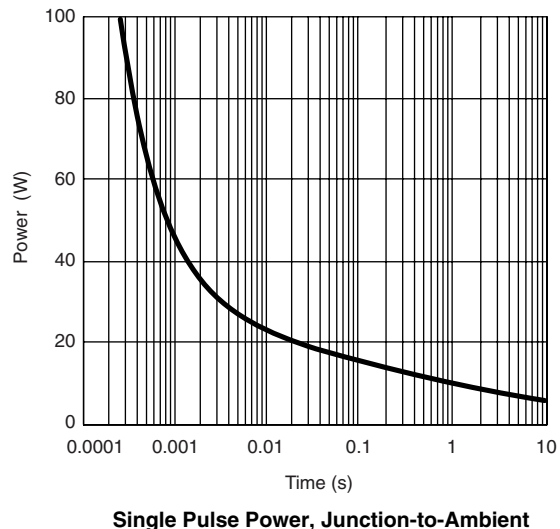
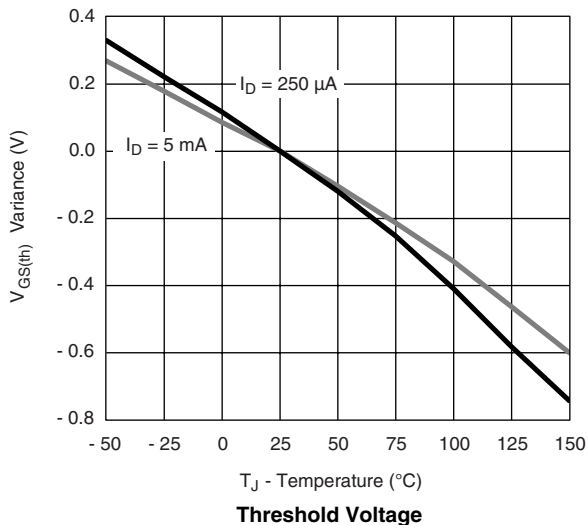
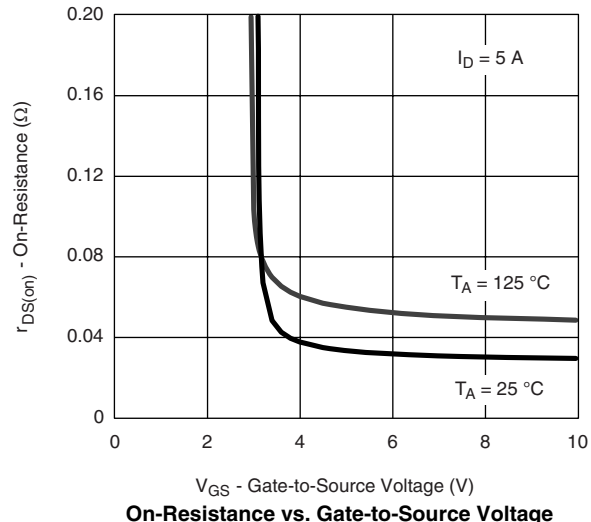
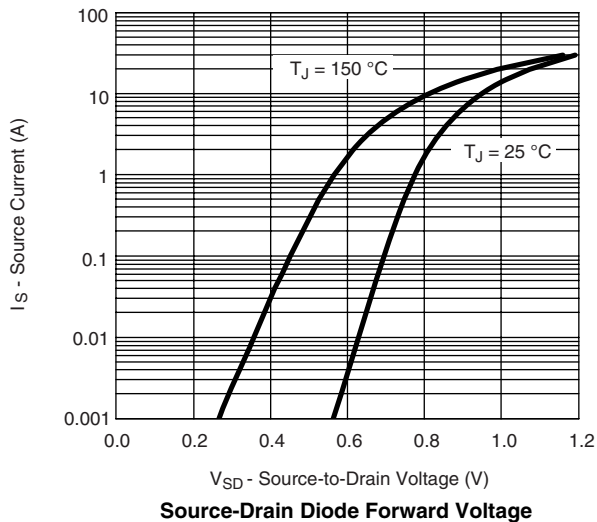
On-Resistance vs. Junction Temperature

SUD50N04-37P



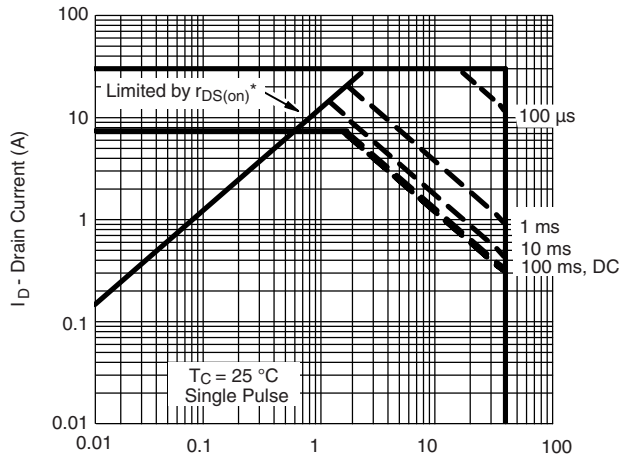
Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted

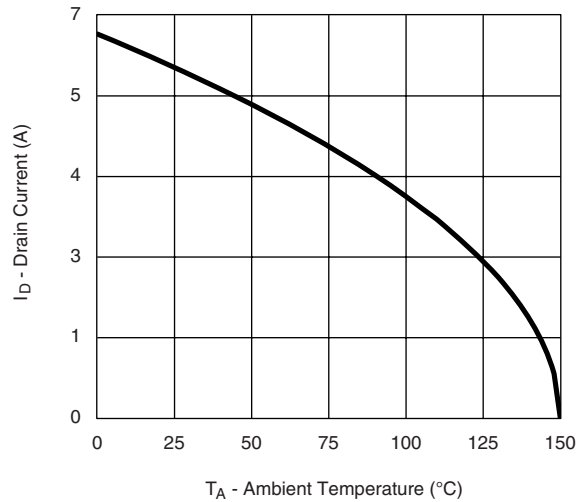




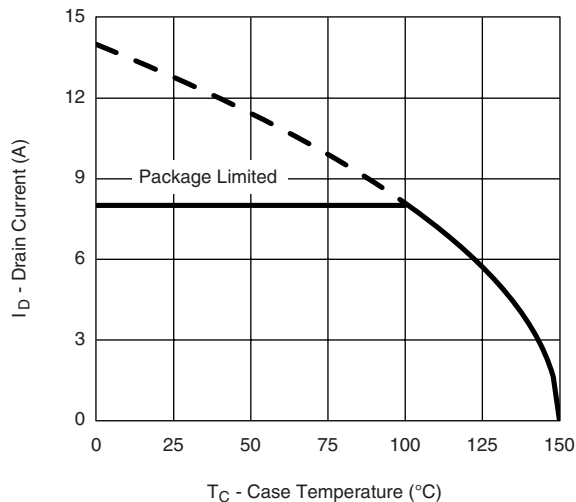
TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



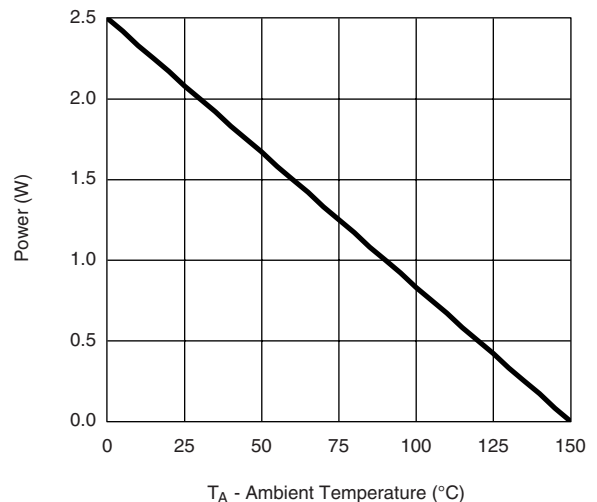
V_{DS} - Drain-to-Source Voltage (V)
 * $V_{GS} >$ minimum V_{GS} at which $r_{DS(on)}$ is specified
Safe Operating Area, Junction-to-Case



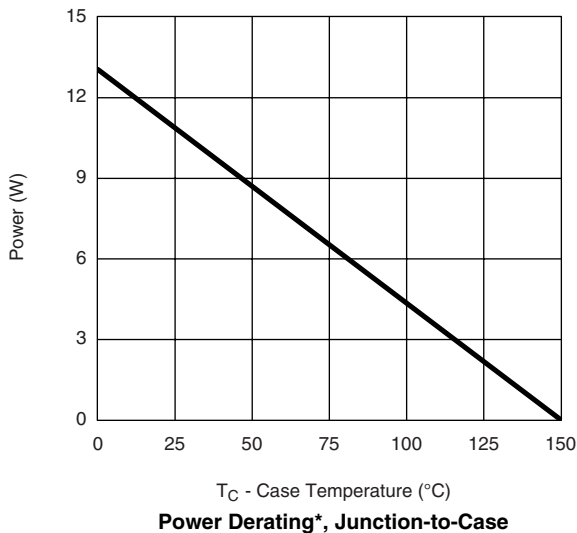
T_A - Ambient Temperature ($^\circ\text{C}$)
Current Derating*, Junction-to-Ambient



T_C - Case Temperature ($^\circ\text{C}$)
Current Derating*, Junction-to-Case



T_A - Ambient Temperature ($^\circ\text{C}$)
Power Derating*, Junction-to-Ambient



T_C - Case Temperature ($^\circ\text{C}$)
Power Derating*, Junction-to-Case

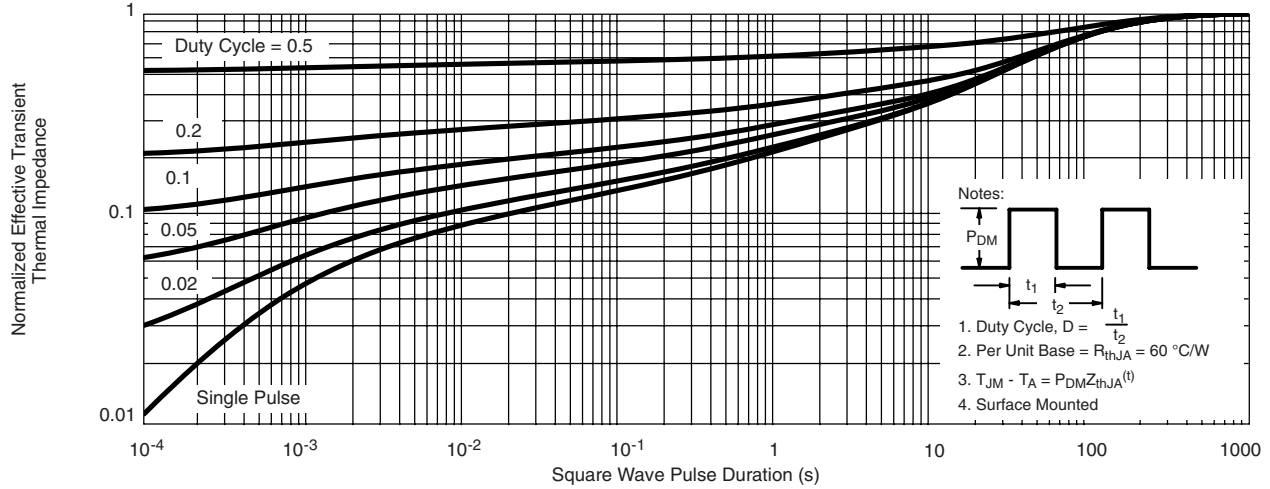
* The power dissipation P_D is based on $T_{J(max)} = 175^\circ\text{C}$, using junction-to-case thermal resistance, and is more useful in settling the upper dissipation limit for cases where additional heatsinking is used. It is used to determine the current rating, when this rating falls below the package limit.

SUD50N04-37P

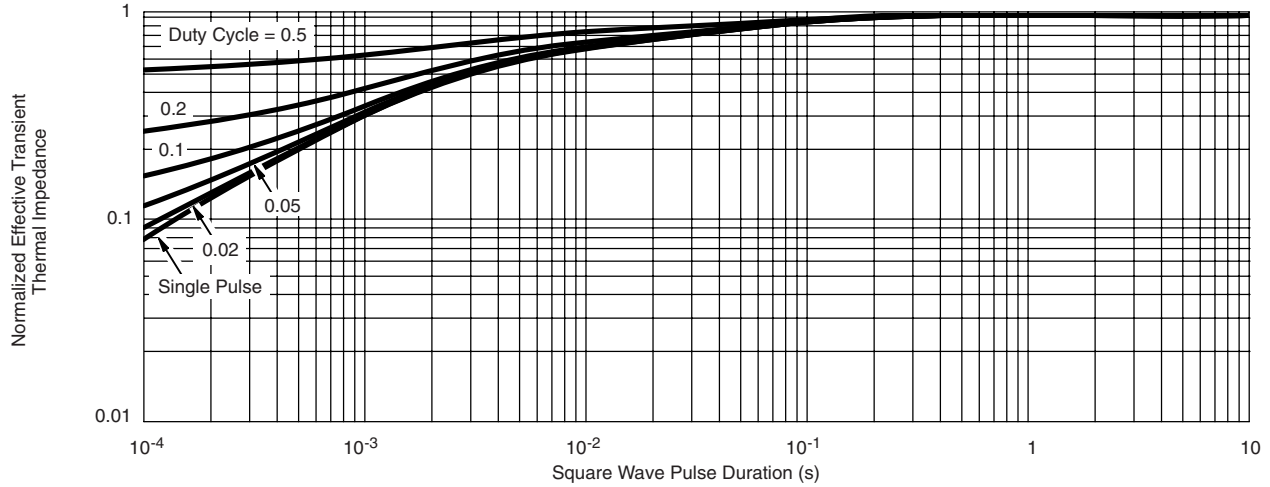


Vishay Siliconix

TYPICAL CHARACTERISTICS 25 °C, unless otherwise noted



Normalized Thermal Transient Impedance, Junction-to-Ambient



Normalized Thermal Transient Impedance, Junction-to-Case

Vishay Siliconix maintains worldwide manufacturing capability. Products may be manufactured at one of several qualified locations. Reliability data for Silicon Technology and Package Reliability represent a composite of all qualified locations. For related documents such as package/tape drawings, part marking, and reliability data, see <http://www.vishay.com/ppg?69732>.



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