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# FCP4N60

## N-Channel SuperFET® MOSFET

600 V, 3.9 A, 1.2 Ω

### Features

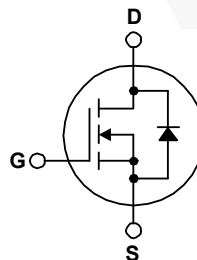
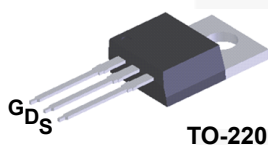
- 650 V @  $T_J = 150^\circ\text{C}$
- Typ.  $R_{DS(on)} = 1.0 \Omega$
- Ultra Low Gate Charge (Typ.  $Q_g = 12.8 \text{ nC}$ )
- Low Effective Output Capacitance (Typ.  $C_{oss(eff.)} = 32 \text{ pF}$ )
- 100% Avalanche Tested
- RoHS Compliant

### Application

- LCD / LED / PDP TV and Monitor Lighting
- Solar Inverter
- AC-DC Power Supply

### Description

SuperFET® MOSFET is Fairchild Semiconductor's first generation of high voltage super-junction (SJ) MOSFET family that is utilizing charge balance technology for outstanding low on-resistance and lower gate charge performance. This technology is tailored to minimize conduction loss, provide superior switching performance,  $dv/dt$  rate and higher avalanche energy. Consequently, SuperFET MOSFET is very suitable for the switching power applications such as PFC, server/telecom power, FPD TV power, ATX power and industrial power applications.



### MOSFET Maximum Ratings $T_C = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	FCP4N60	Unit
$V_{DSS}$	Drain-Source Voltage	600	V
$I_D$	Drain Current - Continuous ( $T_C = 25^\circ\text{C}$ ) - Continuous ( $T_C = 100^\circ\text{C}$ )	3.9 2.5	A A
$I_{DM}$	Drain Current - Pulsed (Note 1)	11.7	A
$V_{GSS}$	Gate-Source voltage	$\pm 30$	V
$E_{AS}$	Single Pulsed Avalanche Energy (Note 2)	128	mJ
$I_{AR}$	Avalanche Current (Note 1)	3.9	A
$E_{AR}$	Repetitive Avalanche Energy (Note 1)	5.0	mJ
$dv/dt$	Peak Diode Recovery $dv/dt$ (Note 3)	4.5	V/ns
$P_D$	Power Dissipation ( $T_C = 25^\circ\text{C}$ ) - Derate Above $25^\circ\text{C}$	50 0.4	W W/ $^\circ\text{C}$
$T_J, T_{STG}$	Operating and Storage Temperature Range	-55 to +150	$^\circ\text{C}$
$T_L$	Maximum Lead Temperature for Soldering, 1/8" from Case for 5 Seconds.	300	$^\circ\text{C}$

### Thermal Characteristics

Symbol	Parameter	FCP4N60	Unit
$R_{\theta JC}$	Thermal Resistance, Junction to Case, Max.	2.5	$^\circ\text{C/W}$
	Thermal Resistance, Junction to Ambient, Max.	83	

$R_{\theta JA}$

## Package Marking and Ordering Information

Part Number	Top Mark	Package	Packing Method	Reel Size	Tape Width	Quantity
FCP4N60	FCP4N60	TO-220	Tube	N/A	N/A	50 units

## Electrical Characteristics $T_C = 25^\circ\text{C}$ unless otherwise noted.

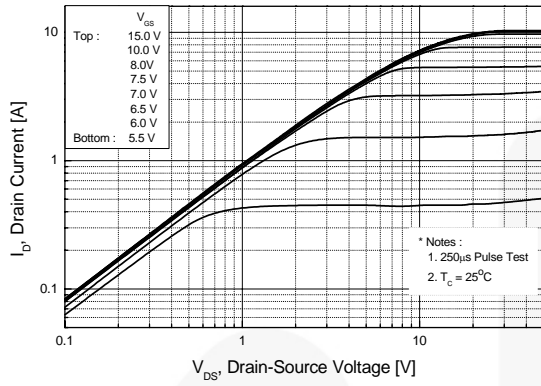
Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
<b>Off Characteristics</b>						
BV <sub>DSS</sub>	Drain-Source Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_J = 25^\circ\text{C}$	600	--	--	V
		$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}, T_J = 150^\circ\text{C}$	--	650	--	V
$\Delta BV_{DSS} / \Delta T_J$	Breakdown Voltage Temperature Coefficient	$I_D = 250\ \mu\text{A}$ , Referenced to $25^\circ\text{C}$	--	0.6	--	V/ $^\circ\text{C}$
BV <sub>DS</sub>	Drain-Source Avalanche Breakdown Voltage	$V_{GS} = 0\text{ V}, I_D = 3.9\text{ A}$	--	700	--	V
I <sub>DSS</sub>	Zero Gate Voltage Drain Current	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$	--	--	1	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, T_C = 125^\circ\text{C}$	--	--	10	$\mu\text{A}$
I <sub>GSSF</sub>	Gate-Body Leakage Current, Forward	$V_{GS} = 30\text{ V}, V_{DS} = 0\text{ V}$	--	--	100	nA
I <sub>GSSR</sub>	Gate-Body Leakage Current, Reverse	$V_{GS} = -30\text{ V}, V_{DS} = 0\text{ V}$	--	--	-100	nA
<b>On Characteristics</b>						
V <sub>GS(th)</sub>	Gate Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	3.0	--	5.0	V
R <sub>DS(on)</sub>	Static Drain-Source On-Resistance	$V_{GS} = 10\text{ V}, I_D = 2.0\text{ A}$	--	1.0	1.2	$\Omega$
g <sub>FS</sub>	Forward Transconductance	$V_{DS} = 40\text{ V}, I_D = 2.0\text{ A}$	--	3.2	--	S
<b>Dynamic Characteristics</b>						
C <sub>iss</sub>	Input Capacitance	$V_{DS} = 25\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	415	540	pF
C <sub>oss</sub>	Output Capacitance		--	210	275	pF
C <sub>riss</sub>	Reverse Transfer Capacitance		--	19.5	--	pF
C <sub>oss</sub>	Output Capacitance	$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, f = 1.0\text{ MHz}$	--	12	16	pF
C <sub>oss eff.</sub>	Effective Output Capacitance	$V_{DS} = 0\text{ V to } 400\text{ V}, V_{GS} = 0\text{ V}$	--	32	--	pF
<b>Switching Characteristics</b>						
t <sub>d(on)</sub>	Turn-On Delay Time	$V_{DD} = 300\text{ V}, I_D = 3.9\text{ A}, R_G = 25\ \Omega$	--	16	45	ns
t <sub>r</sub>	Turn-On Rise Time		--	45	100	ns
t <sub>d(off)</sub>	Turn-Off Delay Time		--	36	85	ns
t <sub>f</sub>	Turn-Off Fall Time		(Note 4)	--	30	70
Q <sub>g</sub>	Total Gate Charge	$V_{DS} = 480\text{ V}, I_D = 3.9\text{ A}, V_{GS} = 10\text{ V}$	--	12.8	16.6	nC
Q <sub>gs</sub>	Gate-Source Charge		--	2.4	--	nC
Q <sub>gd</sub>	Gate-Drain Charge		(Note 4)	--	7.1	--
<b>Drain-Source Diode Characteristics and Maximum Ratings</b>						
I <sub>S</sub>	Maximum Continuous Drain-Source Diode Forward Current		--	--	3.9	A
I <sub>SM</sub>	Maximum Pulsed Drain-Source Diode Forward Current		--	--	11.7	A
V <sub>SD</sub>	Drain-Source Diode Forward Voltage	$V_{GS} = 0\text{ V}, I_S = 3.9\text{ A}$	--	--	1.4	V
t <sub>rr</sub>	Reverse Recovery Time	$V_{GS} = 0\text{ V}, I_S = 3.9\text{ A}, di_f/dt = 100\text{ A}/\mu\text{s}$	--	277	--	ns
Q <sub>rr</sub>	Reverse Recovery Charge		--	2.07	--	$\mu\text{C}$

### Notes:

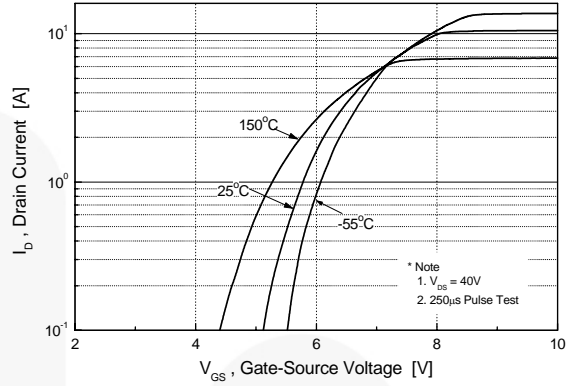
1. Repetitive rating; pulse-width limited by maximum junction temperature.
2.  $I_{AS} = 1.9\text{ A}, V_{DD} = 50\text{ V}, R_G = 25\ \Omega$ , starting  $T_J = 25^\circ\text{C}$ .
3.  $I_{SD} \leq 3.9\text{ A}, di/dt \leq 200\text{ A}/\mu\text{s}, V_{DD} \leq BV_{DSS}$ , starting  $T_J = 25^\circ\text{C}$ .
4. Essentially independent of operating temperature typical characteristics.

## Typical Performance Characteristics

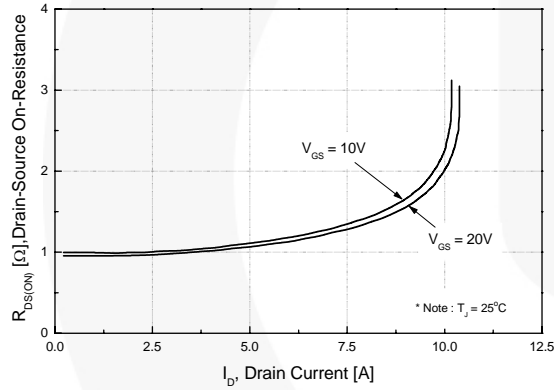
**Figure 1. On-Region Characteristics**



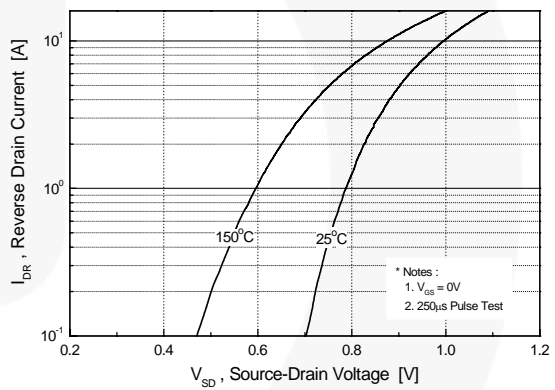
**Figure 2. Transfer Characteristics**



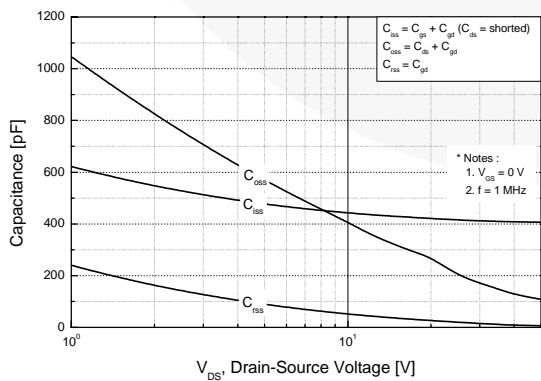
**Figure 3. On-Resistance Variation vs. Drain Current and Gate Voltage**



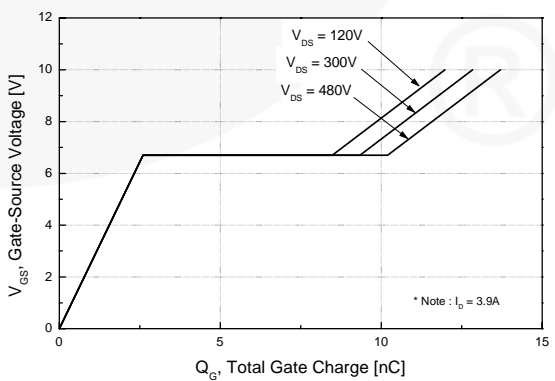
**Figure 4. Body Diode Forward Voltage Variation vs. Source Current and Temperature**



**Figure 5. Capacitance Characteristics**



**Figure 6. Gate Charge Characteristics**



Typical Performance Characteristics (Continued)

Figure 7. Breakdown Voltage Variation vs. Temperature

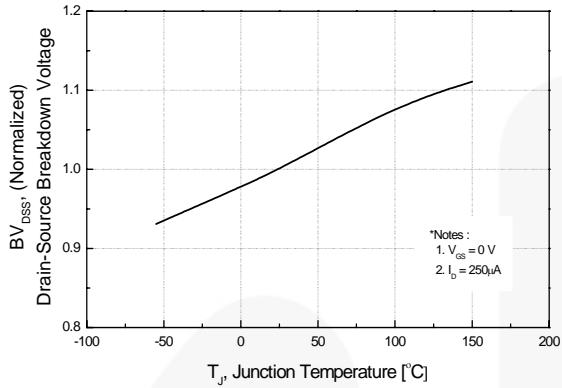


Figure 8. On-Resistance Variation vs. Temperature

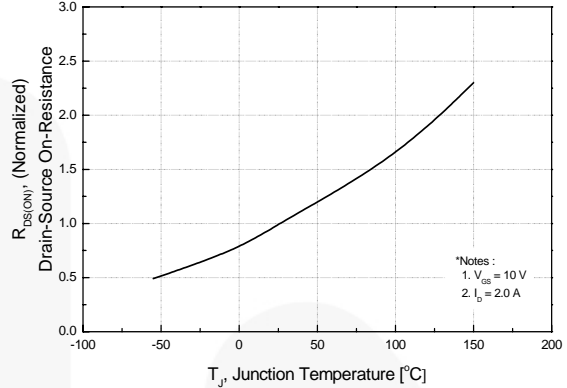


Figure 9. Maximum Safe Operating Area

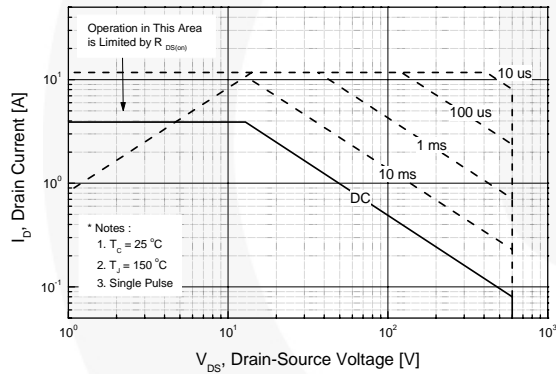


Figure 10. Maximum Drain Current vs. Case Temperature

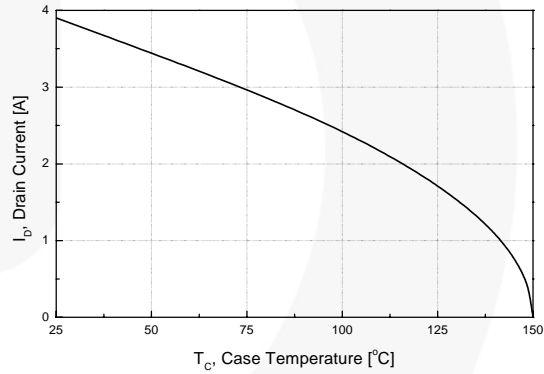
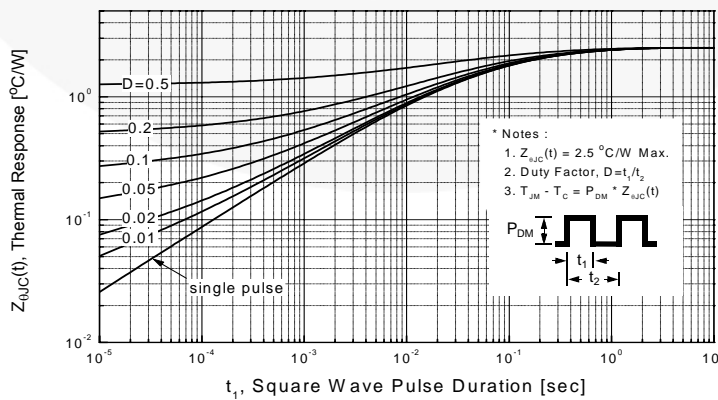


Figure 11. Transient Thermal Response Curve



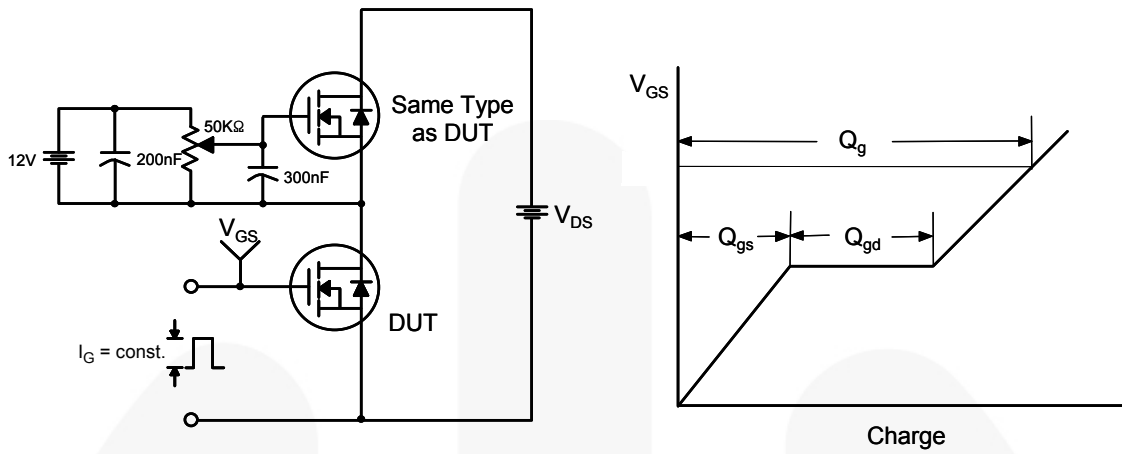


Figure 12. Gate Charge Test Circuit & Waveform

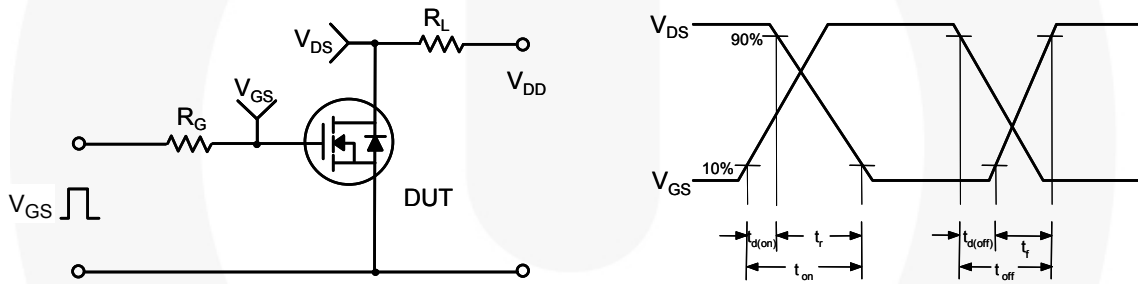


Figure 13. Resistive Switching Test Circuit & Waveforms

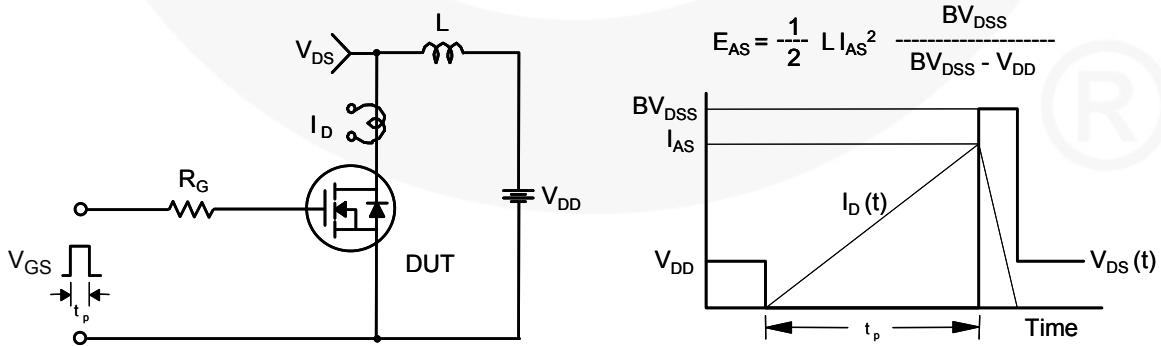


Figure 14. Unclamped Inductive Switching Test Circuit & Waveforms

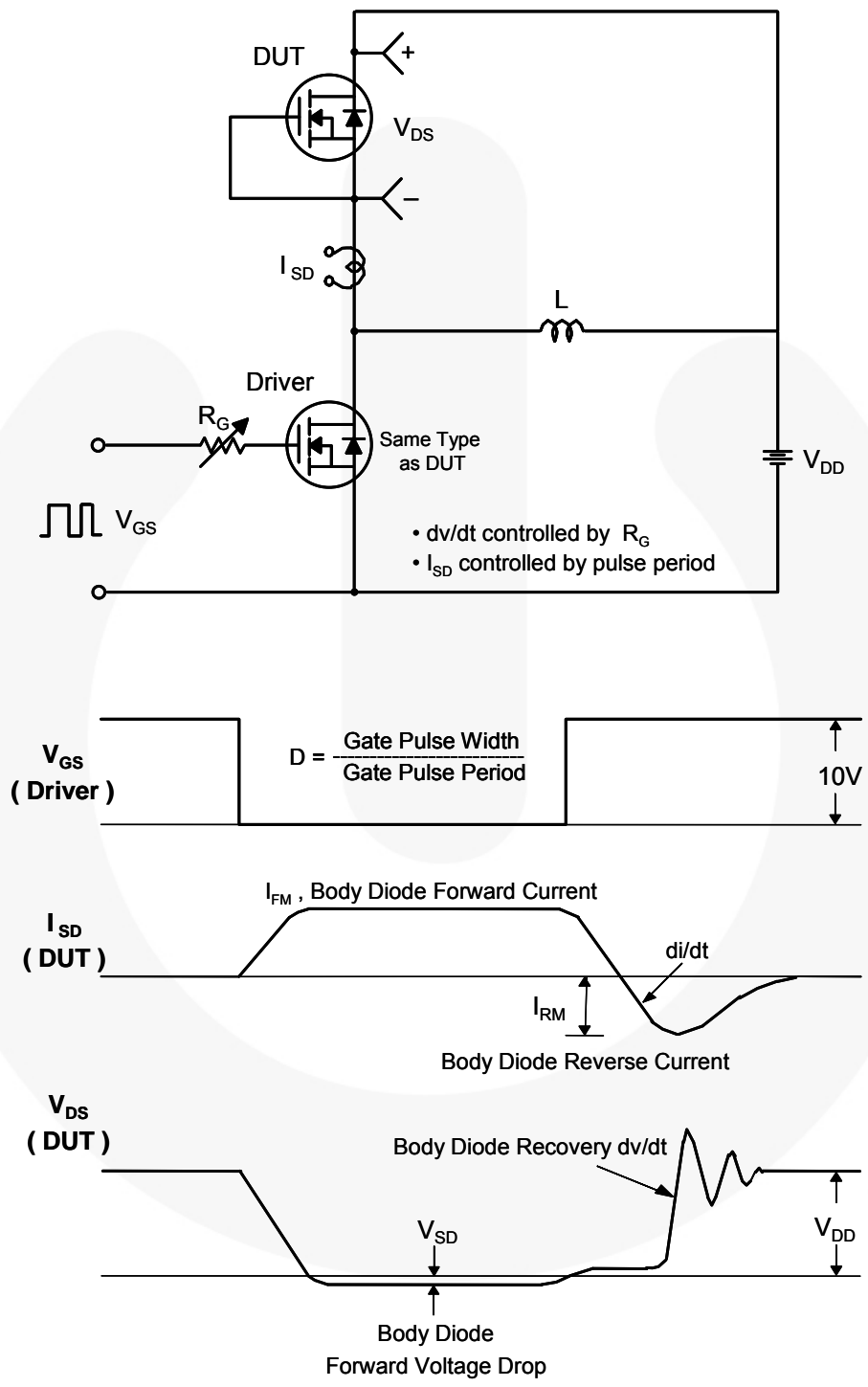
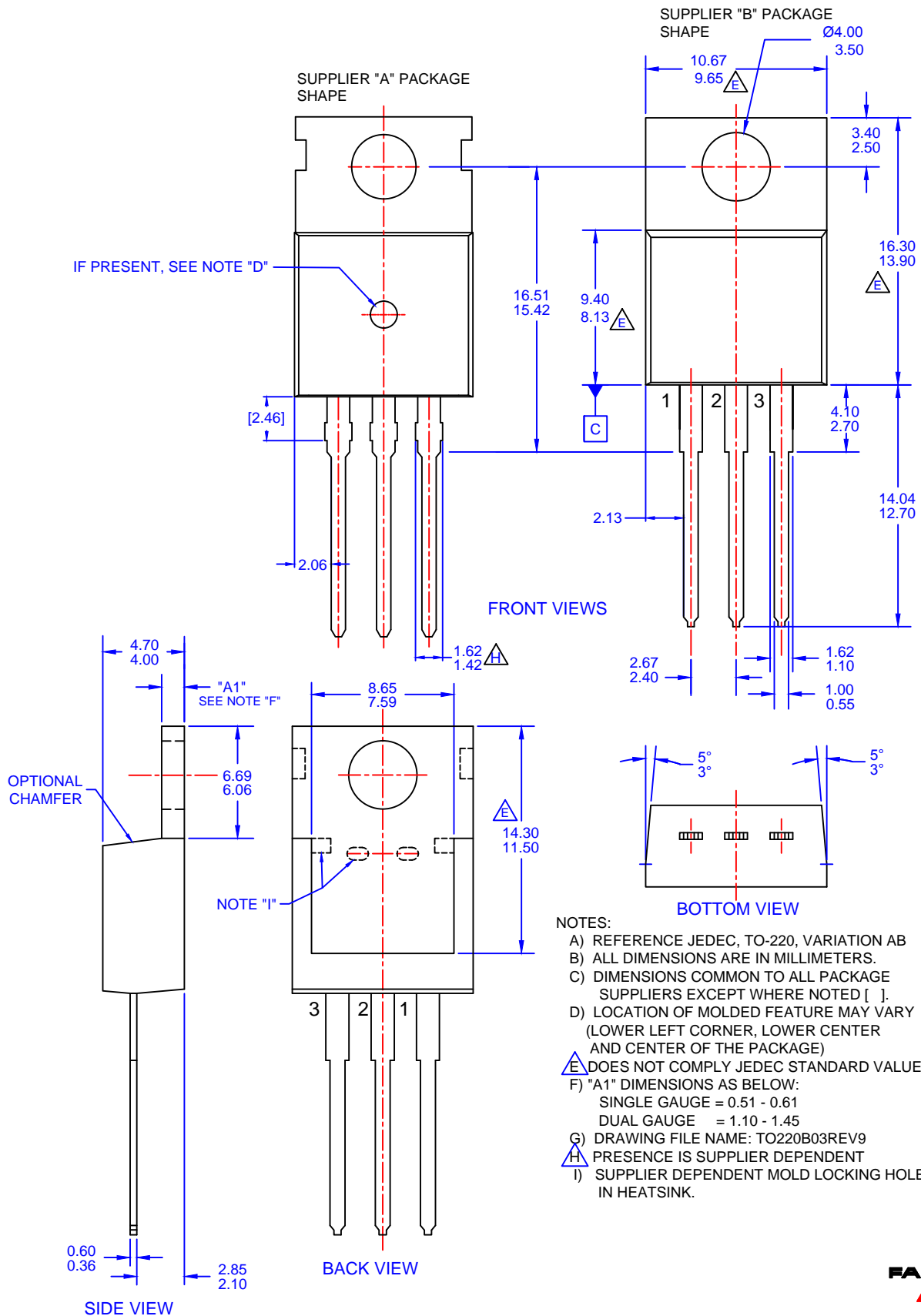


Figure 15. Peak Diode Recovery  $dv/dt$  Test Circuit & Waveforms



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