

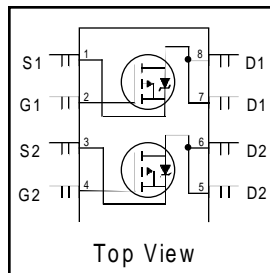


**THE DATASHEET OF  
IRF7306TR**



HEXFET<sup>®</sup> Power MOSFET

- Generation V Technology
- Ultra Low On-Resistance
- Dual P-Channel Mosfet
- Surface Mount
- Available in Tape & Reel
- Dynamic dv/dt Rating
- Fast Switching



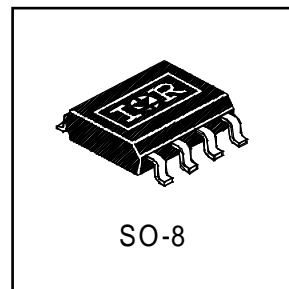
$V_{DSS} = -30V$

$R_{DS(on)} = 0.10\Omega$

**Description**

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The SO-8 has been modified through a customized leadframe for enhanced thermal characteristics and multiple-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red, or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical PCB mount application.



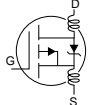
**Absolute Maximum Ratings**

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	10 Sec. Pulsed Drain Current, $V_{GS} @ -10V$	-4.0	A
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-3.6	
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ -10V$	-2.9	
$I_{DM}$	Pulsed Drain Current ①	-14	
$P_D @ T_A = 25^\circ C$	Power Dissipation	2.0	W
	Linear Derating Factor	0.016	W/°C
$V_{GS}$	Gate-to-Source Voltage	$\pm 20$	V
dv/dt	Peak Diode Recovery dv/dt ②	-5.0	V/ns
$T_J, T_{STG}$	Junction and Storage Temperature Range	-55 to + 150	°C

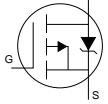
**Thermal Resistance Ratings**

	Parameter	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient④	—	62.5	°C/W

## Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	-30	—	—	V	$V_{GS} = 0V, I_D = -250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	—	-0.037	—	V/°C	Reference to $25^\circ\text{C}$ , $I_D = -1mA$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance	—	—	0.10	$\Omega$	$V_{GS} = -10V, I_D = -1.8A$ ③
		—	—	0.16		$V_{GS} = -4.5V, I_D = -1.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	-1.0	—	—	V	$V_{DS} = V_{GS}, I_D = -250\mu A$
$g_{fs}$	Forward Transconductance	2.5	—	—	S	$V_{DS} = -24V, I_D = -1.8A$
$I_{DSS}$	Drain-to-Source Leakage Current	—	—	-1.0	$\mu A$	$V_{DS} = -24V, V_{GS} = 0V$
		—	—	-25		$V_{DS} = -24V, V_{GS} = 0V, T_J = 125^\circ\text{C}$
$I_{GSS}$	Gate-to-Source Forward Leakage	—	—	-100	nA	$V_{GS} = -20V$
	Gate-to-Source Reverse Leakage	—	—	100		$V_{GS} = 20V$
$Q_g$	Total Gate Charge	—	—	25	nC	$I_D = -1.8A$
$Q_{gs}$	Gate-to-Source Charge	—	—	2.9		$V_{DS} = -24V$
$Q_{gd}$	Gate-to-Drain ("Miller") Charge	—	—	9.0		$V_{GS} = -10V$ , See Fig. 6 and 12 ③
$t_{d(on)}$	Turn-On Delay Time	—	11	—	ns	$V_{DD} = -15V$
$t_r$	Rise Time	—	17	—		$I_D = -1.8A$
$t_{d(off)}$	Turn-Off Delay Time	—	25	—		$R_G = 6.0\Omega$
$t_f$	Fall Time	—	18	—		$R_D = 8.2\Omega$ , See Fig. 10 ③
$L_D$	Internal Drain Inductance	—	4.0	—	nH	Between lead tip and center of die contact 
$L_S$	Internal Source Inductance	—	6.0	—		
$C_{iss}$	Input Capacitance	—	440	—	pF	$V_{GS} = 0V$
$C_{oss}$	Output Capacitance	—	200	—		$V_{DS} = -25V$
$C_{rss}$	Reverse Transfer Capacitance	—	93	—		$f = 1.0MHz$ , See Fig. 5

## Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
$I_S$	Continuous Source Current (Body Diode)	—	—	-2.5	A	MOSFET symbol showing the integral reverse p-n junction diode. 
$I_{SM}$	Pulsed Source Current (Body Diode) ①	—	—	-14		
$V_{SD}$	Diode Forward Voltage	—	—	-1.0	V	$T_J = 25^\circ\text{C}$ , $I_S = -1.8A$ , $V_{GS} = 0V$ ③
$t_{rr}$	Reverse Recovery Time	—	53	80	ns	$T_J = 25^\circ\text{C}$ , $I_F = -1.8A$
$Q_{rr}$	Reverse Recovery Charge	—	66	99	$\mu C$	$di/dt = 100A/\mu s$ ③
$t_{on}$	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$ )				

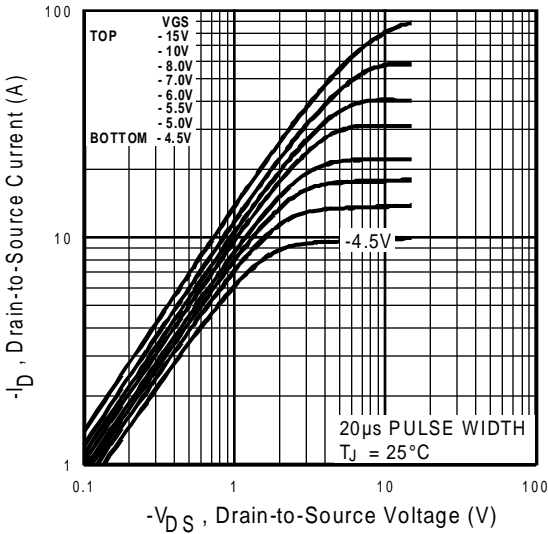
### Notes:

① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )

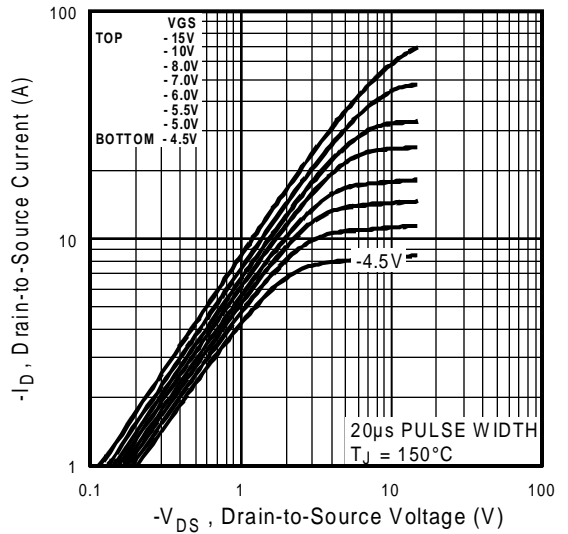
③ Pulse width  $\leq 300\mu s$ ; duty cycle  $\leq 2\%$ .

②  $I_{SD} \leq -1.8A$ ,  $di/dt \leq 90A/\mu s$ ,  $V_{DD} \leq V_{(BR)DSS}$ ,  $T_J \leq 150^\circ\text{C}$

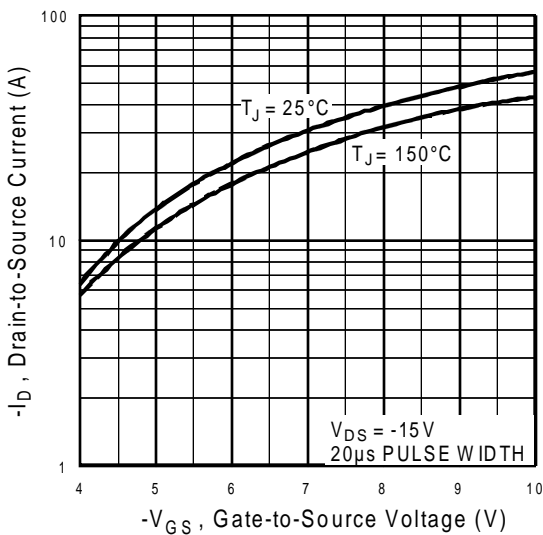
④ Surface mounted on FR-4 board,  $t \leq 10sec$ .



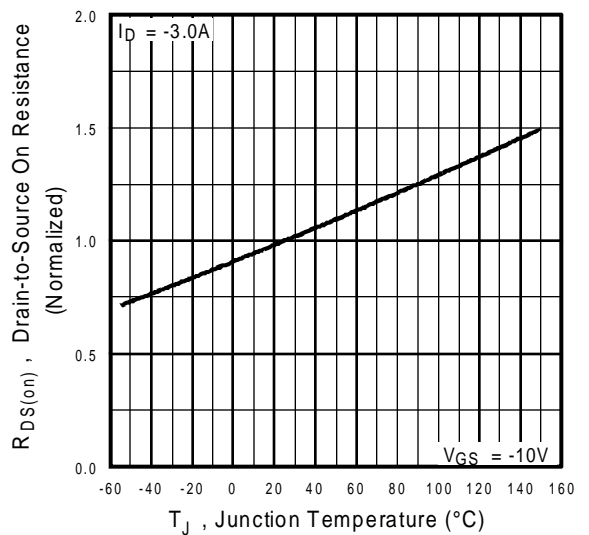
**Fig 1.** Typical Output Characteristics



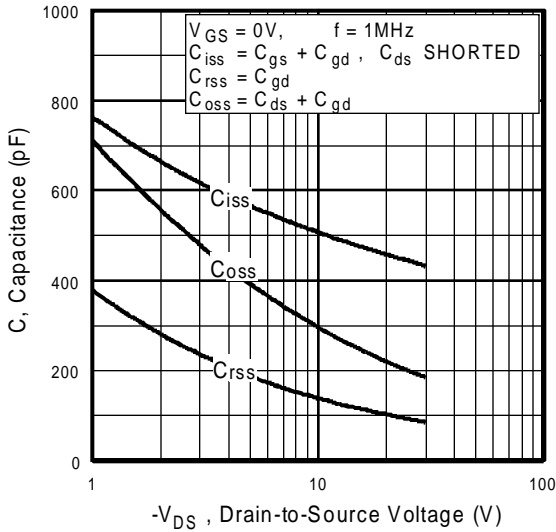
**Fig 2.** Typical Output Characteristics



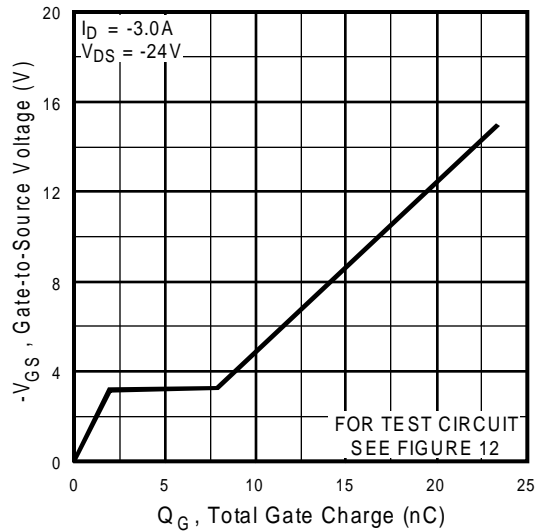
**Fig 3.** Typical Transfer Characteristics



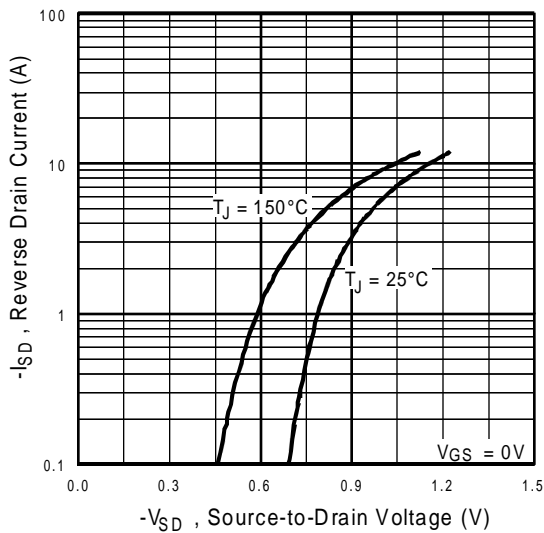
**Fig 4.** Normalized On-Resistance Vs. Temperature



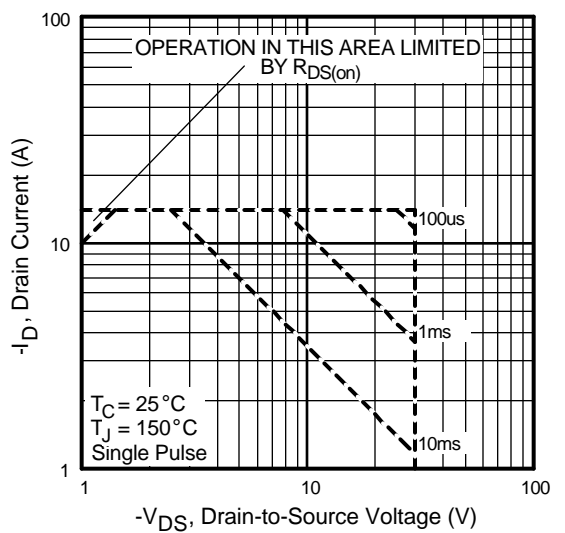
**Fig 5.** Typical Capacitance Vs. Drain-to-Source Voltage



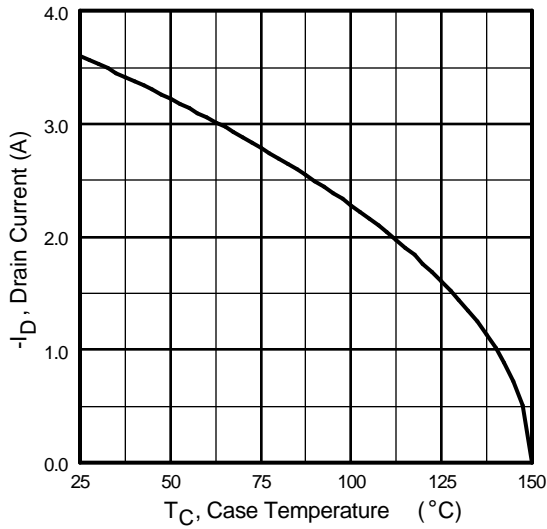
**Fig 6.** Typical Gate Charge Vs. Gate-to-Source Voltage



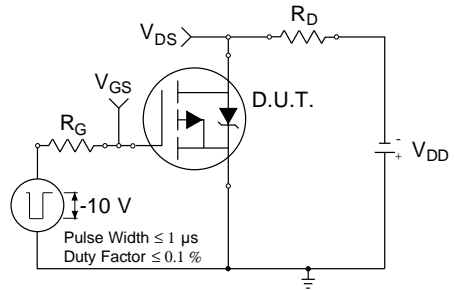
**Fig 7.** Typical Source-Drain Diode Forward Voltage



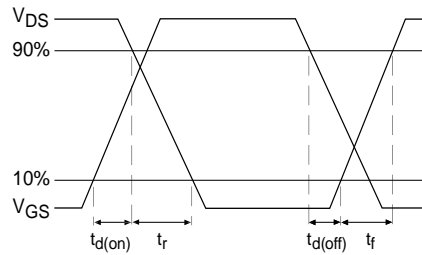
**Fig 8.** Maximum Safe Operating Area



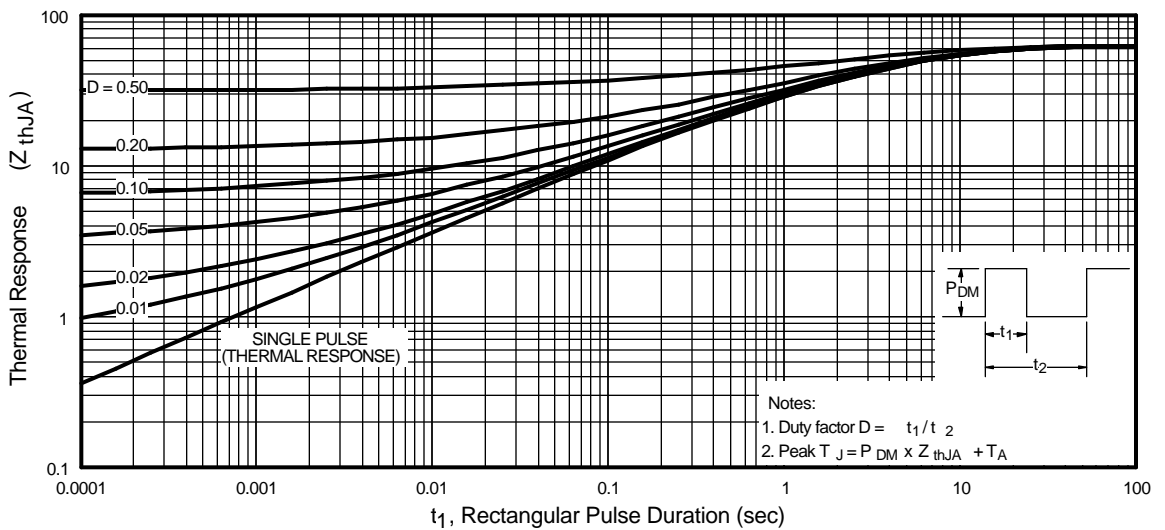
**Fig 9.** Maximum Drain Current Vs. Ambient Temperature



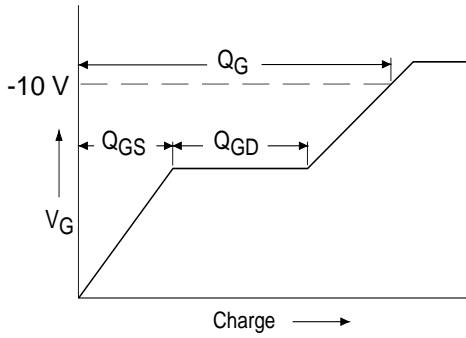
**Fig 10a.** Switching Time Test Circuit



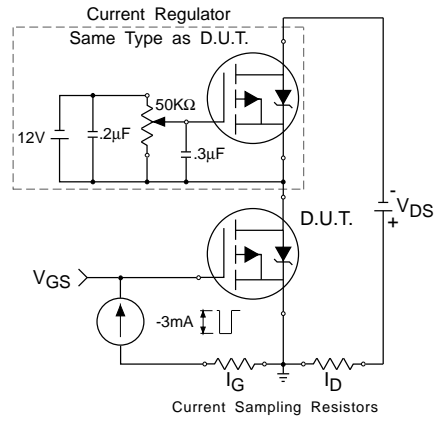
**Fig 10b.** Switching Time Waveforms



**Fig 11.** Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

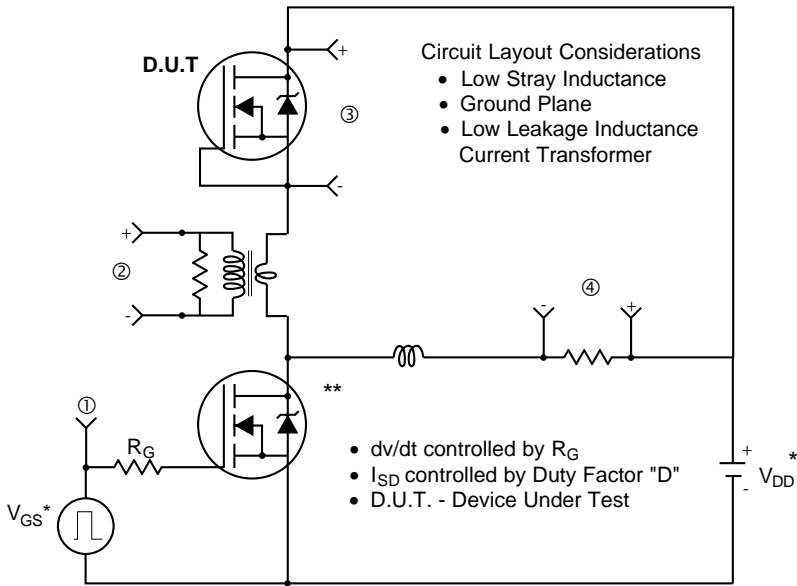


**Fig 12a.** Basic Gate Charge Waveform



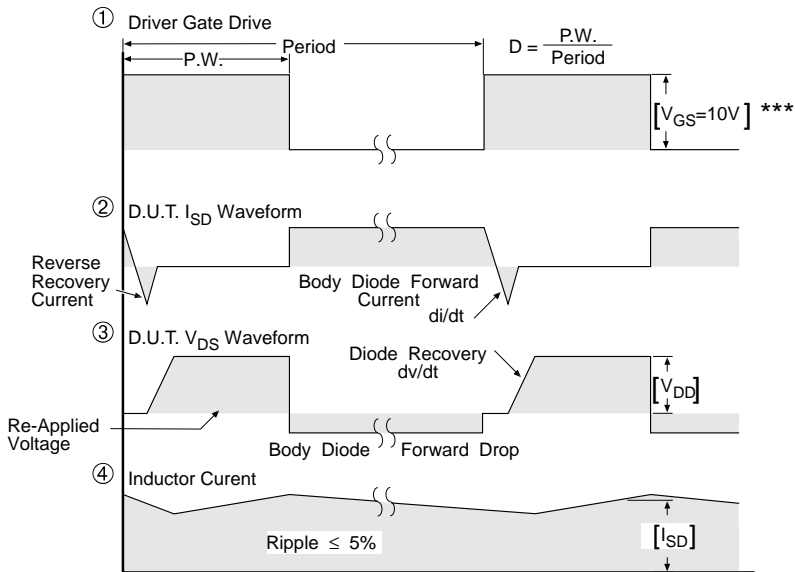
**Fig 12b.** Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



\* Reverse Polarity for P-Channel

\*\* Use P-Channel Driver for P-Channel Measurements



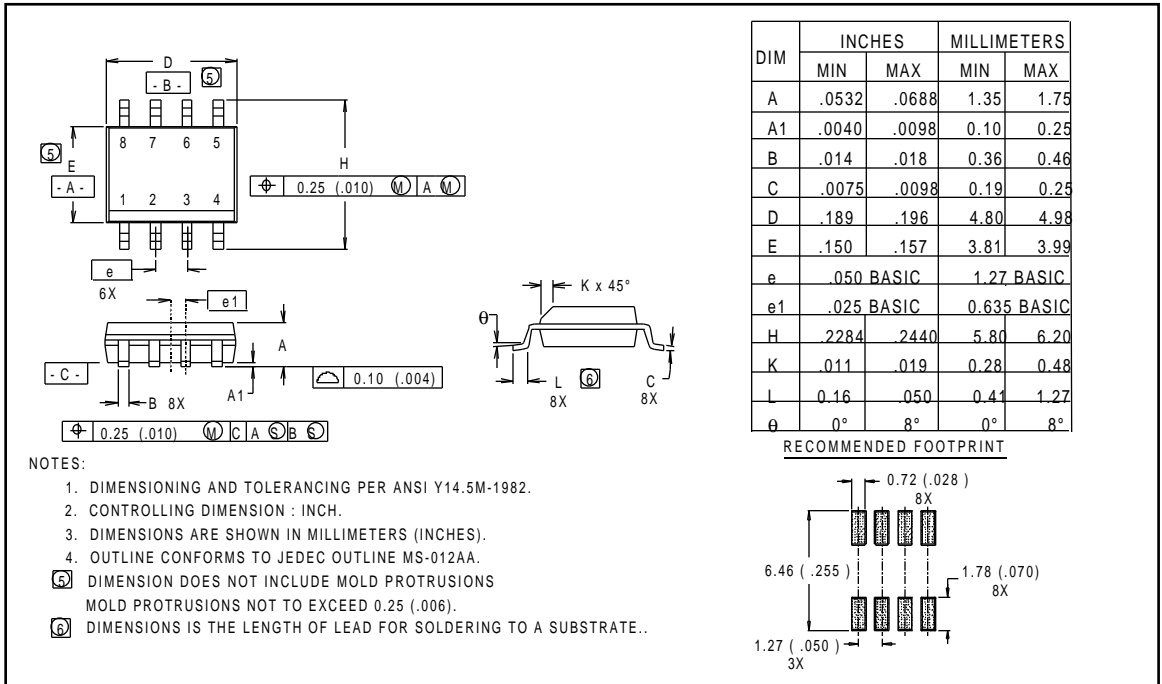
\*\*\*  $V_{GS} = 5.0V$  for Logic Level and  $3V$  Drive Devices

Fig 13. For P-Channel HEXFETS

## Package Outline

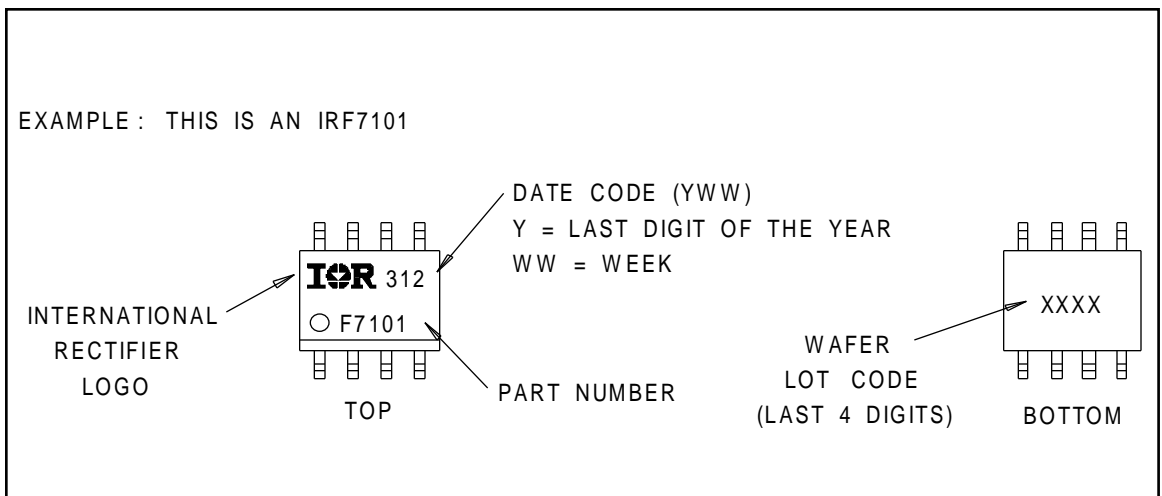
### SO-8 Outline

Dimensions are shown in millimeters (inches)



## Part Marking Information

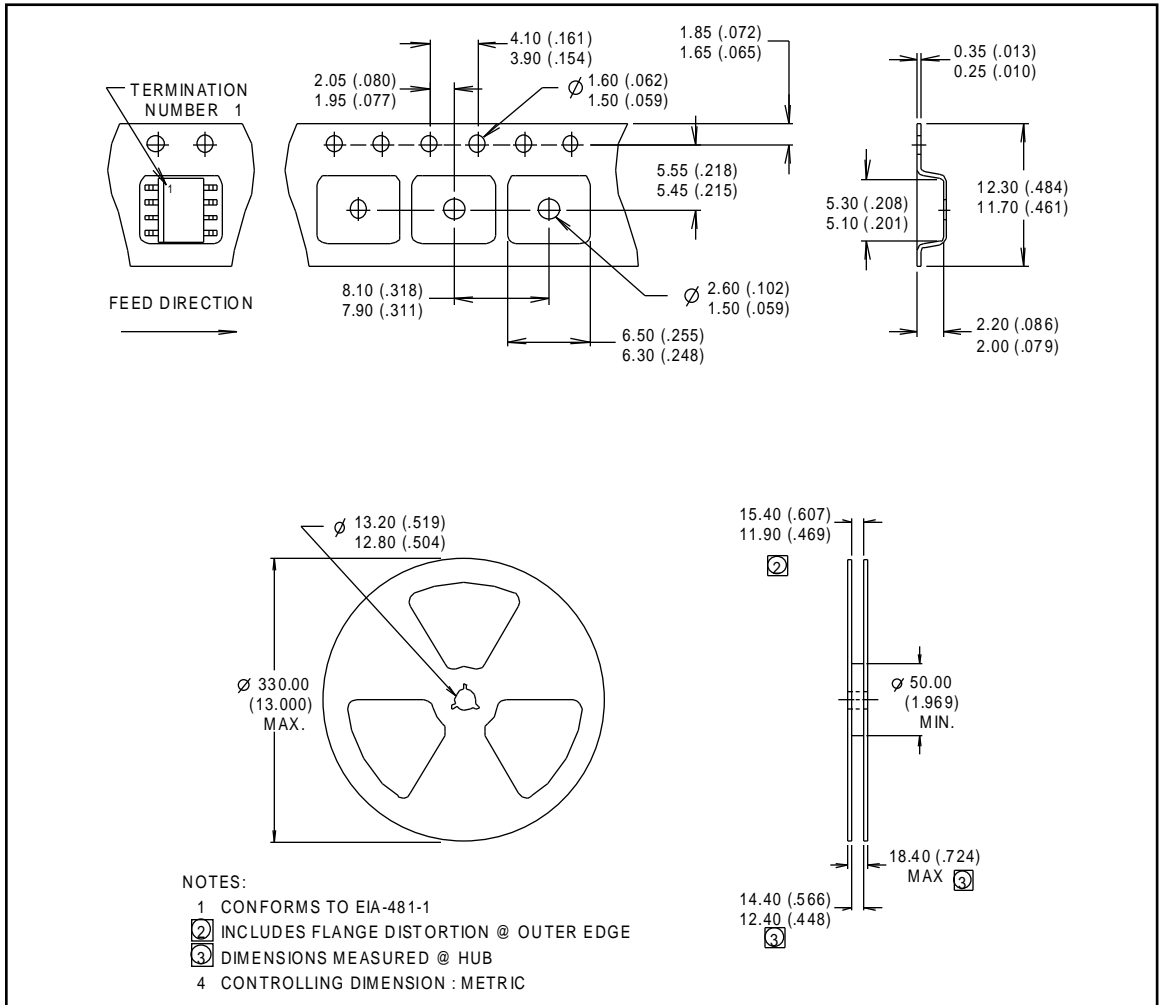
### SO-8



**Tape & Reel Information**

**SO-8**

Dimensions are shown in millimeters (inches)



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