

TOSHIBA Field Effect Transistor Silicon P Channel MOS Type(U-MOSVI)

SSM6J502NU

Power Management Switch Applications

- 1.5V drive
- Low ON-resistance: $R_{DS(ON)} = 60.5 \text{ m}\Omega$ (max) (@ $V_{GS} = -1.5 \text{ V}$)
 $R_{DS(ON)} = 38.4 \text{ m}\Omega$ (max) (@ $V_{GS} = -1.8 \text{ V}$)
 $R_{DS(ON)} = 28.3 \text{ m}\Omega$ (max) (@ $V_{GS} = -2.5 \text{ V}$)
 $R_{DS(ON)} = 23.1 \text{ m}\Omega$ (max) (@ $V_{GS} = -4.5 \text{ V}$)

Absolute Maximum Ratings (Ta = 25°C)

Characteristic	Symbol	Rating	Unit
Drain-Source voltage	V_{DSS}	-20	V
Gate-Source voltage	V_{GSS}	± 8	V
Drain current	DC	I_D	-6
	Pulse	I_{DP} (Note 1)	-24
Power dissipation	P_D (Note 2)		1
		$t \leq 10\text{s}$	2
Channel temperature	T_{ch}	150	°C
Storage temperature	T_{stg}	-55 to 150	°C

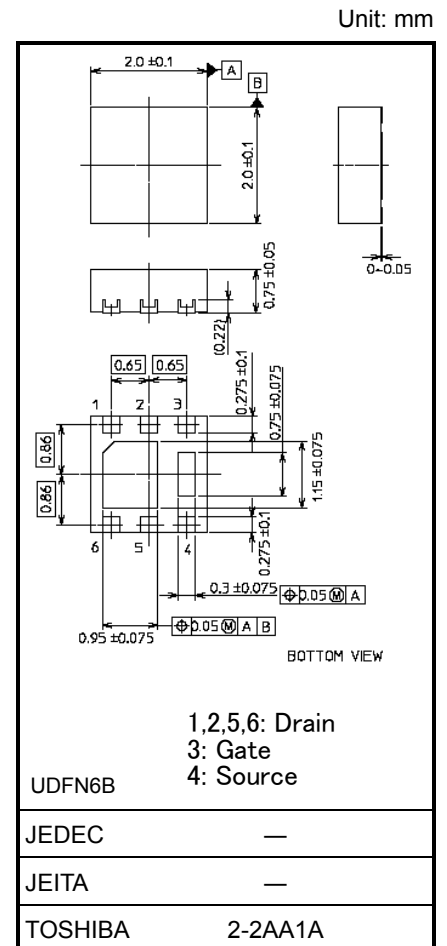
Note: Using continuously under heavy loads (e.g. the application of high temperature/current/voltage and the significant change in temperature, etc.) may cause this product to decrease in the reliability significantly even if the operating conditions (i.e. operating temperature/current/voltage, etc.) are within the absolute maximum ratings.

Please design the appropriate reliability upon reviewing the Toshiba Semiconductor Reliability Handbook ("Handling Precautions"/"Derating Concept and Methods") and individual reliability data (i.e. reliability test report and estimated failure rate, etc).

Note 1: Ensure that the channel temperature does not exceed 150°C

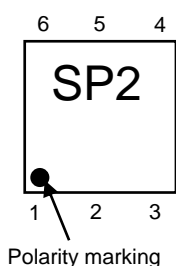
Note 2: Mounted on FR4 board.

(25.4 mm × 25.4 mm × 1.6 mm, Cu Pad: 645 mm²)

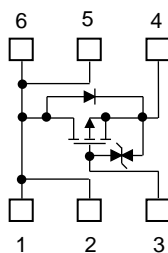


Weight: 8.5 mg (typ.)

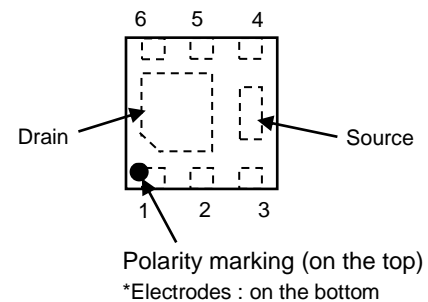
Marking(Top View)



Equivalent Circuit(Top View)



Pin Condition(Top View)



Start of commercial production
2010-11

Electrical Characteristics (Ta = 25°C)

Characteristic	Symbol	Test Conditions	Min	Typ.	Max	Unit
Drain-Source breakdown voltage	V (BR) DSS	ID = -1 mA, VGS = 0 V	-20	—	—	V
	V (BR) DSX	ID = -1 mA, VGS = 5 V (Note 4)	-15	—	—	
Drain cut-off current	IDSS	VDS = -20 V, VGS = 0 V	—	—	-1	μA
Gate leakage current	IGSS	VGS = ±8 V, VDS = 0 V	—	—	±1	μA
Gate threshold voltage	Vth	VDS = -3 V, ID = -1 mA	-0.3	—	-1.0	V
Forward transfer admittance	Yfs	VDS = -3 V, ID = -2.0 A (Note 3)	8.8	17.5	—	S
Drain-source ON-resistance	RDS (ON)	ID = -4.0 A, VGS = -4.5 V (Note 3)	—	18.2	23.1	mΩ
		ID = -4.0 A, VGS = -2.5 V (Note 3)	—	21.5	28.3	
		ID = -2.5 A, VGS = -1.8 V (Note 3)	—	26.1	38.4	
		ID = -1.5 A, VGS = -1.5 V (Note 3)	—	29.7	60.5	
Input capacitance	Ciss	VDS = -10 V, VGS = 0 V, f = 1 MHz	—	1800	—	pF
Output capacitance	Coss					
Reverse transfer capacitance	Crss					
Total Gate Charge	Qg		—	24.8	—	
Gate-Source Charge	Qgs1	VDD = -10 V, ID = -4.4 A VGS = -4.5 V	—	0.8	—	nC
Gate-Drain Charge	Qgd		—	6.8	—	
Switching time	Turn-on time	VDD = -10 V, ID = -1.5 A, VGS = 0 to -2.5 V, RG = 4.7 Ω	—	25	—	ns
	Turn-off time		—	133	—	
Drain-Source forward voltage	VDSF	ID = 4 A, VGS = 0 V (Note 3)	—	0.7	1.2	V

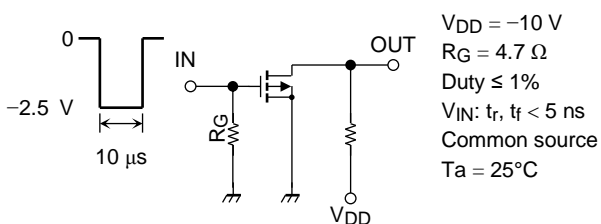
Note 3: Pulse measurement.

Note 4: If a forward bias is applied between gate and source, this device enters V(BR)DSX mode.

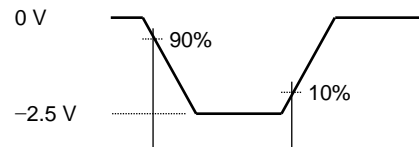
Note that the drain-source breakdown voltage is lowered in this mode.

Switching Time Test Circuit

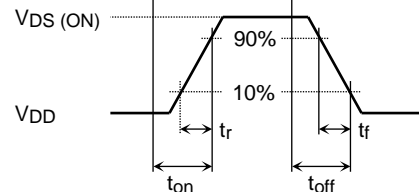
(a) Test circuit



(b) VIN



(c) Vout



Precaution

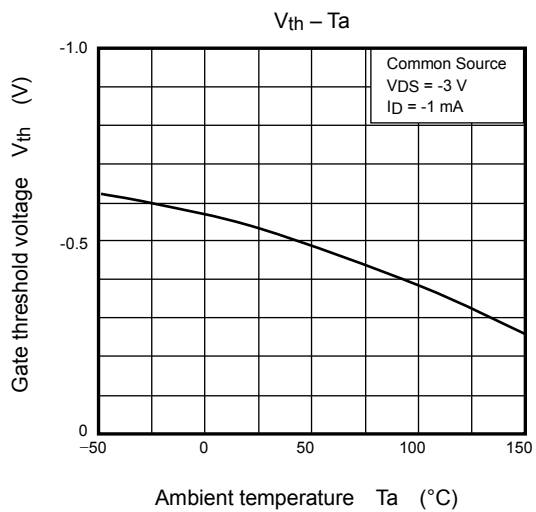
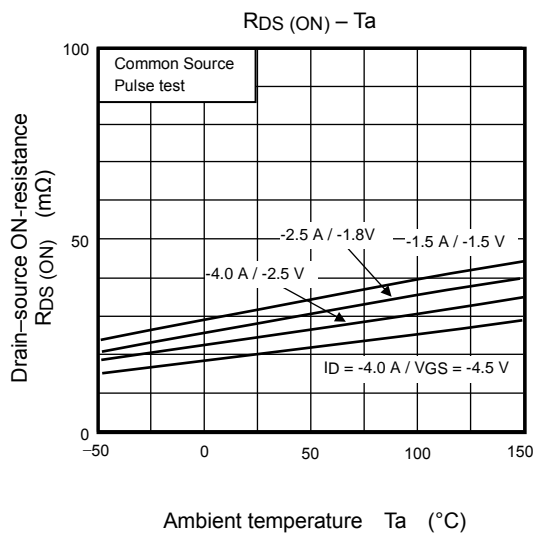
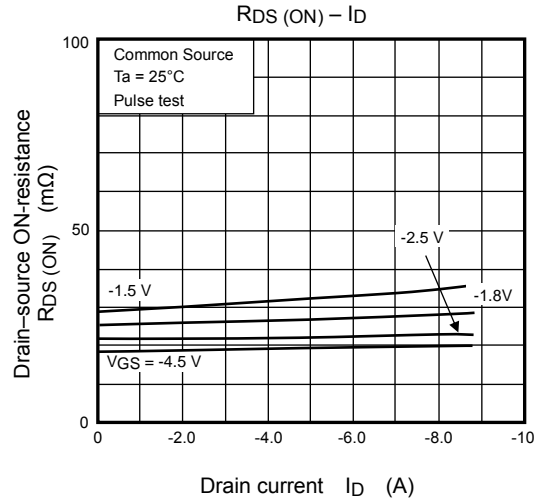
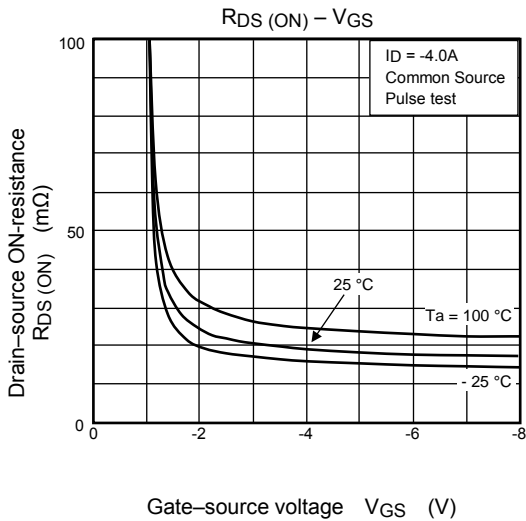
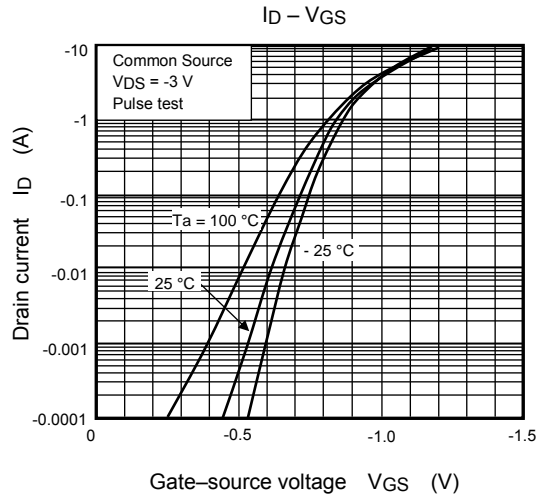
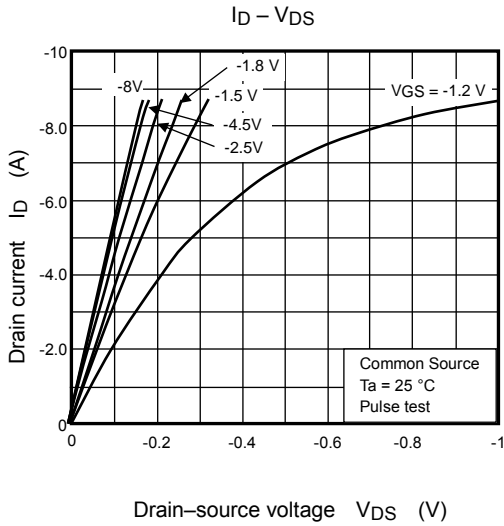
Let Vth be the voltage applied between gate and source that causes the drain current (ID) to below (-1 mA for the SSM6J502NU). Then, for normal switching operation, VGS(on) must be higher than Vth, and VGS(off) must be lower than Vth. This relationship can be expressed as: VGS(off) < Vth < VGS(on).

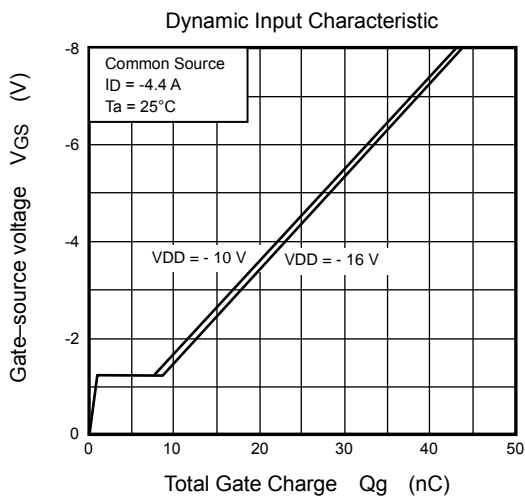
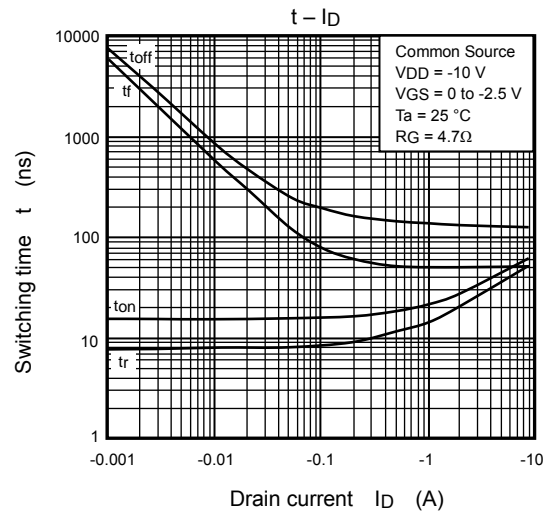
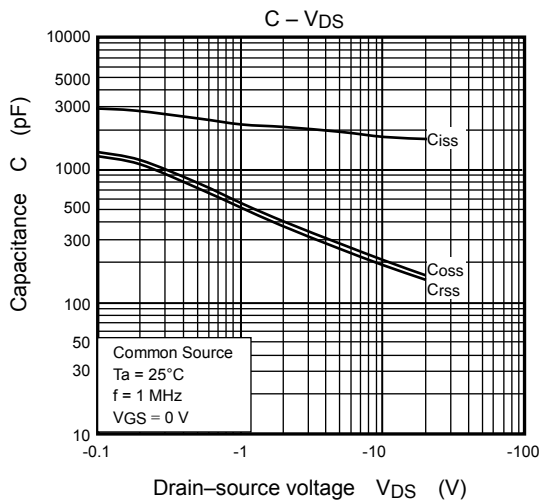
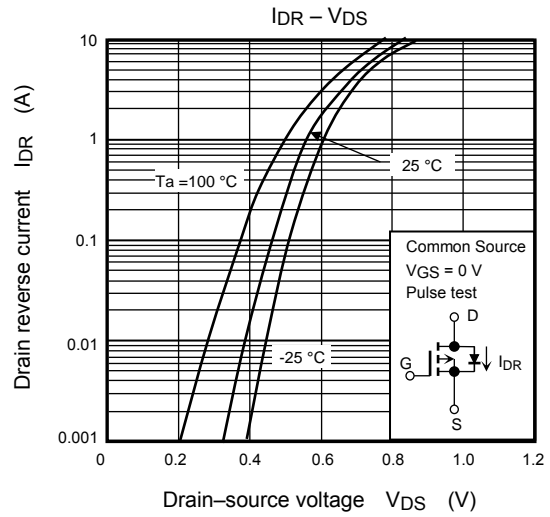
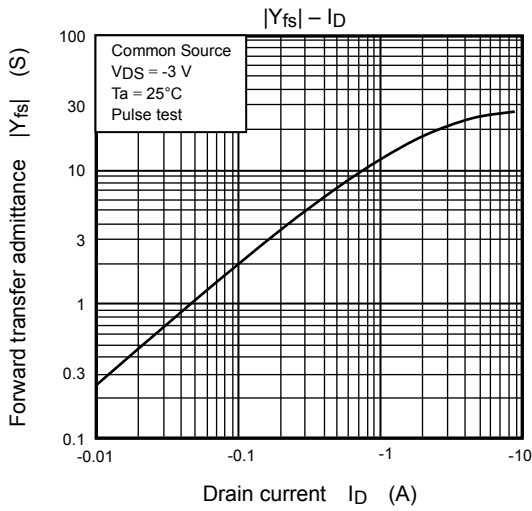
Take this into consideration when using the device.

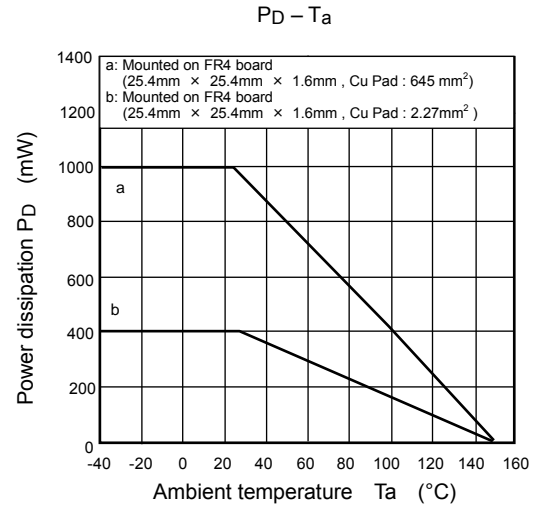
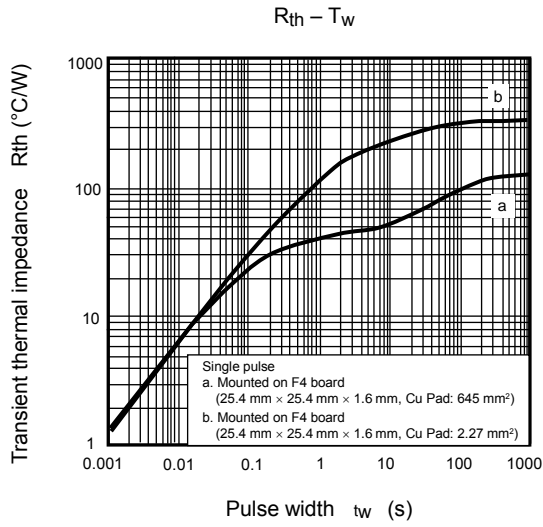
Handling Precaution

When handling individual devices that are not yet mounted on a circuit board, make sure that the environment is protected against electrostatic discharge. Operators should wear antistatic clothing, and containers and other objects that come into direct contact with devices should be made of antistatic materials.

Thermal resistance Rth (ch-a) and power dissipation PD vary depending on board material, board area, board thickness and pad area. When using this device, please take heat dissipation into consideration







Note: The above characteristics curves are presented for reference only and not guaranteed by production test, unless otherwise noted.

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