



**THE DATASHEET OF  
NGD15N41ACT4G**



# NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL, NGP15N41ACL

## Ignition IGBT 15 A, 410 V N-Channel DPAK, D<sup>2</sup>PAK and TO-220

This Logic Level Insulated Gate Bipolar Transistor (IGBT) features monolithic circuitry integrating ESD and Over-Voltage clamped protection for use in inductive coil drivers applications. Primary uses include Ignition, Direct Fuel Injection, or wherever high voltage and high current switching is required.

### Features

- Ideal for Coil-on-Plug Applications
- DPAK Package Offers Smaller Footprint and Increased Board Space
- Gate-Emitter ESD Protection
- Temperature Compensated Gate-Collector Voltage Clamp Limits Stress Applied to Load
- Integrated ESD Diode Protection
- New Design Increases Unclamped Inductive Switching (UIS) Energy Per Area
- Low Threshold Voltage to Interface Power Loads to Logic or Microprocessor Devices
- Low Saturation Voltage
- High Pulsed Current Capability
- Optional Gate Resistor ( $R_G$ ) and Gate-Emitter Resistor ( $R_{GE}$ )
- These are Pb-Free Devices

### MAXIMUM RATINGS ( $T_J = 25^\circ\text{C}$ unless otherwise noted)

Rating	Symbol	Value	Unit
Collector-Emitter Voltage	$V_{CES}$	440	$V_{DC}$
Collector-Gate Voltage	$V_{CER}$	440	$V_{DC}$
Gate-Emitter Voltage	$V_{GE}$	15	$V_{DC}$
Collector Current-Continuous @ $T_C = 25^\circ\text{C}$ - Pulsed	$I_C$	15 50	$A_{DC}$ $A_{AC}$
ESD (Human Body Model) $R = 1500 \Omega$ , $C = 100 \text{ pF}$	ESD	8.0	kV
ESD (Machine Model) $R = 0 \Omega$ , $C = 200 \text{ pF}$	ESD	800	V
Total Power Dissipation @ $T_C = 25^\circ\text{C}$ Derate above $25^\circ\text{C}$	$P_D$	107 0.71	Watts $\text{W}/^\circ\text{C}$
Operating and Storage Temperature Range	$T_J, T_{stg}$	-55 to +175	$^\circ\text{C}$

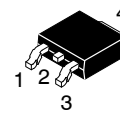
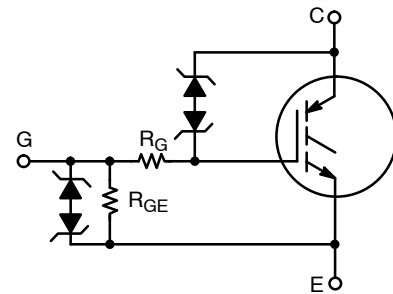
Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.



ON Semiconductor®

<http://onsemi.com>

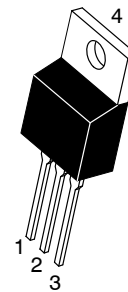
**15 AMPS**  
**410 VOLTS**  
 $V_{CE(on)} \leq 2.1 \text{ V @}$   
 $I_C = 10 \text{ A}, V_{GE} \geq 4.5 \text{ V}$



DPAK  
CASE 369C  
STYLE 2



D<sup>2</sup>PAK  
CASE 418B  
STYLE 4



TO-220AB  
CASE 221A  
STYLE 9

### ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 8 of this data sheet.

### DEVICE MARKING INFORMATION

See general marking information in the device marking section on page 8 of this data sheet.

# NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL, NGP15N41ACL

## UNCLAMPED COLLECTOR-TO-EMITTER AVALANCHE CHARACTERISTICS ( $-55^{\circ} \leq T_J \leq 175^{\circ}C$ )

Characteristic	Symbol	Value	Unit
Single Pulse Collector-to-Emitter Avalanche Energy $V_{CC} = 50\text{ V}$ , $V_{GE} = 5.0\text{ V}$ , Pk $I_L = 16.6\text{ A}$ , $L = 1.8\text{ mH}$ , Starting $T_J = 25^{\circ}C$ $V_{CC} = 50\text{ V}$ , $V_{GE} = 5.0\text{ V}$ , Pk $I_L = 15\text{ A}$ , $L = 1.8\text{ mH}$ , Starting $T_J = 125^{\circ}C$	$E_{AS}$	250 200	mJ

## THERMAL CHARACTERISTICS

Characteristic	Symbol	Value	Unit
Thermal Resistance, Junction to Case	$R_{\theta JC}$	1.4	$^{\circ}C/W$
Thermal Resistance, Junction to Ambient	DPAK (Note 1) $R_{\theta JA}$	100	
	D <sup>2</sup> PAK (Note 1) $R_{\theta JA}$	50	
	TO-220 $R_{\theta JA}$	62.5	
Maximum Lead Temperature for Soldering Purposes, 1/8" from case for 5 seconds	$T_L$	275	$^{\circ}C$

## ELECTRICAL CHARACTERISTICS

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
----------------	--------	-----------------	-------------	-----	-----	-----	------

### OFF CHARACTERISTICS

Collector-Emitter Clamp Voltage	$BV_{CES}$	$I_C = 2.0\text{ mA}$	$T_J = -40^{\circ}C$ to $150^{\circ}C$	380	410	440	$V_{DC}$
		$I_C = 10\text{ mA}$	$T_J = -40^{\circ}C$ to $150^{\circ}C$	380	410	440	
Zero Gate Voltage Collector Current	$I_{CES}$	$V_{CE} = 350\text{ V}$ , $V_{GE} = 0\text{ V}$	$T_J = 25^{\circ}C$	-	2.0	20	$\mu A_{DC}$
			$T_J = 150^{\circ}C$	-	10	40*	
			$T_J = -40^{\circ}C$	-	1.0	10	
Reverse Collector-Emitter Leakage Current	$I_{ECS}$	$V_{CE} = -24\text{ V}$	$T_J = 25^{\circ}C$	-	0.7	2.0	mA
			$T_J = 150^{\circ}C$	-	12	25*	
			$T_J = -40^{\circ}C$	-	0.1	1.0	
Reverse Collector-Emitter Clamp Voltage	$BV_{CES(R)}$	$I_C = -75\text{ mA}$	$T_J = 25^{\circ}C$	27	33	37	$V_{DC}$
			$T_J = 150^{\circ}C$	30	36	40	
			$T_J = -40^{\circ}C$	25	31	35	
Gate-Emitter Clamp Voltage	$BV_{GES}$	$I_G = 5.0\text{ mA}$	$T_J = -40^{\circ}C$ to $150^{\circ}C$	11	13	15	$V_{DC}$
Gate-Emitter Leakage Current	$I_{GES}$	$V_{GE} = 10\text{ V}$	$T_J = -40^{\circ}C$ to $150^{\circ}C$	384	640	1000	$\mu A_{DC}$
Gate Resistor	$R_G$	-	$T_J = -40^{\circ}C$ to $150^{\circ}C$	-	70	-	$\Omega$
Gate Emitter Resistor	$R_{GE}$	-	$T_J = -40^{\circ}C$ to $150^{\circ}C$	10	16	26	k $\Omega$

### ON CHARACTERISTICS (Note 2)

Gate Threshold Voltage	$V_{GE(th)}$	$I_C = 1.0\text{ mA}$ , $V_{GE} = V_{CE}$	$T_J = 25^{\circ}C$	1.1	1.4	1.9	$V_{DC}$
			$T_J = 150^{\circ}C$	0.75	1.0	1.4	
			$T_J = -40^{\circ}C$	1.2	1.6	2.1*	
Threshold Temperature Coefficient (Negative)	-	-	-	-	3.4	-	mV/ $^{\circ}C$

1. When surface mounted to an FR4 board using the minimum recommended pad size.

2. Pulse Test: Pulse Width  $\leq 300\ \mu s$ , Duty Cycle  $\leq 2\%$ .

\*Maximum Value of Characteristic across Temperature Range.

**NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL,  
NGP15N41ACL**

**ELECTRICAL CHARACTERISTICS (continued)**

Characteristic	Symbol	Test Conditions	Temperature	Min	Typ	Max	Unit
<b>ON CHARACTERISTICS (continued) (Note 3)</b>							
Collector-to-Emitter On-Voltage	$V_{CE(on)}$	$I_C = 6.0 \text{ A},$ $V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.0	1.6	1.8	$V_{DC}$
			$T_J = 150^\circ\text{C}$	0.9	1.5	1.8	
			$T_J = -40^\circ\text{C}$	1.1	1.65	1.9*	
		$I_C = 8.0 \text{ A},$ $V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.3	1.8	2.0*	
			$T_J = 150^\circ\text{C}$	1.2	1.7	1.9	
			$T_J = -40^\circ\text{C}$	1.4	1.8	2.0*	
		$I_C = 10 \text{ A},$ $V_{GE} = 4.0 \text{ V}$	$T_J = 25^\circ\text{C}$	1.4	2.0	2.2	
			$T_J = 150^\circ\text{C}$	1.5	2.0	2.3*	
			$T_J = -40^\circ\text{C}$	1.4	2.0	2.2	
		$I_C = 10 \text{ A},$ $V_{GE} = 4.5 \text{ V}$	$T_J = 25^\circ\text{C}$	1.3	1.9	2.1	
			$T_J = 150^\circ\text{C}$	1.3	1.9	2.1	
			$T_J = -40^\circ\text{C}$	1.4	1.95	2.1*	
Forward Transconductance	gfs	$V_{CE} = 5.0 \text{ V}, I_C = 6.0 \text{ A}$	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	8.0	15	25	Mhos

**DYNAMIC CHARACTERISTICS**

Input Capacitance	$C_{ISS}$	$V_{CC} = 25 \text{ V}, V_{GE} = 0 \text{ V}$ $f = 1.0 \text{ MHz}$	$T_J = -40^\circ\text{C}$ to $150^\circ\text{C}$	400	650	1000	pF
Output Capacitance	$C_{OSS}$			30	55	100	
Transfer Capacitance	$C_{RSS}$			3.0	4.5	8.0	

**SWITCHING CHARACTERISTICS**

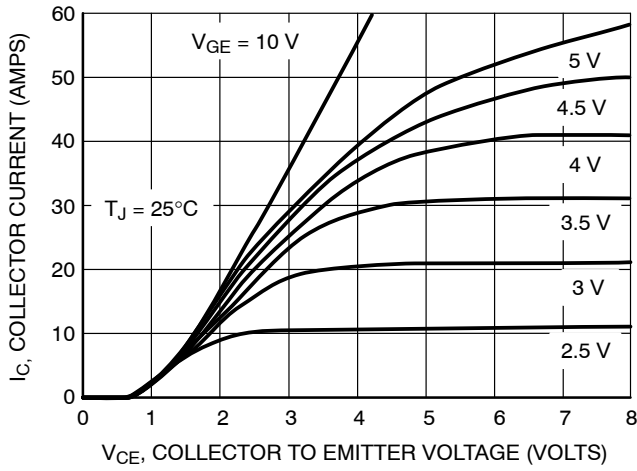
Turn-Off Delay Time (Inductive)	$t_{d(off)}$	$V_{CC} = 300 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, L = 300 \mu\text{H}$	$T_J = 25^\circ\text{C}$	-	4.0	10	$\mu\text{Sec}$
			$T_J = 150^\circ\text{C}$	-	4.5	10	
Fall Time (Inductive)	$t_f$	$V_{CC} = 300 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, L = 300 \mu\text{H}$	$T_J = 25^\circ\text{C}$	-	6.0	12	$\mu\text{Sec}$
			$T_J = 150^\circ\text{C}$	-	10	12	
Turn-Off Delay Time (Resistive)	$t_{d(off)}$	$V_{CC} = 300 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 46 \Omega,$	$T_J = 25^\circ\text{C}$	-	3.0	10	$\mu\text{Sec}$
			$T_J = 150^\circ\text{C}$	-	3.5	10	
Fall Time (Resistive)	$t_f$	$V_{CC} = 300 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 46 \Omega,$	$T_J = 25^\circ\text{C}$	-	8.0	15	$\mu\text{Sec}$
			$T_J = 150^\circ\text{C}$	-	12	15	
Turn-On Delay Time	$t_{d(on)}$	$V_{CC} = 10 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 1.5 \Omega$	$T_J = 25^\circ\text{C}$	-	0.7	4.0	$\mu\text{Sec}$
			$T_J = 150^\circ\text{C}$	-	0.7	4.0	
Rise Time	$t_r$	$V_{CC} = 10 \text{ V}, I_C = 6.5 \text{ A}$ $R_G = 1.0 \text{ k}\Omega, R_L = 1.5 \Omega$	$T_J = 25^\circ\text{C}$	-	4.0	7.0	$\mu\text{Sec}$
			$T_J = 150^\circ\text{C}$	-	5.0	7.0	

3. Pulse Test: Pulse Width  $\leq 300 \mu\text{s}$ , Duty Cycle  $\leq 2\%$ .

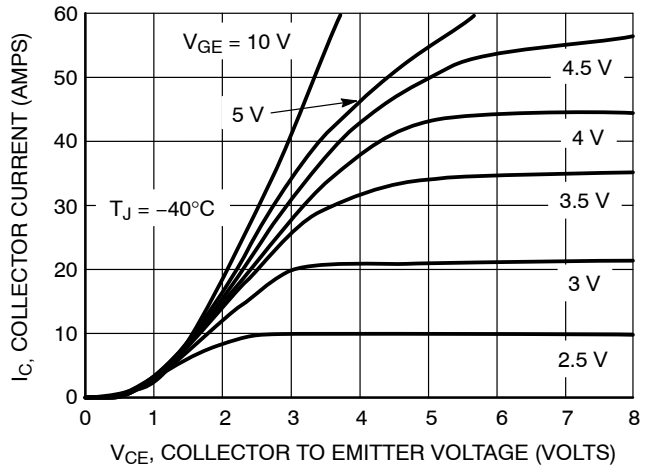
\*Maximum Value of Characteristic across Temperature Range.

**NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL, NGP15N41ACL**

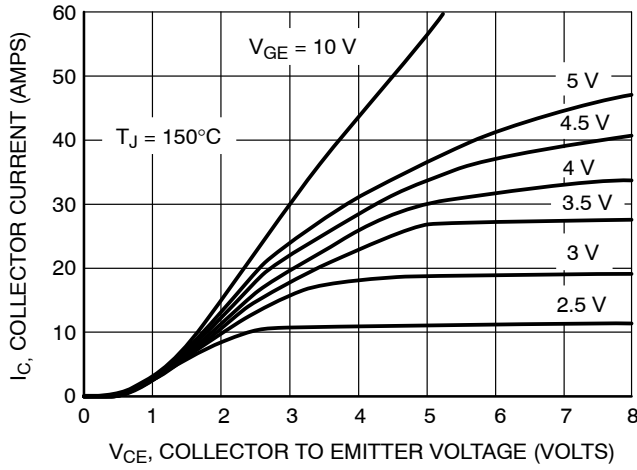
**TYPICAL ELECTRICAL CHARACTERISTICS (unless otherwise noted)**



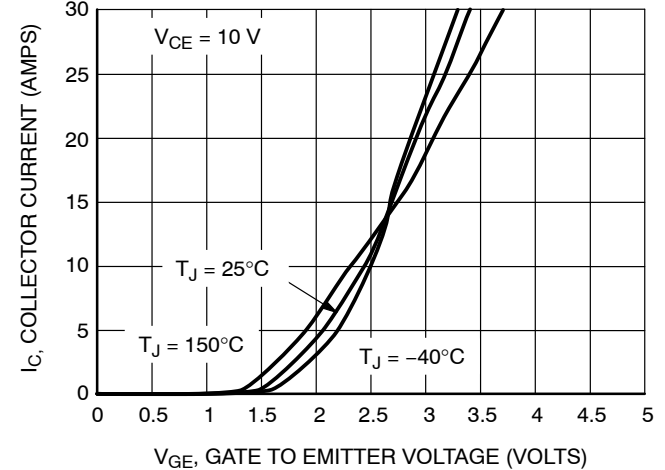
**Figure 1. Output Characteristics**



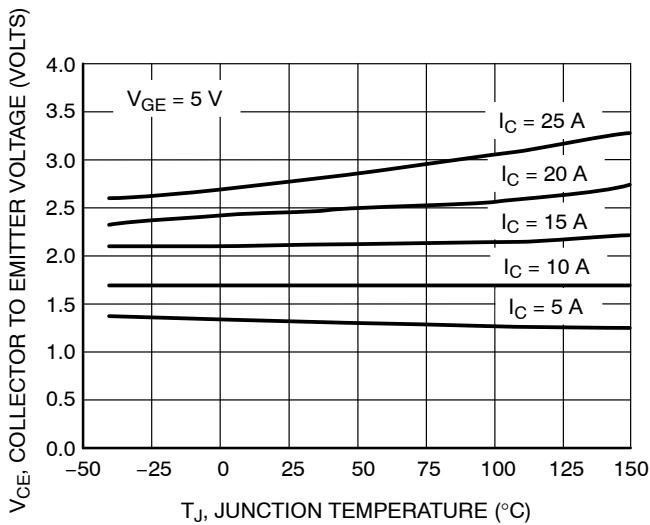
**Figure 2. Output Characteristics**



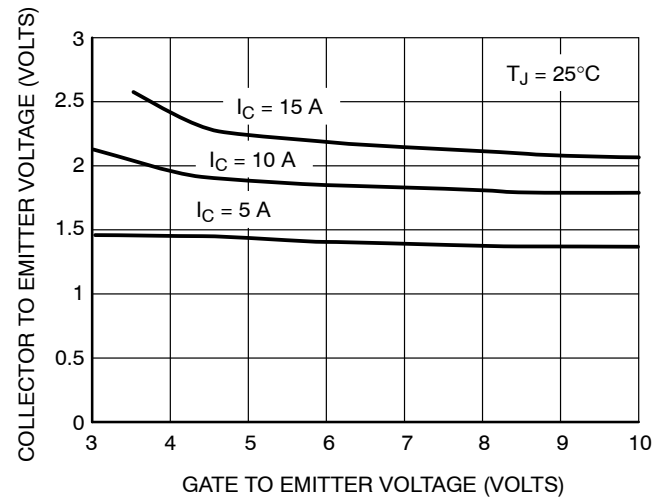
**Figure 3. Output Characteristics**



**Figure 4. Transfer Characteristics**

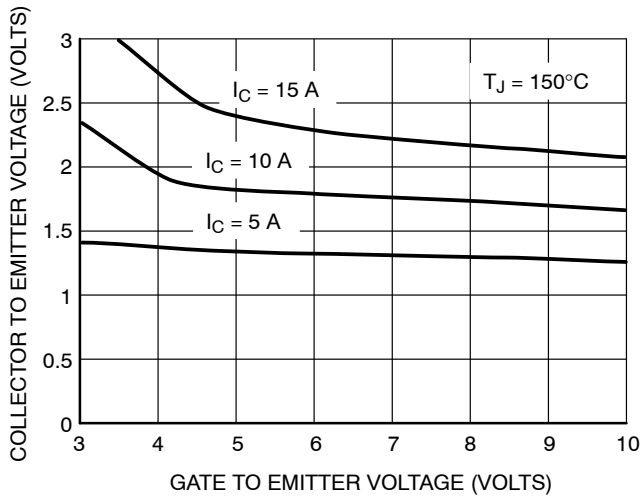


**Figure 5. Collector-to-Emitter Saturation Voltage versus Junction Temperature**

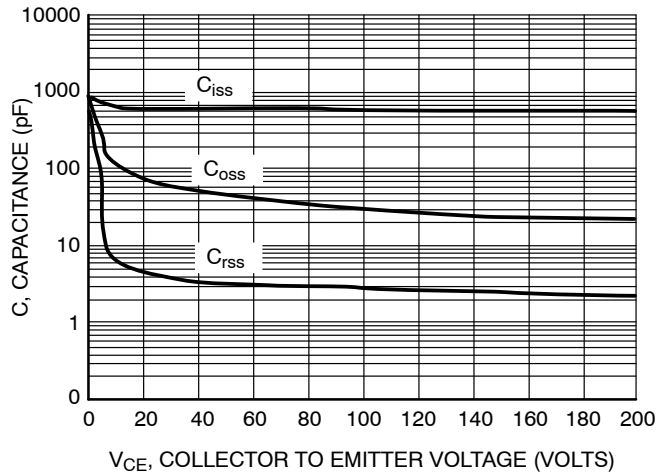


**Figure 6. Collector-to-Emitter Voltage versus Gate-to-Emitter Voltage**

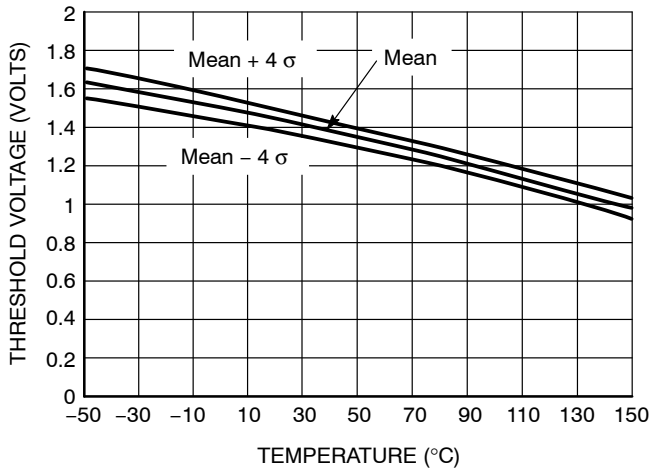
**NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL, NGP15N41ACL**



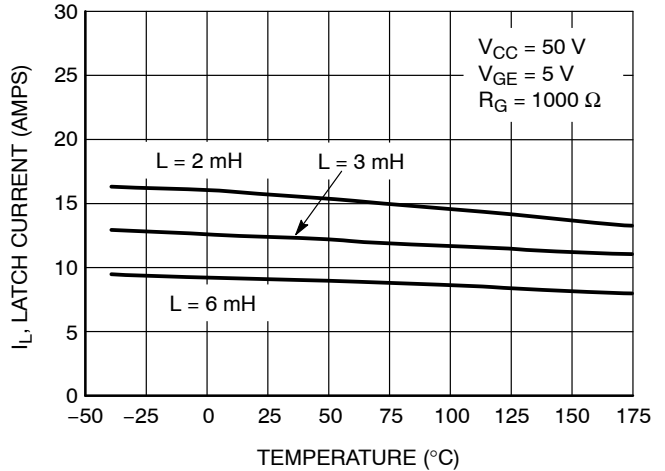
**Figure 7. Collector-to-Emitter Voltage versus Gate-to-Emitter Voltage**



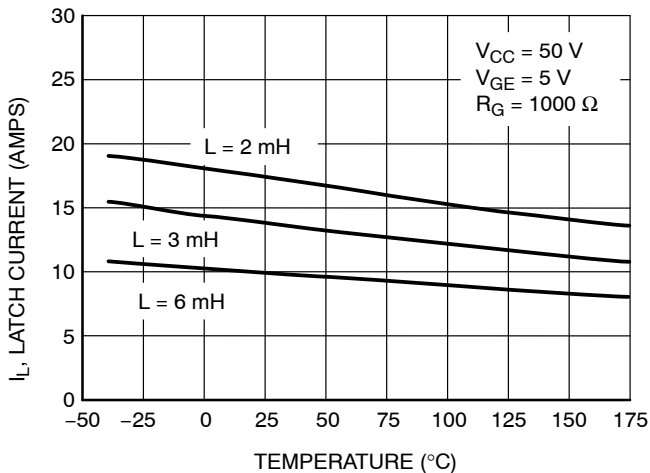
**Figure 8. Capacitance Variation**



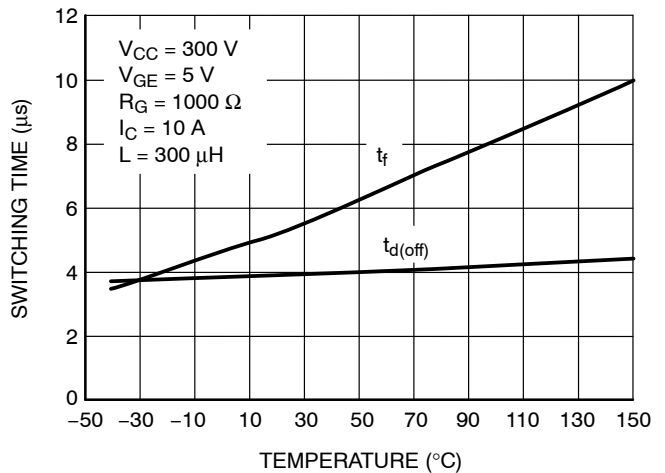
**Figure 9. Gate Threshold Voltage versus Temperature**



**Figure 10. Minimum Open Secondary Latch Current versus Temperature**

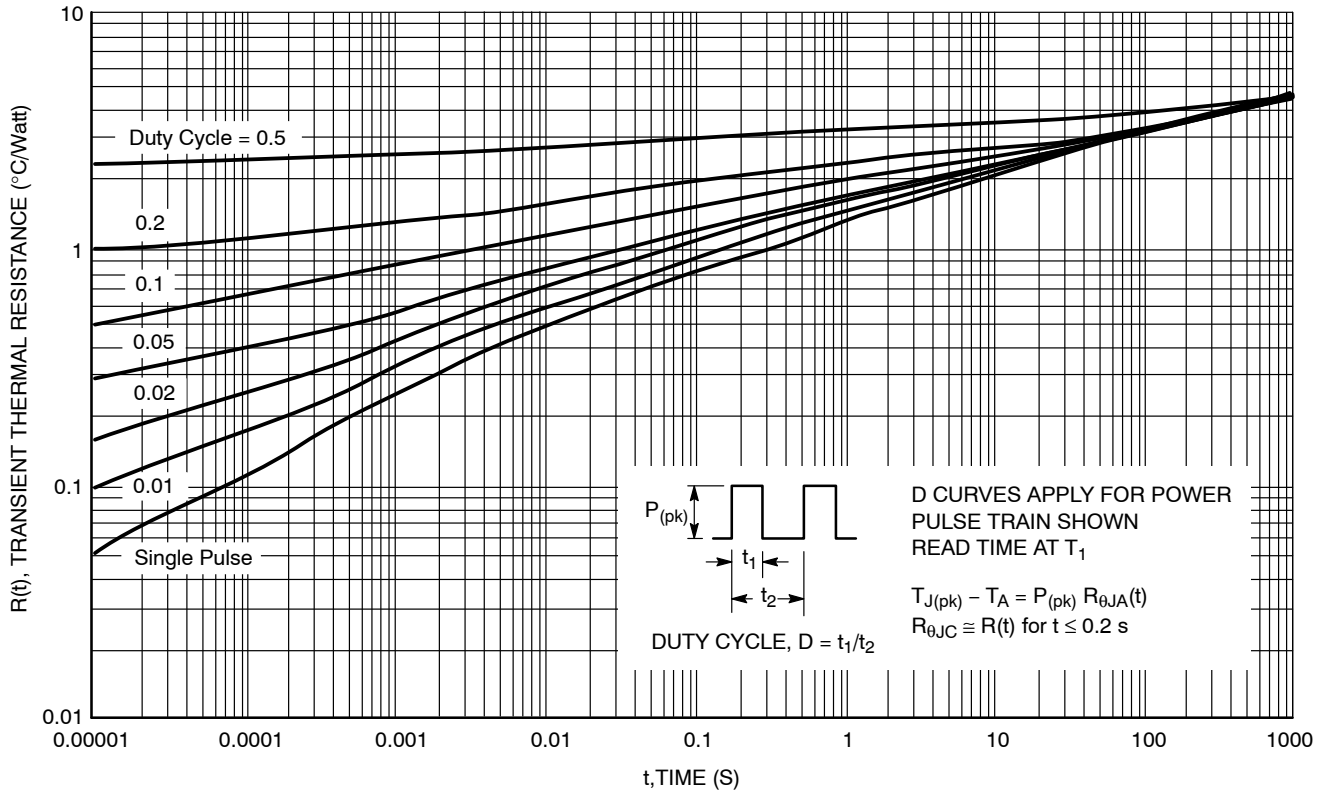


**Figure 11. Typical Open Secondary Latch Current versus Temperature**

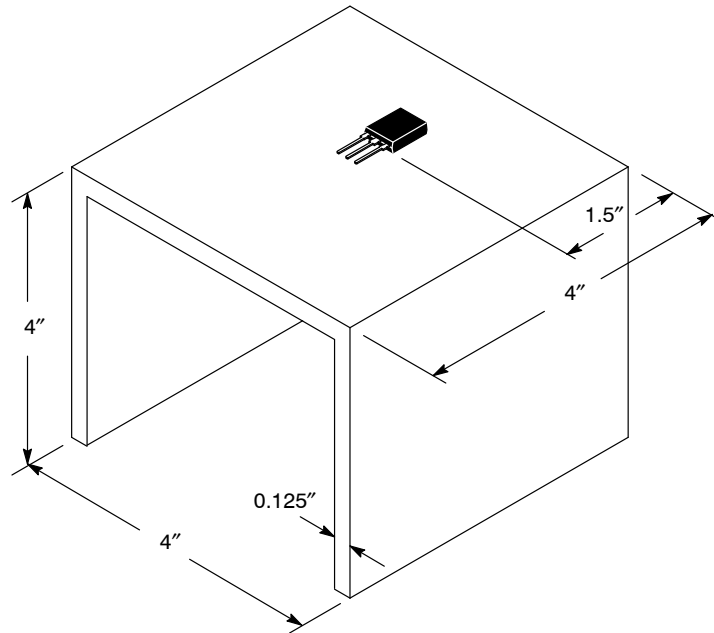


**Figure 12. Inductive Switching Fall Time versus Temperature**

NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL,  
NGP15N41ACL

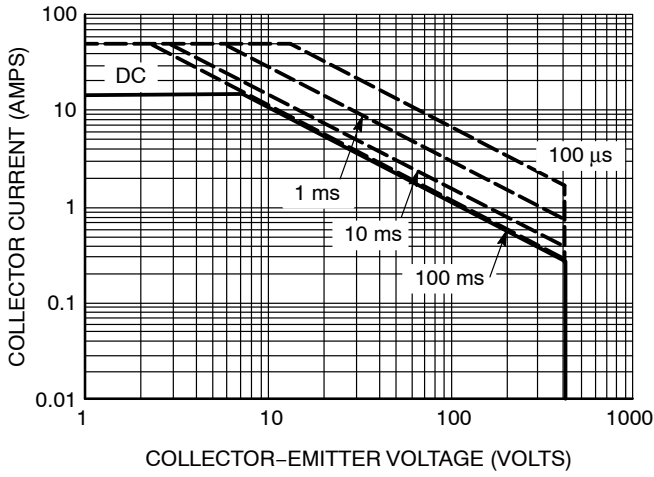


**Figure 13. Transient Thermal Resistance  
(Non-normalized Junction-to-Ambient mounted on  
fixture in Figure 14)**

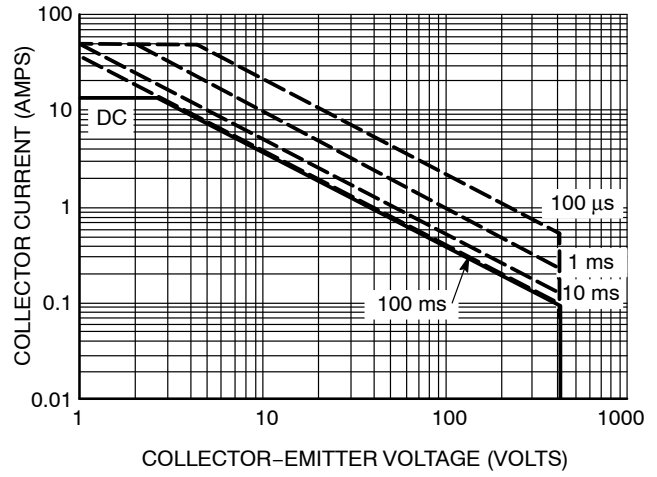


**Figure 14. Test Fixture for Transient Thermal Curve  
(48 square inches of 1/8" thick aluminum)**

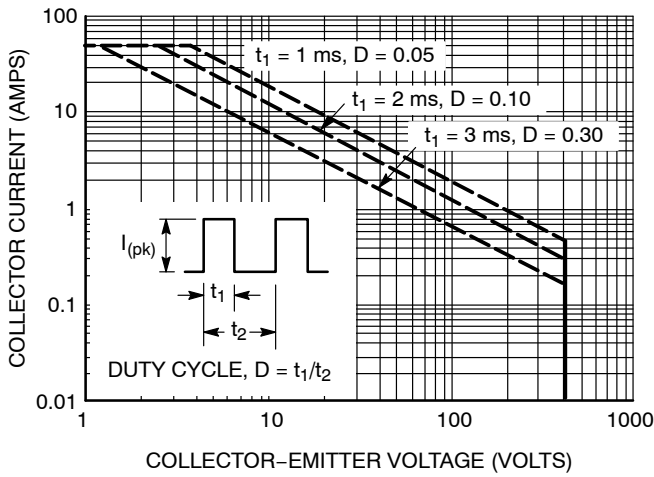
**NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL,  
NGP15N41ACL**



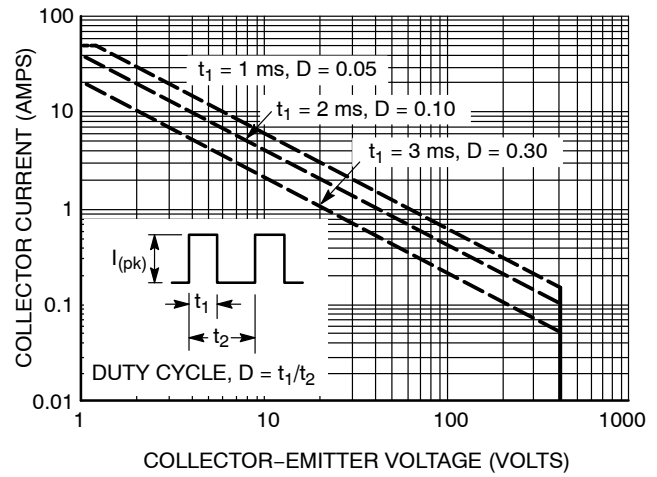
**Figure 15. Single Pulse Safe Operating Area  
(Mounted on an Infinite Heatsink at  $T_A = 25^\circ\text{C}$ )**



**Figure 16. Single Pulse Safe Operating Area  
(Mounted on an Infinite Heatsink at  $T_A = 125^\circ\text{C}$ )**



**Figure 17. Pulse Train Safe Operating Area  
(Mounted on an Infinite Heatsink at  $T_C = 25^\circ\text{C}$ )**



**Figure 18. Pulse Train Safe Operating Area  
(Mounted on an Infinite Heatsink at  $T_C = 125^\circ\text{C}$ )**

**NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL,  
NGP15N41ACL**

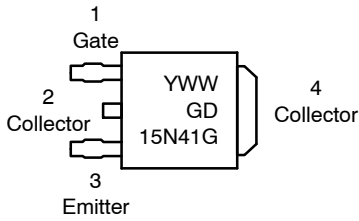
**ORDERING INFORMATION**

Device	Package Type	Shipping†
NGD15N41CLT4G	DPAK (Pb-Free)	2500/Tape & Reel
NGD15N41ACL4G		
NGB15N41CLT4G	D <sup>2</sup> PAK (Pb-Free)	800/Tape & Reel
NGB15N41ACL4G		
NGP15N41CLG	TO-220 (Pb-Free)	50 Units/Rail
NGP15N41ACLG		

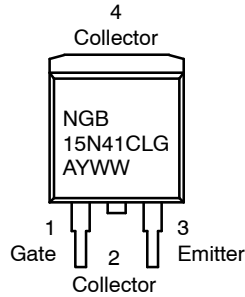
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

**MARKING DIAGRAMS**

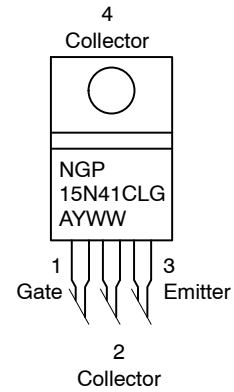
**DPAK  
CASE 369C  
STYLE 7**



**D<sup>2</sup>PAK  
CASE 418B  
STYLE 4**



**TO-220AB  
CASE 221A  
STYLE 9**

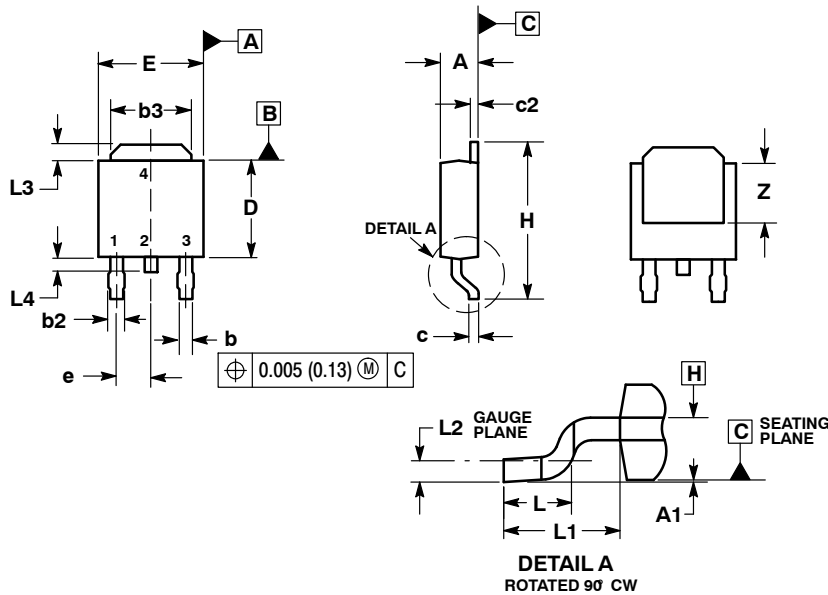


A = Assembly Location  
Y = Year  
WW = Work Week  
G = Pb-Free Device

# NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL, NGP15N41ACL

## PACKAGE DIMENSIONS

### DPAK (SINGLE GAUGE) CASE 369C-01 ISSUE D

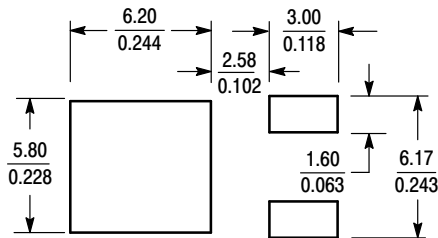


#### NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: INCHES.
3. THERMAL PAD CONTOUR OPTIONAL WITHIN DIMENSIONS b3, L3 and Z.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR BURRS. MOLD FLASH, PROTRUSIONS, OR GATE BURRS SHALL NOT EXCEED 0.006 INCHES PER SIDE.
5. DIMENSIONS D AND E ARE DETERMINED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
6. DATUMS A AND B ARE DETERMINED AT DATUM PLANE H.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.086	0.094	2.18	2.38
A1	0.000	0.005	0.00	0.13
b	0.025	0.035	0.63	0.89
b2	0.030	0.045	0.76	1.14
b3	0.180	0.215	4.57	5.46
c	0.018	0.024	0.46	0.61
c2	0.018	0.024	0.46	0.61
D	0.235	0.245	5.97	6.22
E	0.250	0.265	6.35	6.73
e	0.090 BSC		2.29 BSC	
H	0.370	0.410	9.40	10.41
L	0.055	0.070	1.40	1.78
L1	0.108 REF		2.74 REF	
L2	0.020 BSC		0.51 BSC	
L3	0.035	0.050	0.89	1.27
L4	---	0.040	---	1.01
Z	0.155	---	3.93	---

#### SOLDERING FOOTPRINT\*



SCALE 3:1  $\left( \frac{\text{mm}}{\text{inches}} \right)$

#### STYLE 2:

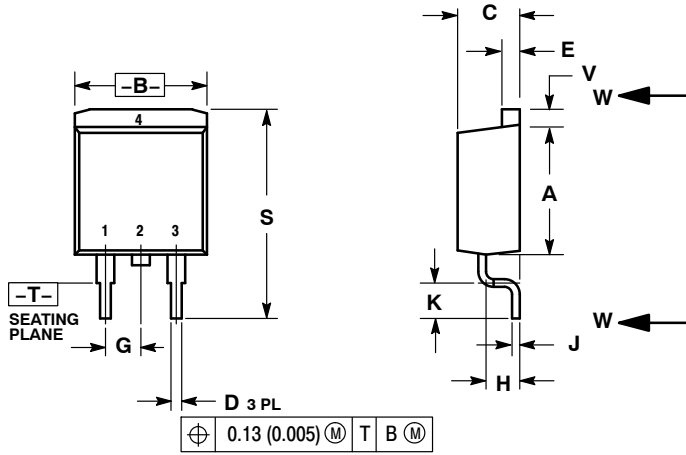
- PIN 1. GATE
2. DRAIN
3. SOURCE
4. DRAIN

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL,  
NGP15N41ACL

PACKAGE DIMENSIONS

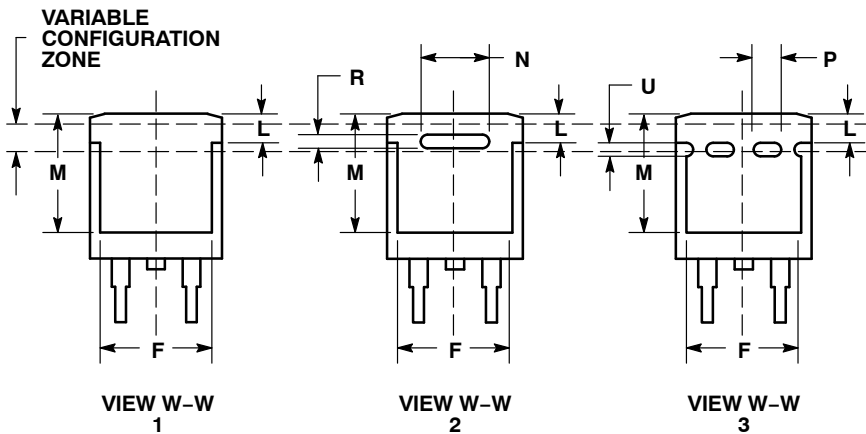
D<sup>2</sup>PAK  
CASE 418B-04  
ISSUE K



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 418B-01 THRU 418B-03 OBSOLETE, NEW STANDARD 418B-04.

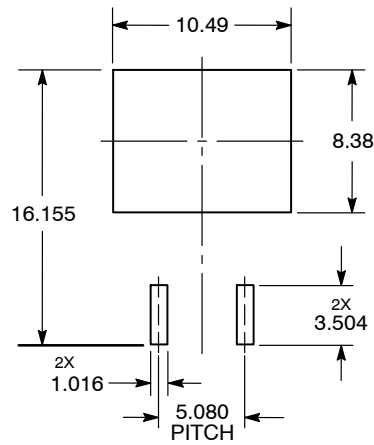
DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.340	0.380	8.64	9.65
B	0.380	0.405	9.65	10.29
C	0.160	0.190	4.06	4.83
D	0.020	0.035	0.51	0.89
E	0.045	0.055	1.14	1.40
F	0.310	0.350	7.87	8.89
G	0.100 BSC		2.54 BSC	
H	0.080	0.110	2.03	2.79
J	0.018	0.025	0.46	0.64
K	0.090	0.110	2.29	2.79
L	0.052	0.072	1.32	1.83
M	0.280	0.320	7.11	8.13
N	0.197 REF		5.00 REF	
P	0.079 REF		2.00 REF	
R	0.039 REF		0.99 REF	
S	0.575	0.625	14.60	15.88
V	0.045	0.055	1.14	1.40



STYLE 4:

- PIN 1. GATE
- COLLECTOR
- EMITTER
- COLLECTOR

SOLDERING FOOTPRINT\*



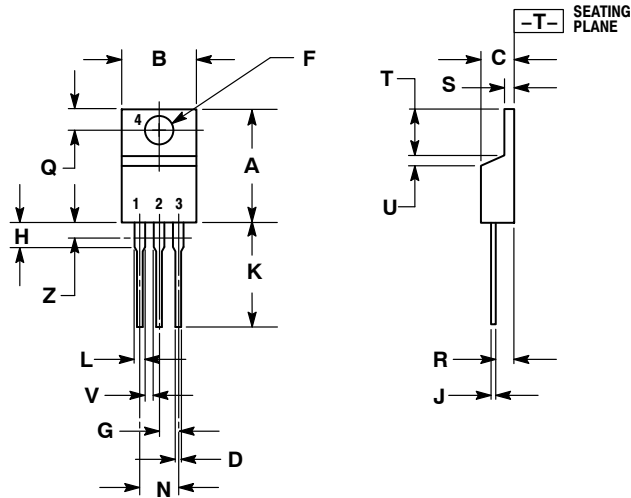
DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

# NGD15N41CL, NGD15N41ACL, NGB15N41CL, NGB15N41ACL, NGP15N41CL, NGP15N41ACL

## PACKAGE DIMENSIONS

TO-220  
CASE 221A-09  
ISSUE AF



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION Z DEFINES A ZONE WHERE ALL BODY AND LEAD IRREGULARITIES ARE ALLOWED.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.570	0.620	14.48	15.75
B	0.380	0.405	9.66	10.28
C	0.160	0.190	4.07	4.82
D	0.025	0.035	0.64	0.88
F	0.142	0.161	3.61	4.09
G	0.095	0.105	2.42	2.66
H	0.110	0.155	2.80	3.93
J	0.014	0.025	0.36	0.64
K	0.500	0.562	12.70	14.27
L	0.045	0.060	1.15	1.52
N	0.190	0.210	4.83	5.33
Q	0.100	0.120	2.54	3.04
R	0.080	0.110	2.04	2.79
S	0.045	0.055	1.15	1.39
T	0.235	0.255	5.97	6.47
U	0.000	0.050	0.00	1.27
V	0.045	---	1.15	---
Z	---	0.080	---	2.04

STYLE 9:

- PIN 1. GATE  
2. COLLECTOR  
3. EMITTER  
4. COLLECTOR

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**

Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free  
USA/Canada  
**Europe, Middle East and Africa Technical Support:**  
Phone: 421 33 790 2910  
**Japan Customer Focus Center**  
Phone: 81-3-5817-1050



**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)

**Order Literature:** <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

-  [View NGD15N41ACLT4G on WIN SOURCE](#)
-  [Littelfuse Inc. Information](#)

## Optimize Your Supply Chain with WIN SOURCE Solutions

-  Global Sourcing Solution
-  Obsolete Management
-  Cost Control Management
-  Shortage Management
-  Alternative Solution
-  Excess Inventory Management