



**THE DATASHEET OF  
HUFA76429P3**



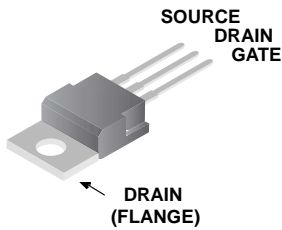
**44A, 60V, 0.025 Ohm, N-Channel, Logic Level UltraFET® Power MOSFETs**



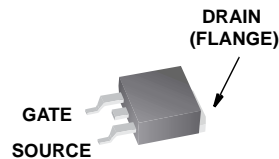
**Packaging**

JEDEC TO-220AB

JEDEC TO-263AB

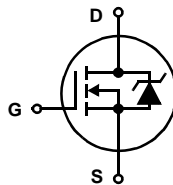


HUFA76429P3



HUFA76429S3S

**Symbol**



**Features**

- Ultra Low On-Resistance
  - $r_{DS(ON)} = 0.022\Omega, V_{GS} = 10V$
  - $r_{DS(ON)} = 0.025\Omega, V_{GS} = 5V$
- Simulation Models
  - Temperature Compensated PSPICE® and SABER™ Electrical Models
  - Spice and SABER Thermal Impedance Models
  - www.fairchildsemi.com
- Peak Current vs Pulse Width Curve
- UIS Rating Curve
- Switching Time vs  $R_{GS}$  Curves

**Ordering Information**

PART NUMBER	PACKAGE	BRAND
HUFA76429P3	TO-220AB	76429P
HUFA76429S3S	TO-263AB	76429S

NOTE: When ordering, use the entire part number. Add the suffix T to obtain the variant in tape and reel, e.g., HUFA76429S3ST.

**Absolute Maximum Ratings**  $T_C = 25^\circ C$ , Unless Otherwise Specified

	HUFA76429P3, HUFA76429S3S	UNITS
Drain to Source Voltage (Note 1) . . . . .	$V_{DSS}$ 60	V
Drain to Gate Voltage ( $R_{GS} = 20k\Omega$ ) (Note 1) . . . . .	$V_{DGR}$ 60	V
Gate to Source Voltage . . . . .	$V_{GS}$ $\pm 16$	V
Drain Current		
Continuous ( $T_C = 25^\circ C, V_{GS} = 5V$ ) . . . . .	$I_D$ 44	A
Continuous ( $T_C = 25^\circ C, V_{GS} = 10V$ ) (Figure 2) . . . . .	$I_D$ 47	A
Continuous ( $T_C = 100^\circ C, V_{GS} = 5V$ ) . . . . .	$I_D$ 31	A
Continuous ( $T_C = 100^\circ C, V_{GS} = 4.5V$ ) (Figure 2) . . . . .	$I_D$ 30	A
Pulsed Drain Current . . . . .	$I_{DM}$ Figure 4	
Pulsed Avalanche Rating . . . . .	UIS Figures 6, 17, 18	
Power Dissipation . . . . .	$P_D$ 110	W
Derate Above $25^\circ C$ . . . . .	0.74	W/ $^\circ C$
Operating and Storage Temperature . . . . .	$T_J, T_{STG}$ -55 to 175	$^\circ C$
Maximum Temperature for Soldering		
Leads at 0.063in (1.6mm) from Case for 10s . . . . .	$T_L$ 300	$^\circ C$
Package Body for 10s, See Techbrief TB334 . . . . .	$T_{pkg}$ 260	$^\circ C$

NOTES:

1.  $T_J = 25^\circ C$  to  $150^\circ C$ .

**CAUTION:** Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

This product has been designed to meet the extreme test conditions and environment demanded by the automotive industry. For a copy of the requirements, see AEC Q101 at: <http://www.aecouncil.com/>

Reliability data can be found at: <http://www.fairchildsemi.com/products/discrete/reliability/index.html>.

All Fairchild semiconductor products are manufactured, assembled and tested under ISO9000 and QS9000 quality systems certification.

## HUFA76429P3, HUFA76429S3S

### Electrical Specifications $T_C = 25^\circ\text{C}$ , Unless Otherwise Specified

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS	
<b>OFF STATE SPECIFICATIONS</b>							
Drain to Source Breakdown Voltage	BV <sub>DSS</sub>	I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V (Figure 12)	60	-	-	V	
		I <sub>D</sub> = 250μA, V <sub>GS</sub> = 0V, T <sub>C</sub> = -40°C (Figure 12)	55	-	-	V	
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = 55V, V <sub>GS</sub> = 0V	-	-	1	μA	
		V <sub>DS</sub> = 50V, V <sub>GS</sub> = 0V, T <sub>C</sub> = 150°C	-	-	250	μA	
Gate to Source Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±16V	-	-	±100	nA	
<b>ON STATE SPECIFICATIONS</b>							
Gate to Source Threshold Voltage	V <sub>GS(TH)</sub>	V <sub>GS</sub> = V <sub>DS</sub> , I <sub>D</sub> = 250μA (Figure 11)	1	-	3	V	
Drain to Source On Resistance	r <sub>DS(ON)</sub>	I <sub>D</sub> = 47A, V <sub>GS</sub> = 10V (Figures 9, 10)	-	0.018	0.022	Ω	
		I <sub>D</sub> = 31A, V <sub>GS</sub> = 5V (Figure 9)	-	0.021	0.025	Ω	
		I <sub>D</sub> = 30A, V <sub>GS</sub> = 4.5V (Figure 9)	-	0.022	0.027	Ω	
<b>THERMAL SPECIFICATIONS</b>							
Thermal Resistance Junction to Case	R <sub>θJC</sub>	TO-220 and TO-263	-	-	1.36	°C/W	
Thermal Resistance Junction to Ambient	R <sub>θJA</sub>		-	-	62	°C/W	
<b>SWITCHING SPECIFICATIONS (V<sub>GS</sub> = 4.5V)</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>DD</sub> = 30V, I <sub>D</sub> = 30A V <sub>GS</sub> = 4.5V, R <sub>GS</sub> = 7.5Ω (Figures 15, 21, 22)	-	-	325	ns	
Turn-On Delay Time	t <sub>d(ON)</sub>		-	13	-	ns	
Rise Time	t <sub>r</sub>		-	203	-	ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>		-	30	-	ns	
Fall Time	t <sub>f</sub>		-	74	-	ns	
Turn-Off Time	t <sub>OFF</sub>		-	-	155	ns	
<b>SWITCHING SPECIFICATIONS (V<sub>GS</sub> = 10V)</b>							
Turn-On Time	t <sub>ON</sub>	V <sub>DD</sub> = 30V, I <sub>D</sub> = 47A V <sub>GS</sub> = 10V, R <sub>GS</sub> = 8.2Ω (Figures 16, 21, 22)	-	-	160	ns	
Turn-On Delay Time	t <sub>d(ON)</sub>		-	7.8	-	ns	
Rise Time	t <sub>r</sub>		-	100	-	ns	
Turn-Off Delay Time	t <sub>d(OFF)</sub>		-	51	-	ns	
Fall Time	t <sub>f</sub>		-	104	-	ns	
Turn-Off Time	t <sub>OFF</sub>		-	-	235	ns	
<b>GATE CHARGE SPECIFICATIONS</b>							
Total Gate Charge	Q <sub>g(TOT)</sub>	V <sub>GS</sub> = 0V to 10V	V <sub>DD</sub> = 30V, I <sub>D</sub> = 31A, I <sub>g(REF)</sub> = 1.0mA (Figures 14, 19, 20)	-	38	46	nC
Gate Charge at 5V	Q <sub>g(5)</sub>	V <sub>GS</sub> = 0V to 5V		-	21	25	nC
Threshold Gate Charge	Q <sub>g(TH)</sub>	V <sub>GS</sub> = 0V to 1V		-	1.3	1.6	nC
Gate to Source Gate Charge	Q <sub>gs</sub>			-	3.8	-	nC
Gate to Drain "Miller" Charge	Q <sub>gd</sub>			-	9.7	-	nC
<b>CAPACITANCE SPECIFICATIONS</b>							
Input Capacitance	C <sub>ISS</sub>	V <sub>DS</sub> = 25V, V <sub>GS</sub> = 0V, f = 1MHz (Figure 13)	-	1480	-	pF	
Output Capacitance	C <sub>OSS</sub>		-	440	-	pF	
Reverse Transfer Capacitance	C <sub>RSS</sub>		-	90	-	pF	

### Source to Drain Diode Specifications

PARAMETER	SYMBOL	TEST CONDITIONS	MIN	TYP	MAX	UNITS
Source to Drain Diode Voltage	V <sub>SD</sub>	I <sub>SD</sub> = 44A	-	-	1.25	V
		I <sub>SD</sub> = 22A	-	-	1.00	V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>SD</sub> = 31A, dI <sub>SD</sub> /dt = 100A/μs	-	-	98	ns
Reverse Recovered Charge	Q <sub>RR</sub>	I <sub>SD</sub> = 31A, dI <sub>SD</sub> /dt = 100A/μs	-	-	230	nC

Typical Performance Curves

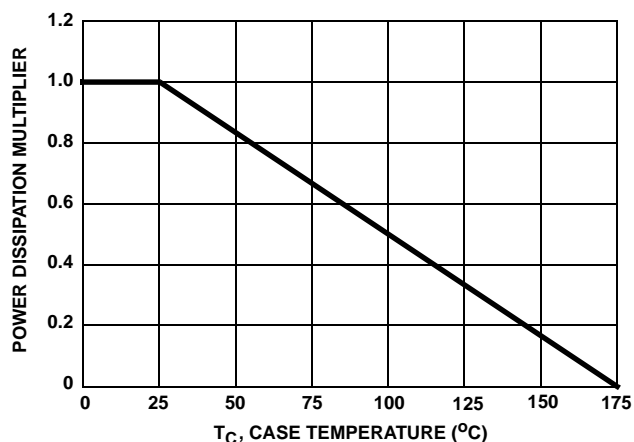


FIGURE 1. NORMALIZED POWER DISSIPATION vs CASE TEMPERATURE

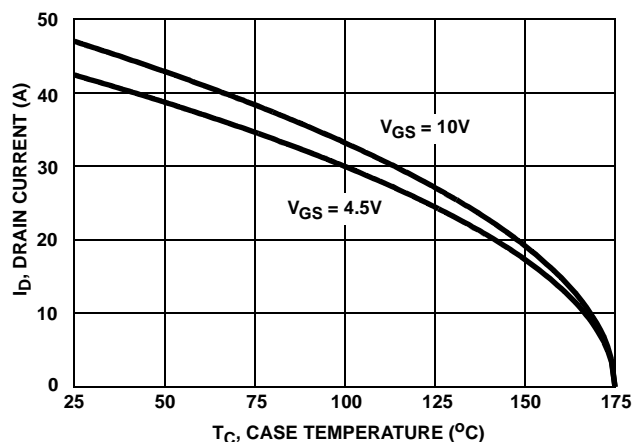


FIGURE 2. MAXIMUM CONTINUOUS DRAIN CURRENT vs CASE TEMPERATURE

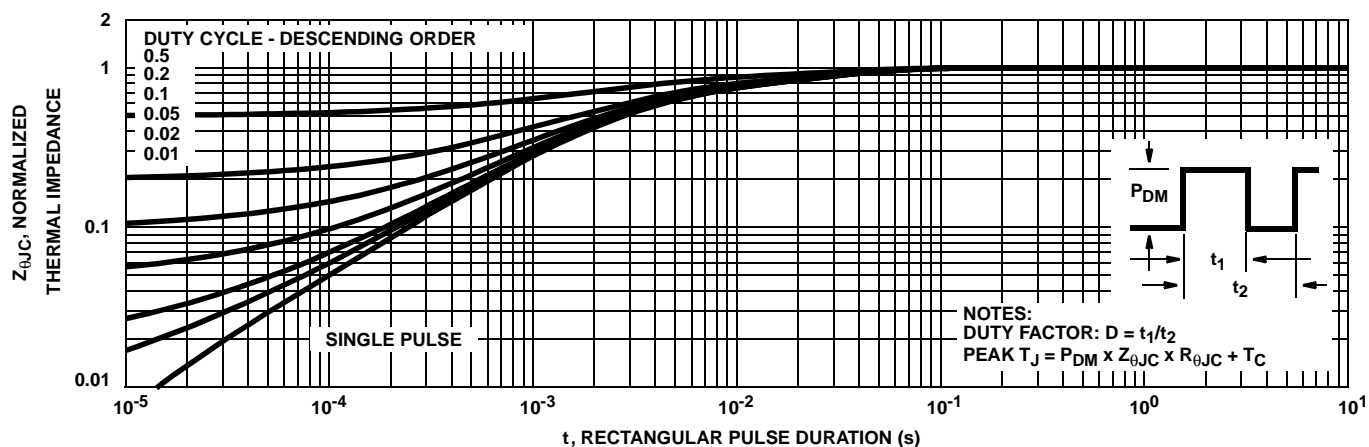


FIGURE 3. NORMALIZED MAXIMUM TRANSIENT THERMAL IMPEDANCE

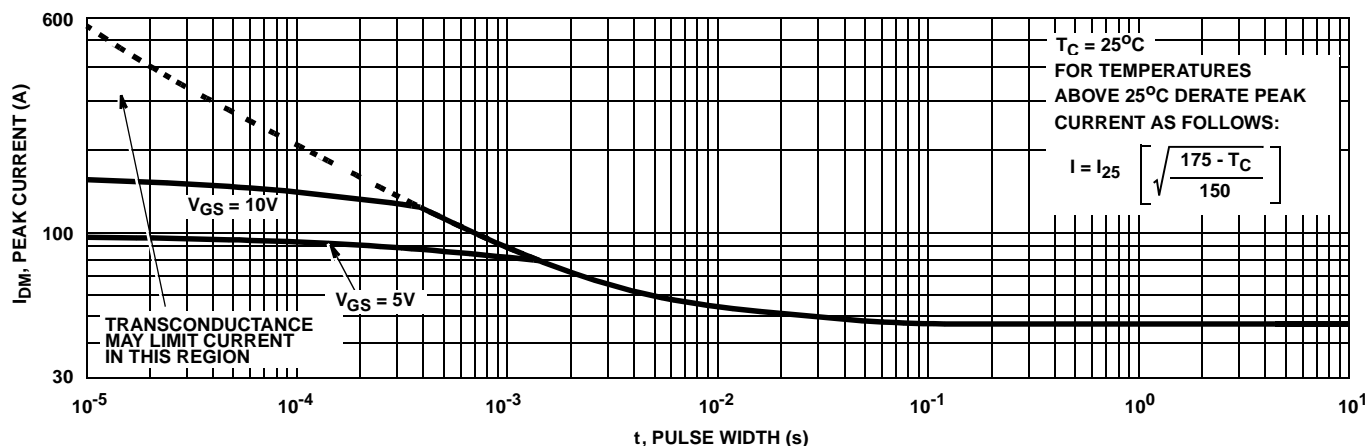


FIGURE 4. PEAK CURRENT CAPABILITY

Typical Performance Curves (Continued)

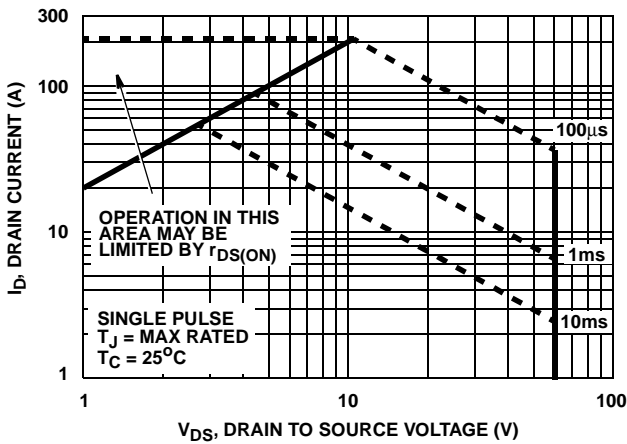
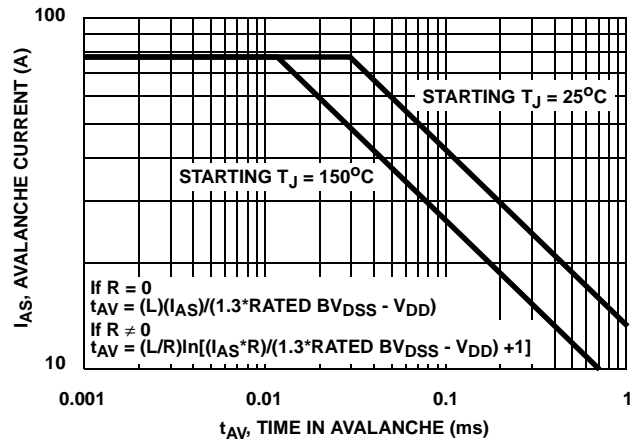


FIGURE 5. FORWARD BIAS SAFE OPERATING AREA



NOTE: Refer to Fairchild Application Notes AN9321 and AN9322.

FIGURE 6. UNCLAMPED INDUCTIVE SWITCHING CAPABILITY

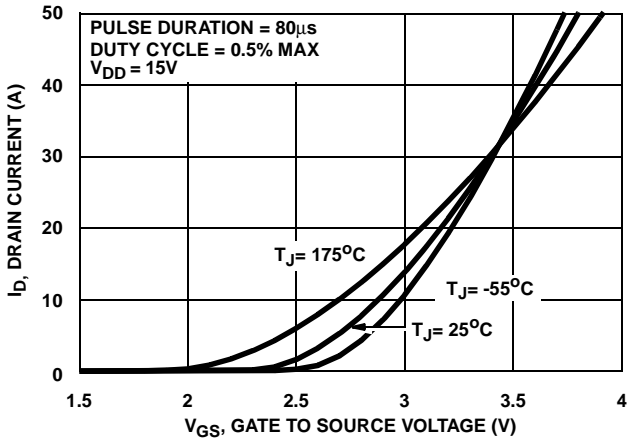


FIGURE 7. TRANSFER CHARACTERISTICS

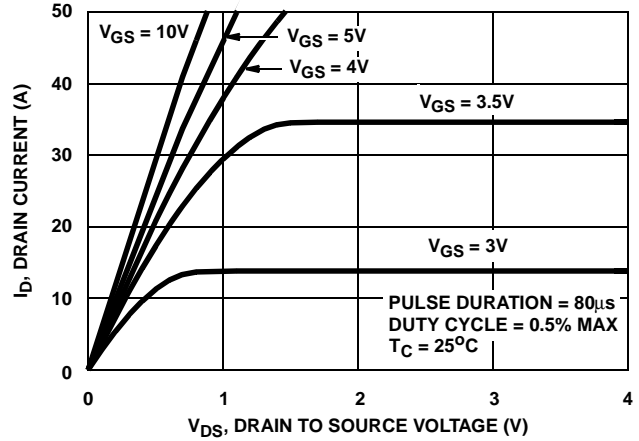


FIGURE 8. SATURATION CHARACTERISTICS

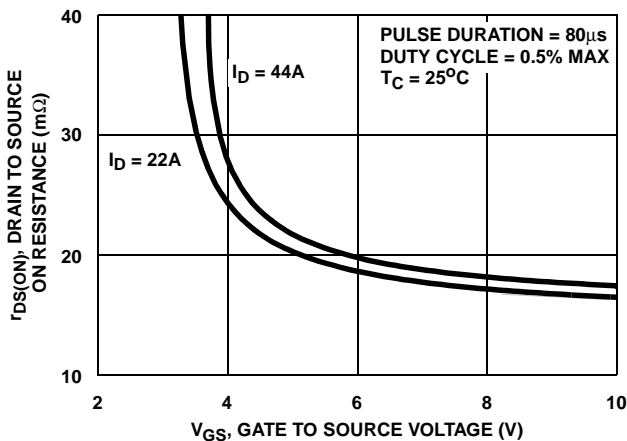


FIGURE 9. DRAIN TO SOURCE ON RESISTANCE vs. GATE VOLTAGE AND DRAIN CURRENT

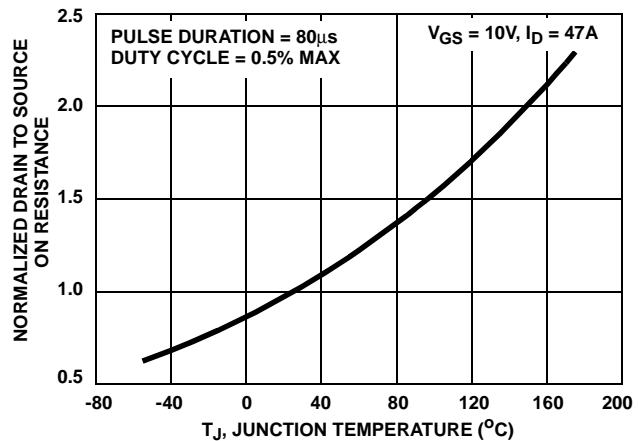


FIGURE 10. NORMALIZED DRAIN TO SOURCE ON RESISTANCE vs. JUNCTION TEMPERATURE

Typical Performance Curves (Continued)

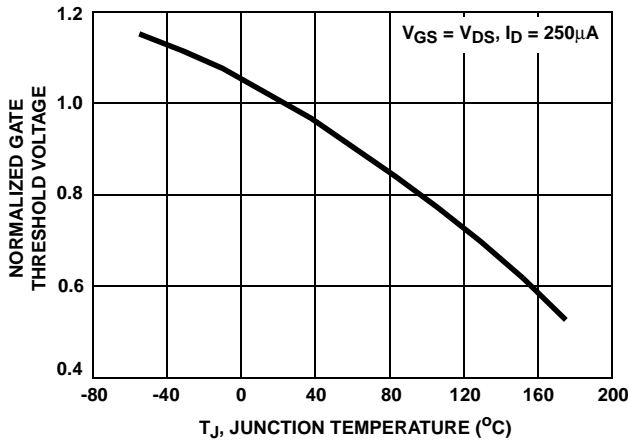


FIGURE 11. NORMALIZED GATE THRESHOLD VOLTAGE vs JUNCTION TEMPERATURE

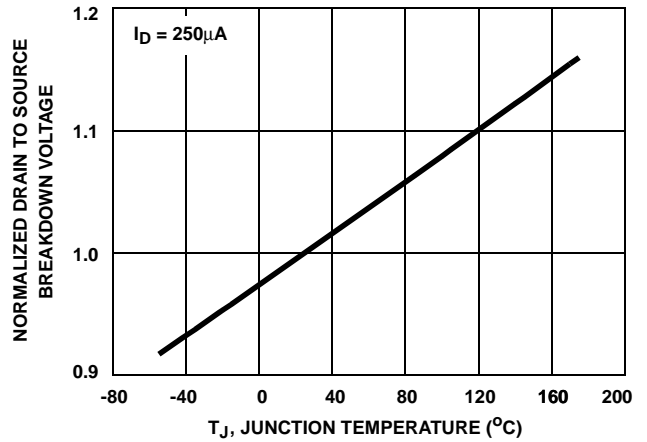


FIGURE 12. NORMALIZED DRAIN TO SOURCE BREAKDOWN VOLTAGE vs JUNCTION TEMPERATURE

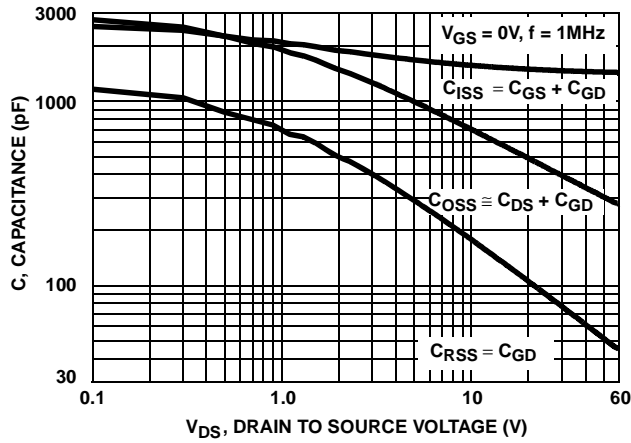
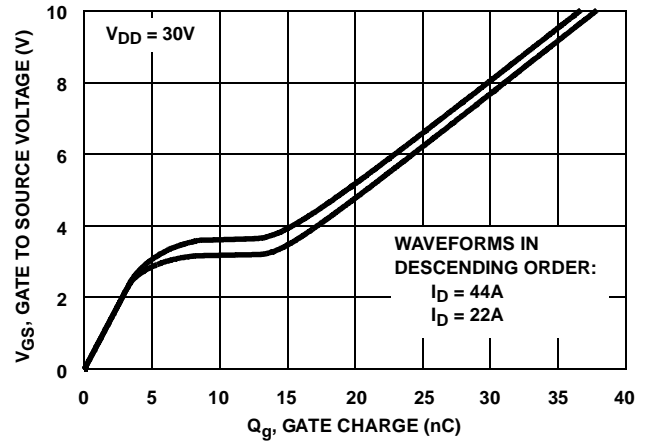


FIGURE 13. CAPACITANCE vs DRAIN TO SOURCE VOLTAGE



NOTE: Refer to Fairchild Application Notes AN7254 and AN7260.

FIGURE 14. GATE CHARGE WAVEFORMS FOR CONSTANT GATE CURRENT

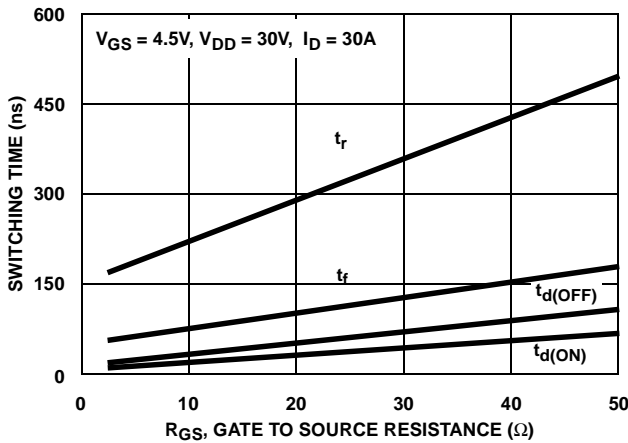


FIGURE 15. SWITCHING TIME vs GATE RESISTANCE

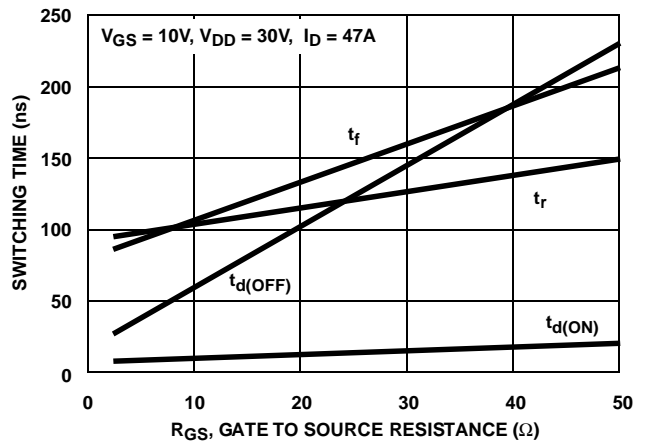


FIGURE 16. SWITCHING TIME vs GATE RESISTANCE

Test Circuits and Waveforms

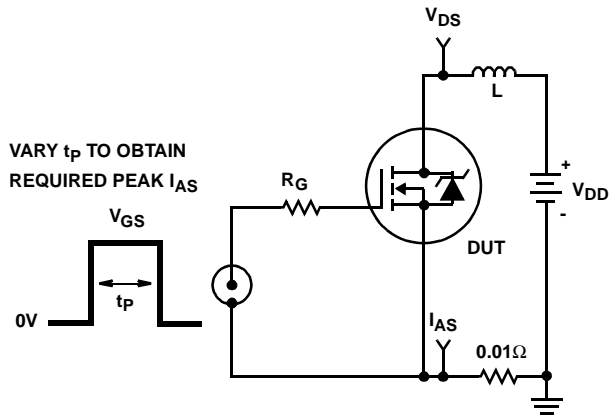


FIGURE 17. UNCLAMPED ENERGY TEST CIRCUIT

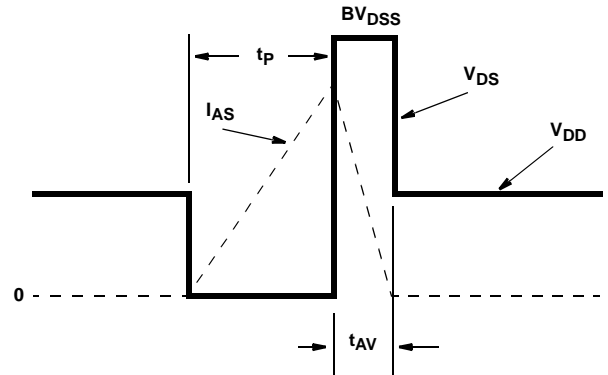


FIGURE 18. UNCLAMPED ENERGY WAVEFORMS

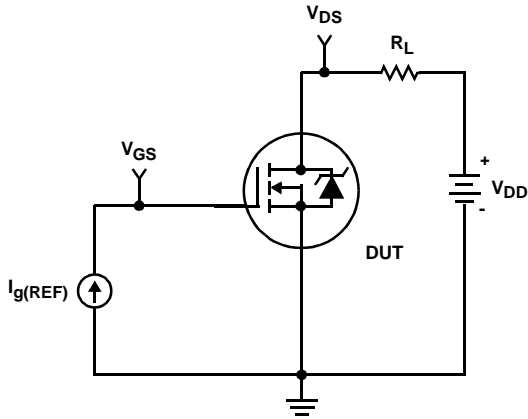


FIGURE 19. GATE CHARGE TEST CIRCUIT

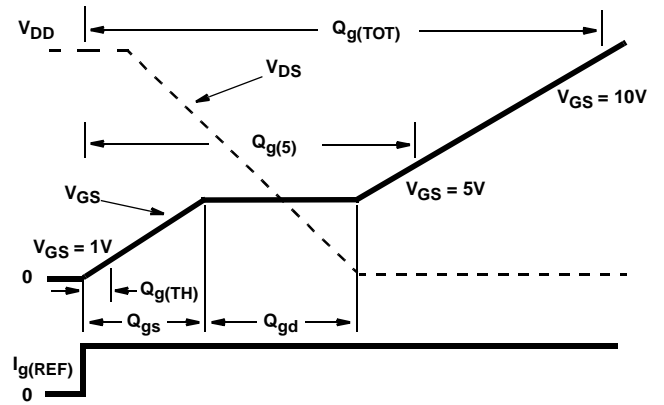


FIGURE 20. GATE CHARGE WAVEFORMS

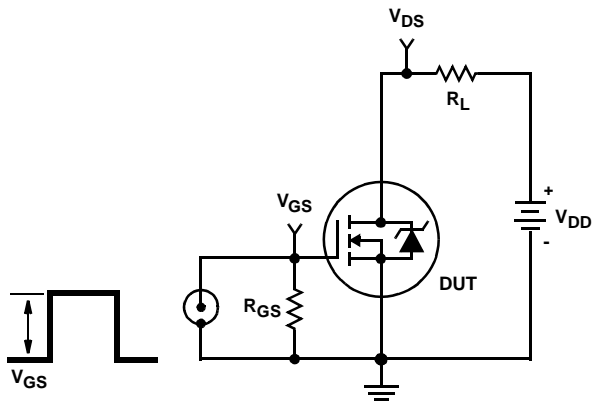


FIGURE 21. SWITCHING TIME TEST CIRCUIT

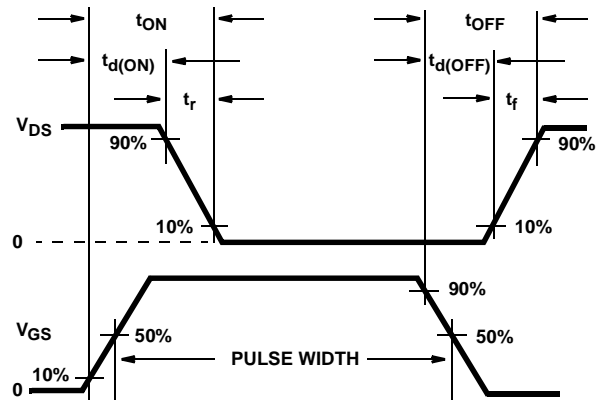


FIGURE 22. SWITCHING TIME WAVEFORM

**PSPICE Electrical Model**

.SUBCKT HUFA76429 2 1 3 ; rev 25 June 1999

CA 12 8 1.95e-9  
 CB 15 14 1.95e-9  
 CIN 6 8 1.39e-9

DBODY 7 5 DBODYMOD  
 DBREAK 5 11 DBREAKMOD  
 DPLCAP 10 5 DPLCAPMOD

EBREAK 11 7 17 18 68.05  
 EDS 14 8 5 8 1  
 EGS 13 8 6 8 1  
 ESG 6 10 6 8 1  
 EVTHRES 6 21 19 8 1  
 EVTEMP 20 6 18 22 1

IT 8 17 1

LDRAIN 2 5 1e-9  
 LGATE 1 9 5.80e-9  
 LSOURCE 3 7 4.57e-9

MMED 16 6 8 8 MMEDMOD  
 MSTRO 16 6 8 8 MSTROMOD  
 MWEAK 16 21 8 8 MWEAKMOD

RBREAK 17 18 RBREAKMOD 1  
 RDRAIN 50 16 RDRAINMOD 7.8e-3  
 RGATE 9 20 2.80  
 RLDRAIN 2 5 10  
 RLGATE 1 9 54.2  
 RLSOURCE 3 7 41.6  
 RSLC1 5 51 RSLCMOD 1e-6  
 RSLC2 5 50 1e3  
 RSOURCE 8 7 RSOURCEMOD 6.5e-3  
 RVTHRES 22 8 RVTHRESMOD 1  
 RVTEMP 18 19 RVTEMPMOD 1

S1A 6 12 13 8 S1AMOD  
 S1B 13 12 13 8 S1BMOD  
 S2A 6 15 14 13 S2AMOD  
 S2B 13 15 14 13 S2BMOD

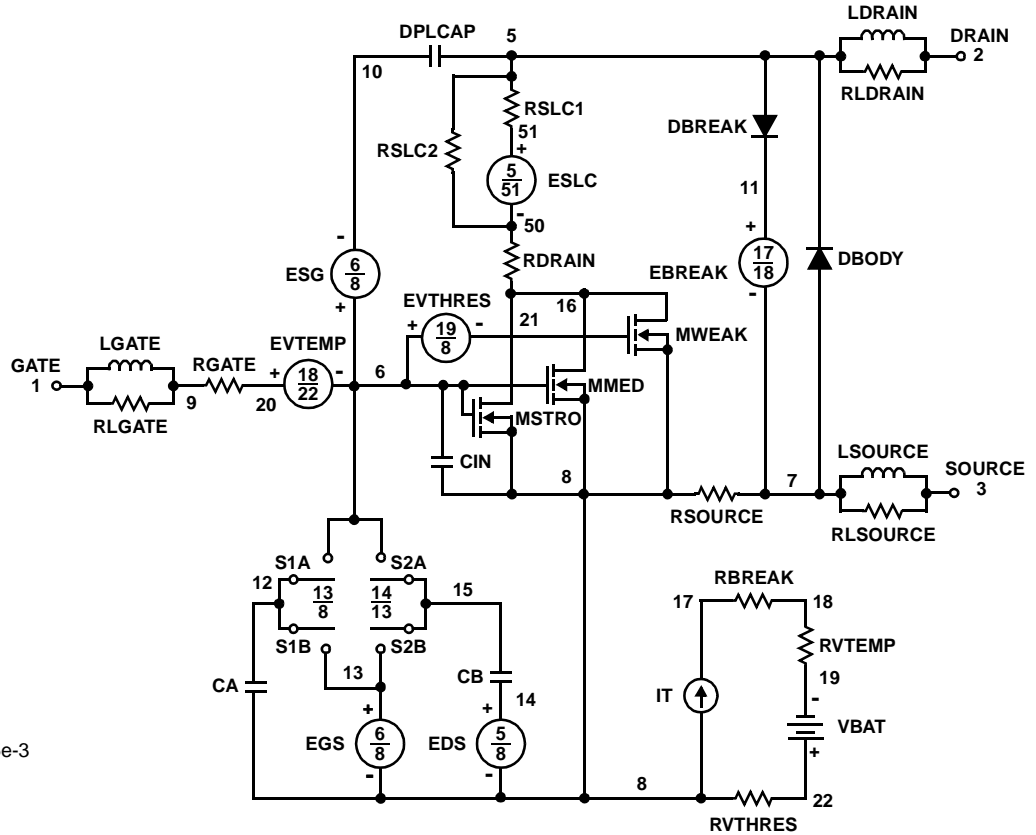
VBAT 22 19 DC 1

ESLC 51 50 VALUE={(V(5,51)/ABS(V(5,51)))\*(PWR(V(5,51))/(1e-6\*117),3))}

.MODEL DBODYMOD D (IS = 1.28e-12 IKF = 11.5 RS = 5.25e-3 TRS1 = 1.78e-3 TRS2 = 1.85e-6 CJO = 1.68e-9 TT = 6.14e-8 M = 0.48 XTI = 4.35)  
 .MODEL DBREAKMOD D (RS = 2.27e-1 TRS1 = 9.10e-4 TRS2 = -1e-6)  
 .MODEL DPLCAPMOD D (CJO = 1.23e-9 IS = 1e-3 ON = 10 M = 0.8)  
 .MODEL MMEDMOD NMOS (VTO = 1.98 KP = 3.2 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 2.80)  
 .MODEL MSTROMOD NMOS (VTO = 2.30 KP = 67 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u)  
 .MODEL MWEAKMOD NMOS (VTO = 1.72 KP = 0.08 IS = 1e-30 N = 10 TOX = 1 L = 1u W = 1u RG = 28.0 RS = 0.1)  
 .MODEL RBREAKMOD RES (TC1 = 1.08e-3 TC2 = 1.35e-7)  
 .MODEL RDRAINMOD RES (TC1 = 8.25e-3 TC2 = 1.85e-5)  
 .MODEL RSLCMOD RES (TC1 = 4.97e-3 TC2 = 5.05e-6)  
 .MODEL RSOURCEMOD RES (TC1 = 1.5e-3 TC2 = 1e-6)  
 .MODEL RVTHRESMOD RES (TC1 = -1.85e-3 TC2 = -9.48e-6)  
 .MODEL RVTEMPMOD RES (TC1 = -1.72e-3 TC2 = 9.50e-7)  
 .MODEL S1AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -6.2 VOFF = -2.4)  
 .MODEL S1BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -2.4 VOFF = -6.2)  
 .MODEL S2AMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = -1.1 VOFF = 0.5)  
 .MODEL S2BMOD VSWITCH (RON = 1e-5 ROFF = 0.1 VON = 0.5 VOFF = -1.1)

.ENDS

NOTE: For further discussion of the PSPICE model, consult **A New PSPICE Sub-Circuit for the Power MOSFET Featuring Global Temperature Options**; IEEE Power Electronics Specialist Conference Records, 1991, written by William J. Hepp and C. Frank Wheatley.





## SPICE Thermal Model

REV 2 August 1999

HUFA76429

CTHERM1 th 6 2.45e-3  
 CTHERM2 6 5 8.15e-3  
 CTHERM3 5 4 7.40e-3  
 CTHERM4 4 3 7.45e-3  
 CTHERM5 3 2 1.01e-2  
 CTHERM6 2 tl 7.49e-2

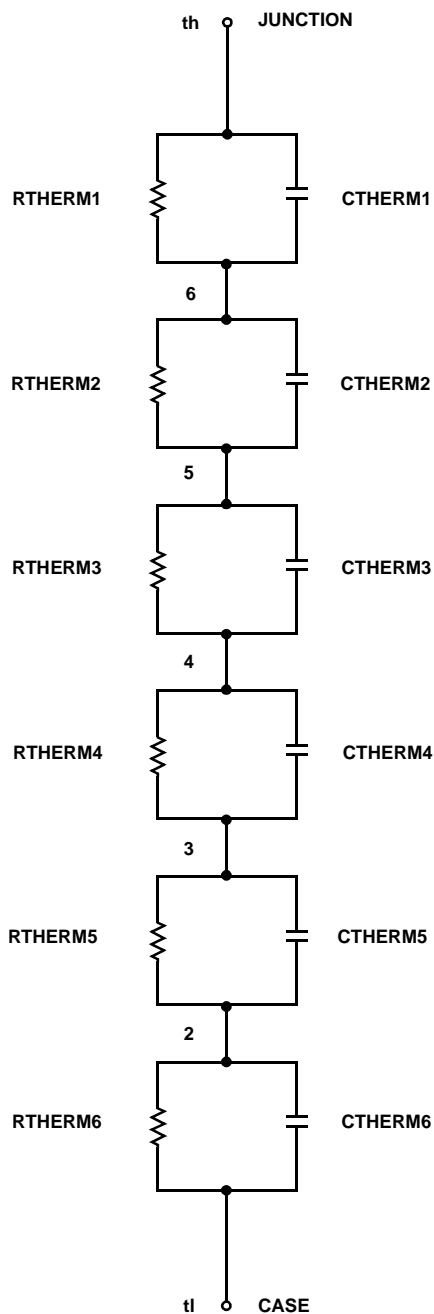
RTHERM1 th 6 9.00e-3  
 RTHERM2 6 5 1.80e-2  
 RTHERM3 5 4 9.15e-2  
 RTHERM4 4 3 2.43e-1  
 RTHERM5 3 2 3.50e-1  
 RTHERM6 2 tl 3.62e-1

## SABER Thermal Model

SABER thermal model HUFA76429

```
template thermal_model th tl
thermal_c th, tl
{
    ctherm.ctherm1 th 6 = 2.45e-3
    ctherm.ctherm2 6 5 = 8.15e-3
    ctherm.ctherm3 5 4 = 7.40e-3
    ctherm.ctherm4 4 3 = 7.45e-3
    ctherm.ctherm5 3 2 = 1.01e-2
    ctherm.ctherm6 2 tl = 7.49e-2
```

```
rtherm.rtherm1 th 6 = 9.00e-3
rtherm.rtherm2 6 5 = 1.80e-2
rtherm.rtherm3 5 4 = 9.15e-2
rtherm.rtherm4 4 3 = 2.43e-1
rtherm.rtherm5 3 2 = 3.50e-1
rtherm.rtherm6 2 tl = 3.62e-1
}
```



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Bottomless <sup>TM</sup>	FAST <sub>r</sub> <sup>TM</sup>	OPTOPLANAR <sup>TM</sup>	STAR*POWER <sup>TM</sup>	
CoolFET <sup>TM</sup>	FRFET <sup>TM</sup>	PACMAN <sup>TM</sup>	Stealth <sup>TM</sup>	
CROSSVOLT <sup>TM</sup>	GlobalOptoisolator <sup>TM</sup>	POP <sup>TM</sup>	SuperSOT <sup>TM</sup> -3	
DenseTrench <sup>TM</sup>	GTO <sup>TM</sup>	Power247 <sup>TM</sup>	SuperSOT <sup>TM</sup> -6	
DOMET <sup>TM</sup>	HiSeC <sup>TM</sup>	PowerTrench <sup>®</sup>	SuperSOT <sup>TM</sup> -8	
EcoSPARK <sup>TM</sup>	ISOPLANAR <sup>TM</sup>	QFET <sup>TM</sup>	SyncFET <sup>TM</sup>	
E <sup>2</sup> CMOS <sup>TM</sup>	LittleFET <sup>TM</sup>	QS <sup>TM</sup>	TinyLogic <sup>TM</sup>	
EnSigna <sup>TM</sup>	MicroFET <sup>TM</sup>	QT Optoelectronics <sup>TM</sup>	TruTranslation <sup>TM</sup>	
FACT <sup>TM</sup>	MicroPak <sup>TM</sup>	Quiet Series <sup>TM</sup>	UHC <sup>TM</sup>	
FACT Quiet Series <sup>TM</sup>	MICROWIRE <sup>TM</sup>	SILENT SWITCHER <sup>®</sup>	UltraFET <sup>®</sup>	

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As used herein:

1. Life support devices or systems are devices or systems which, (a) are intended for surgical implant into the body, or (b) support or sustain life, or (c) whose failure to perform when properly used in accordance with instructions for use provided in the labeling, can be reasonably expected to result in significant injury to the user.
2. A critical component is any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

## PRODUCT STATUS DEFINITIONS

### Definition of Terms

Datasheet Identification	Product Status	Definition
Advance Information	Formative or In Design	This datasheet contains the design specifications for product development. Specifications may change in any manner without notice.
Preliminary	First Production	This datasheet contains preliminary data, and supplementary data will be published at a later date. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
No Identification Needed	Full Production	This datasheet contains final specifications. Fairchild Semiconductor reserves the right to make changes at any time without notice in order to improve design.
Obsolete	Not In Production	This datasheet contains specifications on a product that has been discontinued by Fairchild semiconductor. The datasheet is printed for reference information only.

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