To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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MOS FIELD EFFECT TRANSISTOR
NP36P06SLG

SWITCHING
P-CHANNEL POWER MOSFET

DESCRIPTION

The NP36P06SLG is P-channel MOS Field Effect Transistor designed for high current switching applications.

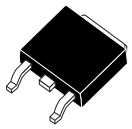
ORDERING INFORMATION

PART NUMBER	PACKAGE
NP36P06SLG	TO-252 (MP-3ZK)

FEATURES

- Super low on-state resistance
  $R_{DS(on)1}$ = 30 mΩ MAX. (V_{GS} = –10 V, I_D = –18 A)
  $R_{DS(on)2}$ = 40 mΩ MAX. (V_{GS} = –4.5 V, I_D = –18 A)
- Low input capacitance
  C_{iss} = 3200 pF TYP.
- Built-in gate protection diode

(TO-252)



ABSOLUTE MAXIMUM RATINGS (T_A = 25°C)

Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	–60	V
Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	∓20	V
Drain Current (DC) (T_C = 25°C)	$I_{D(DC)}$	∓36	A
Drain Current (pulse) Note1	$I_{D(pulse)}$	∓108	A
Total Power Dissipation (T_C = 25°C)	P_{T1}	56	W
Total Power Dissipation (T_A = 25°C)	P_{T2}	1.2	W
Channel Temperature	T_{ch}	175	°C
Storage Temperature	T_{stg}	–55 to +175	°C
Single Avalanche Current Note2	I_{AS}	23.4	A
Single Avalanche Energy Note2	E_{AS}	54.8	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Starting T_{ch} = 25°C, V_{DD} = –30 V, R_G = 25 Ω, V_{GS} = –20 → 0 V

THERMAL RESISTANCE

Channel to Case Thermal Resistance	$R_{th(ch-C)}$	2.68	°C/W
Channel to Ambient Thermal Resistance	$R_{th(ch-A)}$	125	°C/W

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Date Published November 2007 NS
Printed in Japan

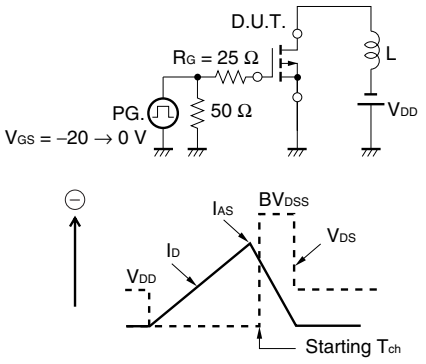
The mark <R> shows major revised points.
The revised points can be easily searched by copying an "<R>" in the PDF file and specifying it in the "Find what:" field.

ELECTRICAL CHARACTERISTICS (T_A = 25°C)

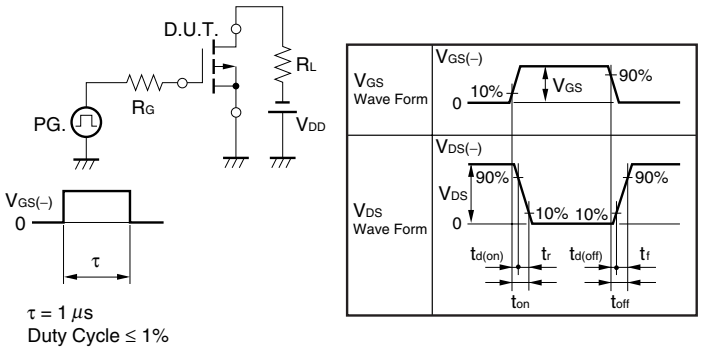
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓20 V, V_{DS} = 0 V			∓10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0	–2.0	–2.5	V
Forward Transfer Admittance Note	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –18 A	12			S
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –18 A		24	30	mΩ
	$R_{DS(on)2}$	V_{GS} = –4.5 V, I_D = –18 A		27	40	mΩ
Input Capacitance	C_{iss}	V_{DS} = –10 V,		3200		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V,		350		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		205		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –30 V, I_D = –18 A,		7		ns
Rise Time	t_r	V_{GS} = –10 V,		12		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 0 Ω		190		ns
Fall Time	t_f			110		ns
Total Gate Charge	Q_G	V_{DD} = –48 V,		52		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V,		6.9		nC
Gate to Drain Charge	Q_{GD}	I_D = –36 A		15		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	I_F = –36 A, V_{GS} = 0 V			1.2	V
Reverse Recovery Time	t_{rr}	I_F = –36 A, V_{GS} = 0 V,		46		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		75		nC

Note Pulsed test PW ≤ 350 μs, Duty Cycle ≤ 2%

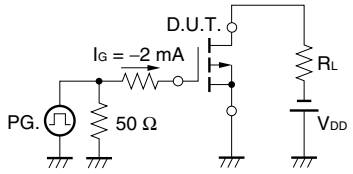
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME

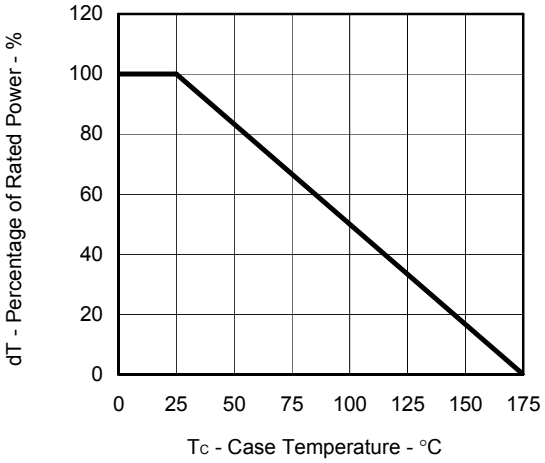


TEST CIRCUIT 3 GATE CHARGE

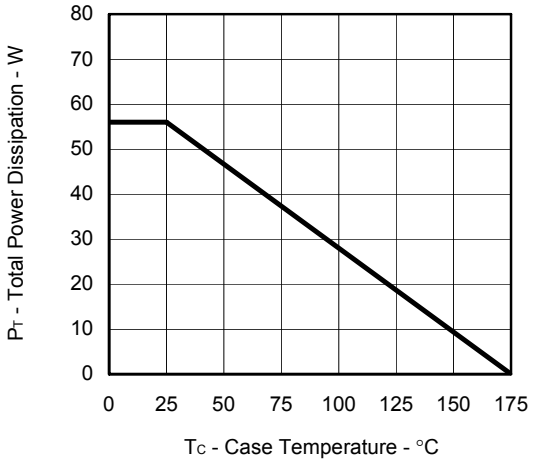


TYPICAL CHARACTERISTICS (T_A = 25°C)

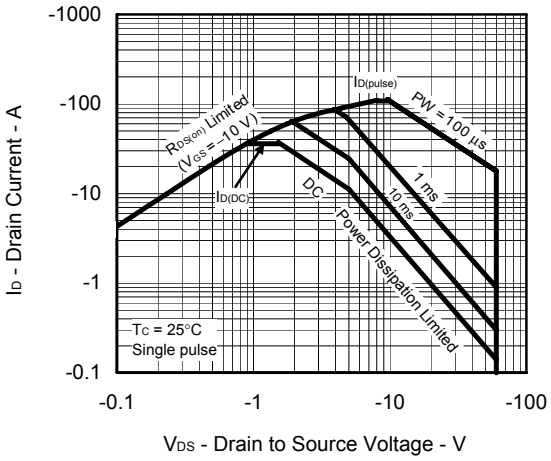
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



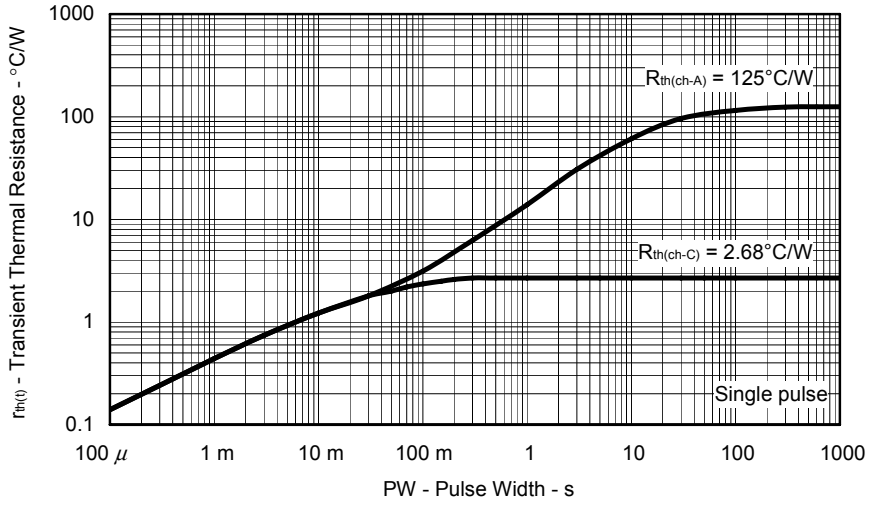
TOTAL POWER DISSIPATION vs. CASE TEMPERATURE



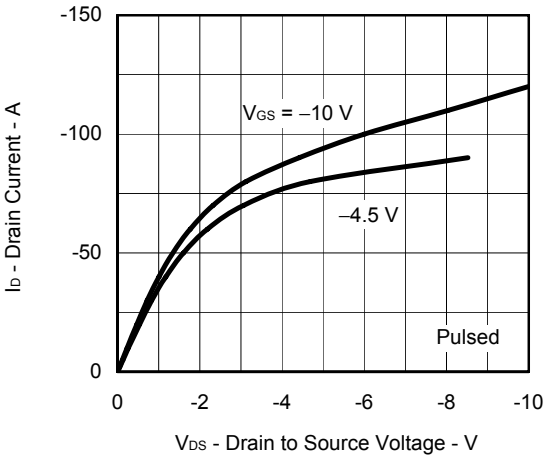
FORWARD BIAS SAFE OPERATING AREA



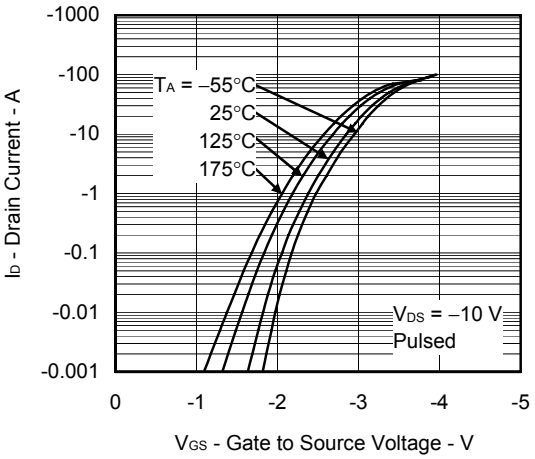
<R> TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



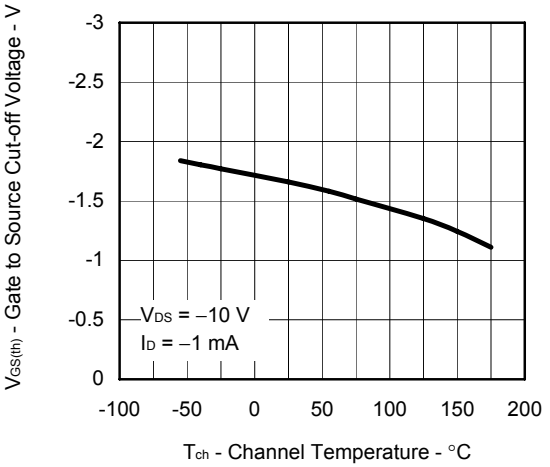
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



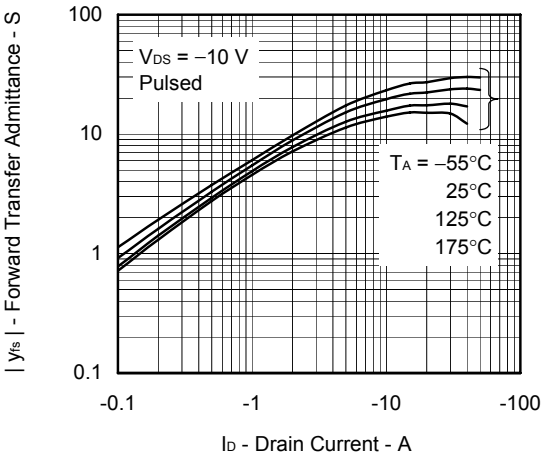
FORWARD TRANSFER CHARACTERISTICS



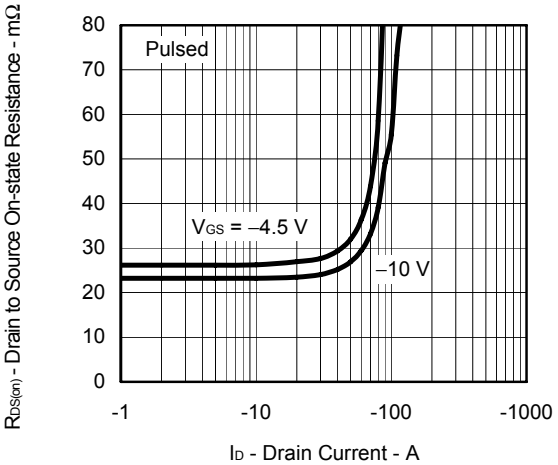
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



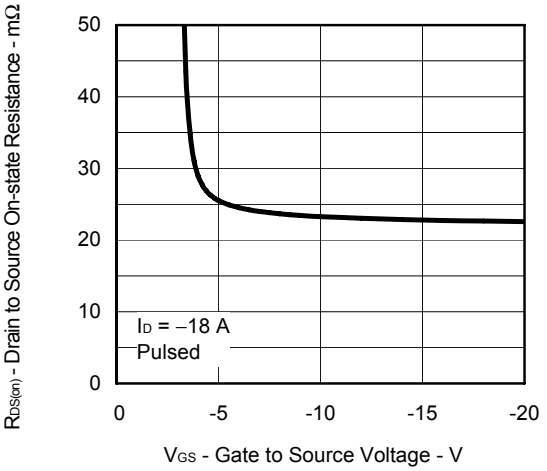
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



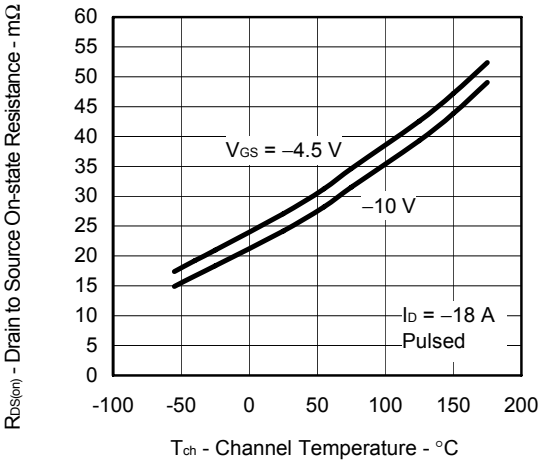
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
DRAIN CURRENT



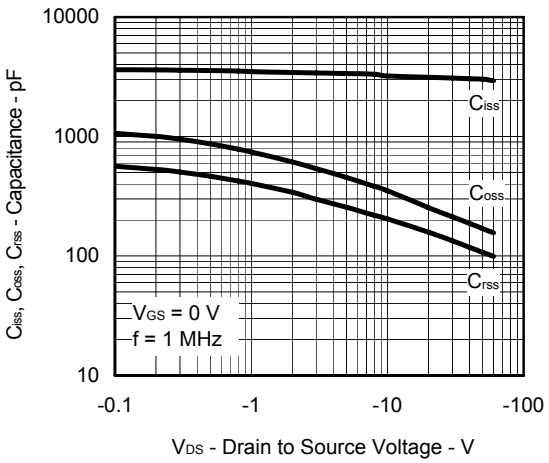
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



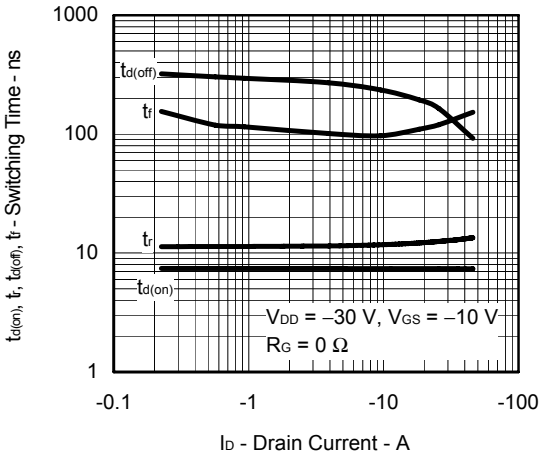
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



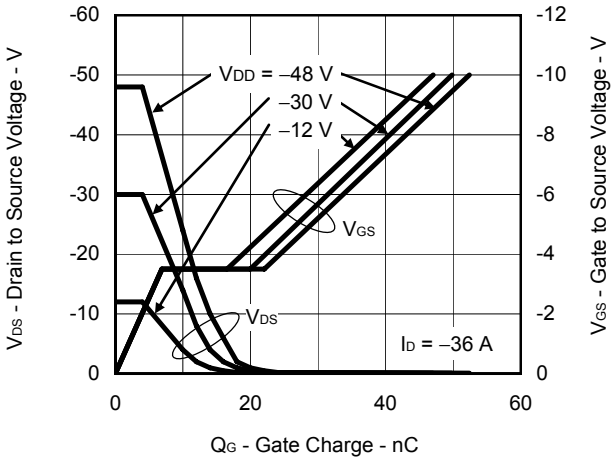
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



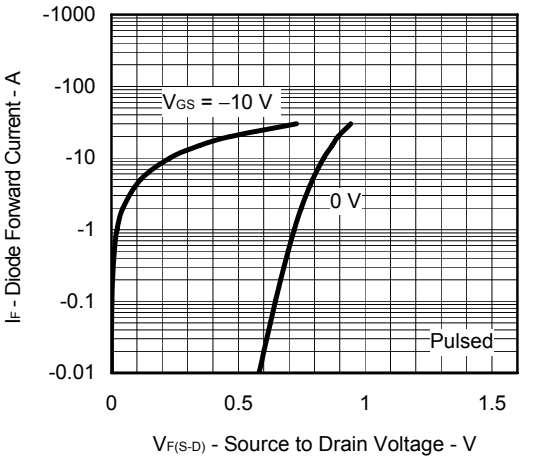
SWITCHING CHARACTERISTICS



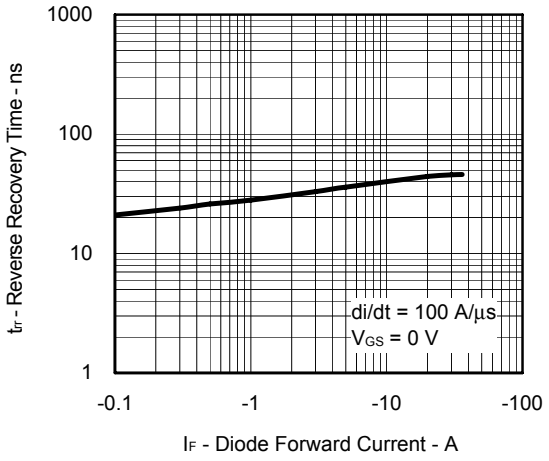
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

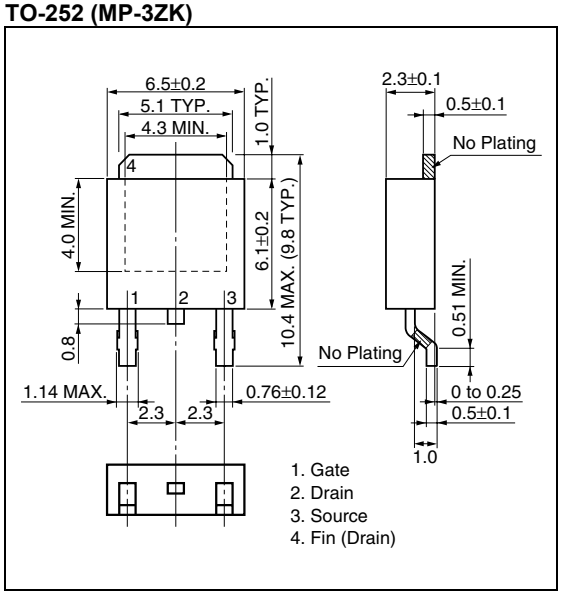


REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT

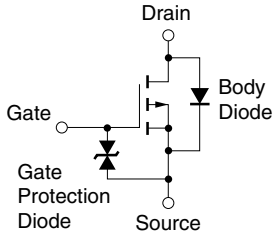


PACKAGE DRAWING (Unit: mm)

TO-252 (MP-3ZK)



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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