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# FSA3357

## Low Voltage SP3T Analog Switch (3:1 Multiplexer/Demultiplexer)

### General Description

The FSA3357 is a high performance, single-pole/triple-throw (SP3T) Analog Switch or 3:1 Multiplexer/Demultiplexer. The device is fabricated with advanced sub-micron CMOS technology to achieve high speed enable and disable times and low On Resistance. The break before make select circuitry prevents disruption of signals on the B<sub>0</sub>, B<sub>1</sub>, or B<sub>2</sub> Ports due to the switches temporarily being enabled during select pin switching. The device is specified to operate over the 1.65 to 5.5V V<sub>CC</sub> operating range. The control input tolerates voltages up to 5.5V independent of the V<sub>CC</sub> operating range.

### Features

- Useful in both analog and digital applications
- Space saving US8 8-lead surface mount package
- Low On Resistance; < 9Ω on typ @ 3.3V V<sub>CC</sub>
- Broad V<sub>CC</sub> operating range; 1.65V to 5.5V
- Rail-to-Rail signal handling
- Power down high impedance control input
- Overvoltage tolerance of control input to 7.0V
- Break before make enable circuitry
- 250 MHz - 3dB bandwidth
- Space saving Pb-Free MicroPak™ packaging

### Applications

- Cell Phone
- PDA
- Video

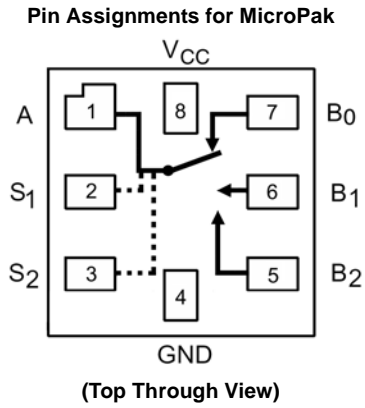
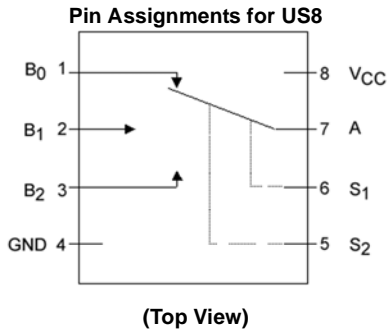
### Ordering Code:

Product Order Number	Package Number	Code Top Mark	Package Description	Supplied As
FSA3357K8X	MAB08A	A357	8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide	3k Units on Tape and Reel
FSA3357L8X	MAC08A	FE	Pb-Free 8-Lead MicroPak, 1.6 mm Wide	5k Units on Tape and Reel

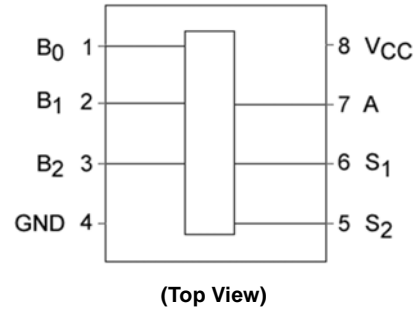
Pb-Free package per JEDEC J-STD-020B.

MicroPak™ is a trademark of Fairchild Semiconductor Corporation.

### Analog Symbols



### Connection Diagram



### Pin Descriptions

Pin Names	Description
A <sub>1</sub> , B <sub>0</sub> , B <sub>1</sub> , B <sub>2</sub>	Data Ports
S <sub>1</sub> , S <sub>2</sub>	Control Input

### Function Table

S <sub>1</sub>	S <sub>2</sub>	Function
0	0	No Connection
1	0	B <sub>0</sub> Connected to A
0	1	B <sub>1</sub> Connected to A
1	1	B <sub>2</sub> Connected to A

**Absolute Maximum Ratings**(Note 1)

Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V
DC Switch Voltage ( $V_S$ ) (Note 2)	-0.5V to $V_{CC}$ +0.5V
DC Input Voltage ( $V_{IN}$ ) (Note 2)	-0.5V to +7.0V
DC Input Diode Current ( $I_{IK}$ )	
@ ( $I_{IK}$ ) $V_{IN} < 0V$	-50 mA
DC Output Current ( $I_{OUT}$ )	128 mA
DC $V_{CC}$ or Ground Current ( $I_{CC}/I_{GND}$ )	±100 mA
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C
Junction Temperature under Bias ( $T_J$ )	150°C
Junction Lead Temperature ( $T_L$ )	
(Soldering, 10 seconds)	260°C
Power Dissipation ( $P_D$ ) @ +85°C	180 mW

**Recommended Operating Conditions**

(Note 3)

Supply Voltage Operating ( $V_{CC}$ )	1.65V to 5.5V
Control Input Voltage ( $V_{IN}$ )	0V to $V_{CC}$
Switch Input Voltage ( $V_{IN}$ )	0V to $V_{CC}$
Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Operating Temperature ( $T_A$ )	-40°C to +85°C
Input Rise and Fall Time ( $t_r, t_f$ )	
Control Input $V_{CC} = 2.3V - 3.6V$	0 ns/V to 10 ns/V
Control Input $V_{CC} = 4.5V - 5.5V$	0 ns/V to 5 ns/V
Thermal Resistance ( $\theta_{JA}$ )	250°C/W
MicroPak 8L Package	224°C/W

**Note 1:** Absolute maximum ratings are DC values beyond which the device may be damaged or have its useful life impaired. The datasheet specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside datasheet specifications.

**Note 2:** The input and output negative voltage ratings may be exceeded if the input and output diode current ratings are observed.

**Note 3:** Control inputs must be held HIGH or LOW, they must not float.

**DC Electrical Characteristics**

Symbol	Parameter	$V_{CC}$ (V)	$T_A = +25^\circ\text{C}$			$T_A = -40^\circ\text{C to } +85^\circ\text{C}$		Units	Conditions			
			Min	Typ	Max	Min	Max					
$V_{IH}$	HIGH Level Input Voltage	1.65 – 1.95	0.75 $V_{CC}$			0.75 $V_{CC}$		V				
		2.3 – 5.5	0.7 $V_{CC}$			0.7 $V_{CC}$						
$V_{IL}$	LOW Level Input Voltage	1.65 – 1.95	0.25 $V_{CC}$			0.25 $V_{CC}$		V				
		2.3 – 5.5	0.3 $V_{CC}$			0.3 $V_{CC}$						
$I_{IN}$	Input Leakage Current	0 – 5.5	±0.1			±1.0		µA	$0 \leq V_{IN} \leq 5.5V$			
$I_{OFF}$	OFF State Leakage Current	1.65 – 5.5	±0.1			±1.0		µA	$0 \leq A, B_n \leq V_{CC}$			
$R_{ON}$	Switch On Resistance (Note 4)	4.5	5.0		7.0	7.0		Ω	$V_{IN} = 0V, I_O = 30\text{ mA}$			
			6.0		12.0	12.0			$V_{IN} = 2.4V, I_O = -30\text{ mA}$			
			7.0		15.0	15.0			$V_{IN} = 4.5V, I_O = -30\text{ mA}$			
		3.0	6.5		9.0	9.0			$V_{IN} = 0V, I_O = 24\text{ mA}$			
			9.0		20.0	20.0			$V_{IN} = 3V, I_O = -24\text{ mA}$			
			8.0		12.0	12.0			$V_{IN} = 0V, I_O = 8\text{ mA}$			
		2.3	11.0		30.0	30.0			$V_{IN} = 2.3V, I_O = -8\text{ mA}$			
			10.0		20.0	20.0			$V_{IN} = 0V, I_O = 4\text{ mA}$			
			17.0		50.0	50.0			$V_{IN} = 1.65V, I_O = -4\text{ mA}$			
		$I_{CC}$	Quiescent Supply Current All Channels ON or OFF	5.5	1.0				10.0		µA	$V_{IN} = V_{CC}$ or GND $I_{OUT} = 0$
					0.0				$V_{CC}$		V	
		ASR	Analog Signal Range	$V_{CC}$	0.0				$V_{CC}$		V	
$\Delta R_{ON}$	On Resistance Match Between Channels (Note 4)(Note 5)(Note 6)	4.5	0.15					Ω	$I_A = -30\text{ mA}, V_{Bn} = 3.15$			
		3.0	0.22						$I_A = -24\text{ mA}, V_{Bn} = 2.1$			
		2.3	0.31						$I_A = -8\text{ mA}, V_{Bn} = 1.6$			
		1.65	0.62						$I_A = -4\text{ mA}, V_{Bn} = 1.15$			
$R_{flat}$	On Resistance Flatness (Note 4)(Note 5)(Note 7)	5.0	6.0					Ω	$I_A = -30\text{ mA}, 0 \leq V_{Bn} \leq V_{CC}$			
		3.3	12.0						$I_A = -24\text{ mA}, 0 \leq V_{Bn} \leq V_{CC}$			
		2.5	40.0						$I_A = -8\text{ mA}, 0 \leq V_{Bn} \leq V_{CC}$			
		1.8	140.0						$I_A = -4\text{ mA}, 0 \leq V_{Bn} \leq V_{CC}$			

## DC Electrical Characteristics (Continued)

**Note 4:** Measured by the voltage drop between A and B<sub>n</sub> pins at the indicated current through the switch. On Resistance is determined by the lower of the voltages on the two (A or B<sub>n</sub> Ports).

**Note 5:** Parameter is characterized but not tested in production.

**Note 6:**  $\Delta R_{ON} = R_{ON\ max} - R_{ON\ min}$  measured at identical V<sub>CC</sub>, temperature and voltage levels.

**Note 7:** Flatness is defined as the difference between the maximum and minimum value of On Resistance over the specified range of conditions.

## AC Electrical Characteristics

Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = +25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions	Figure Number
			Min	Typ	Max	Min	Max			
t <sub>PHL</sub>	Propagation Delay Bus to Bus (Note 8)	1.65 – 1.95	2.0					ns	V <sub>I</sub> = OPEN	Figures 1, 2
t <sub>PLH</sub>		2.3 – 2.7	1.1							
		3.0 – 3.6	0.7							
		4.5 – 5.5	0.4							
t <sub>PZL</sub>	Output Enable Time Turn on Time (A to B <sub>n</sub> )	1.65 – 1.95	5.0	32.0		5.0	34.0	ns	V <sub>I</sub> = 2 x V <sub>CC</sub> for t <sub>PZL</sub> V <sub>I</sub> = 0V for t <sub>PZH</sub>	Figures 1, 2
t <sub>PZH</sub>		2.3 – 2.7	3.0	15.0		3.0	16.5			
		3.0 – 3.6	2.0	9.5		2.0	11.0			
		4.5 – 5.5	1.5	6.5		1.5	7.0			
t <sub>PLZ</sub>	Output Disable Time Turn Off Time (A Port to B <sub>n</sub> Port)	1.65 – 1.95	3.0	14.0		3.0	14.5	ns	V <sub>I</sub> = 2 x V <sub>CC</sub> for t <sub>PLZ</sub> V <sub>I</sub> = 0V for t <sub>PHZ</sub>	Figures 1, 2
t <sub>PHZ</sub>		2.3 – 2.7	2.0	7.2		2.0	7.8			
		3.0 – 3.6	1.5	5.1		1.5	5.5			
		4.5 – 5.5	0.8	3.7		0.8	4.0			
t <sub>B-M</sub>	Break Before Make Time (Note 9)	1.65 – 1.95	0.5			0.5		ns		Figure 3
		2.3 – 2.7	0.5			0.5				
		3.0 – 3.6	0.5			0.5				
		4.5 – 5.5	0.5			0.5				
Q	Charge Injection (Note 9)	5.0	3.0					pC	C <sub>L</sub> = 0.1 nF, V <sub>GEN</sub> = 0V R <sub>GEN</sub> = 0Ω	Figure 4
		3.3	2.0							
OIRR	Off Isolation (Note 10)	1.65 – 5.5	-58.0					dB	R <sub>L</sub> = 50Ω f = 10MHz	Figure 5
Xtalk	Crosstalk	1.65 – 5.5	-60.0					dB	R <sub>L</sub> = 50Ω f = 10MHz	Figure 6
BW	-3dB Bandwidth	1.65 – 5.5	250.0					MHz	R <sub>L</sub> = 50Ω	Figure 9
THD	Total Harmonic Distortion (Note 9)	5.0	.01					%	R <sub>L</sub> = 600Ω 0.5 V <sub>P-P</sub> f = 600 Hz to 20 KHz	

**Note 8:** This parameter is guaranteed by design but not tested. The bus switch contributes no propagation delay other than the RC delay of the On Resistance of the switch and the 50 pF load capacitance, when driven by an ideal voltage source (zero output impedance).

**Note 9:** Guaranteed by Design.

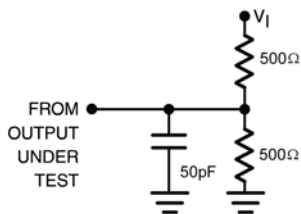
**Note 10:** Off Isolation = 20 log<sub>10</sub> [V<sub>A</sub> / V<sub>Bn</sub>]

## Capacitance (Note 11)

Symbol	Parameter	Typ	Max	Units	Conditions	Figure Number
C <sub>IN</sub>	Control Pin Input Capacitance	2.0		pF	V <sub>CC</sub> = 0V	
C <sub>IO-B</sub>	B Port Off Capacitance	3.6		pF	V <sub>CC</sub> = 5.0V	Figure 7
C <sub>IOA-ON</sub>	A Port Capacitance When Switch Is Enabled	14.5		pF	V <sub>CC</sub> = 5.0V	Figure 8

**Note 11:** T<sub>A</sub> = +25°C, f = 1 MHz, Capacitance is characterized but not tested in production.

## AC Loading and Waveforms

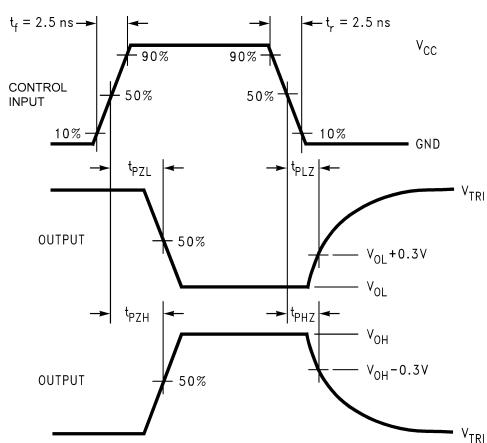
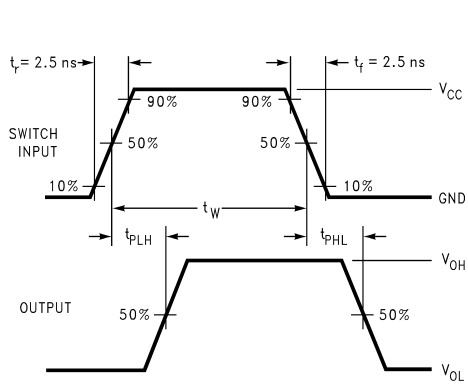


**Note:** Input driven by 50Ω source terminated in 50Ω

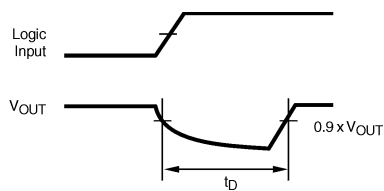
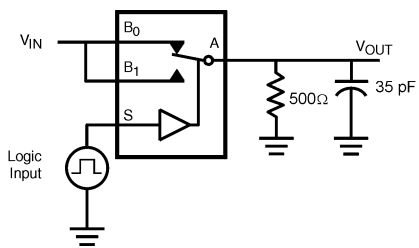
**Note:**  $C_L$  includes load and stray capacitance

**Note:** Input PRR = 1.0 MHz;  $t_W$  = 500 ns

**FIGURE 1. AC Test Circuit**



**FIGURE 2. AC Waveforms**



**FIGURE 3. Break Before Make Interval Timing**

AC Loading and Waveforms (Continued)

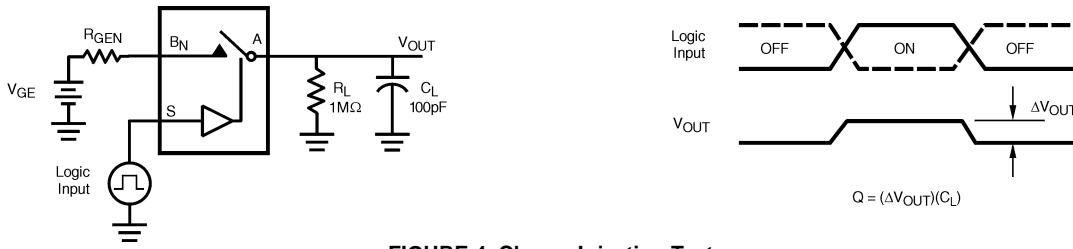


FIGURE 4. Charge Injection Test

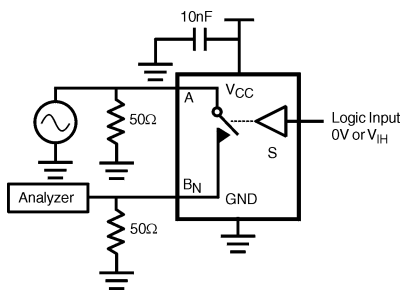


FIGURE 5. Off Isolation

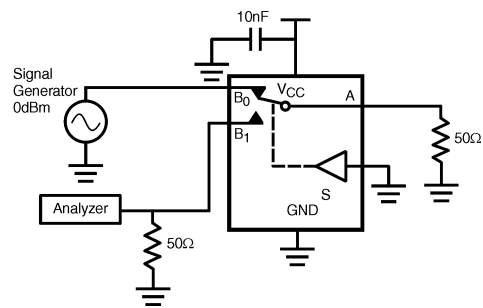


FIGURE 6. Crosstalk

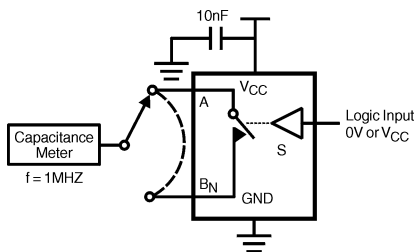


FIGURE 7. Channel Off Capacitance

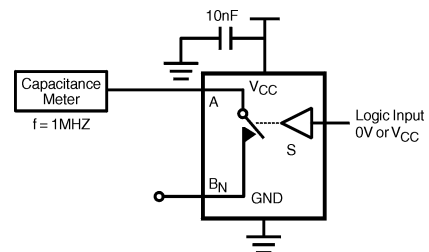


FIGURE 8. Channel On Capacitance

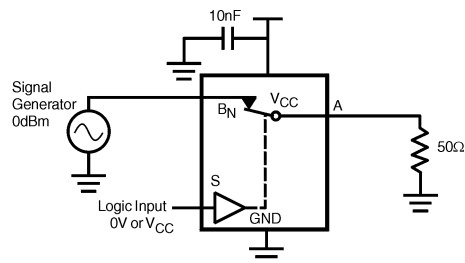


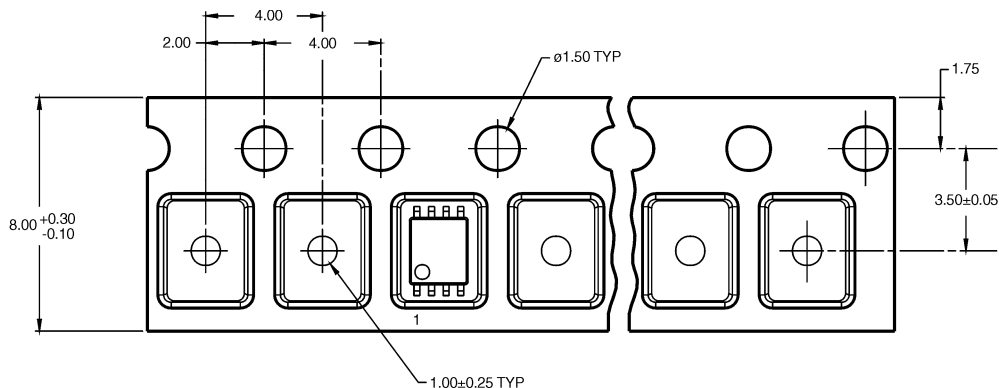
FIGURE 9. Bandwidth

# Tape and Reel Specification

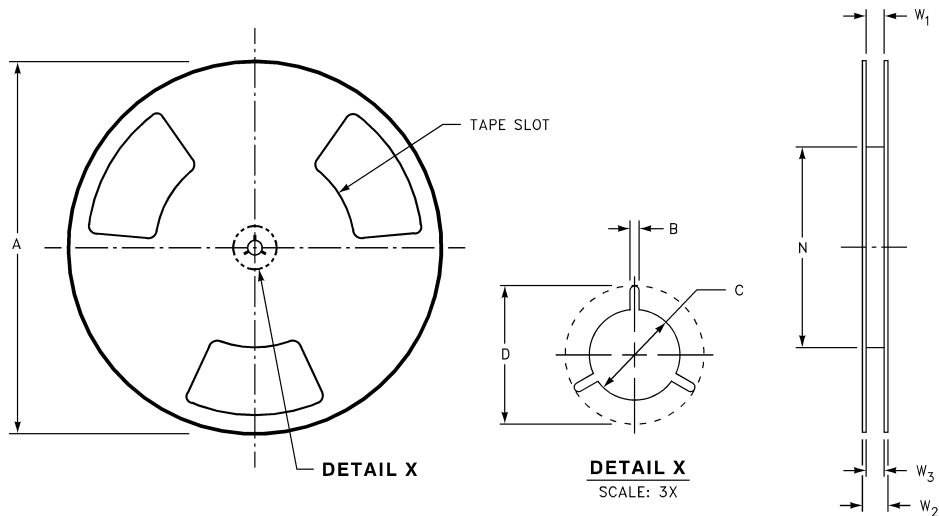
TAPE FORMAT for US8

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
K8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	250	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed

TAPE DIMENSIONS inches (millimeters)



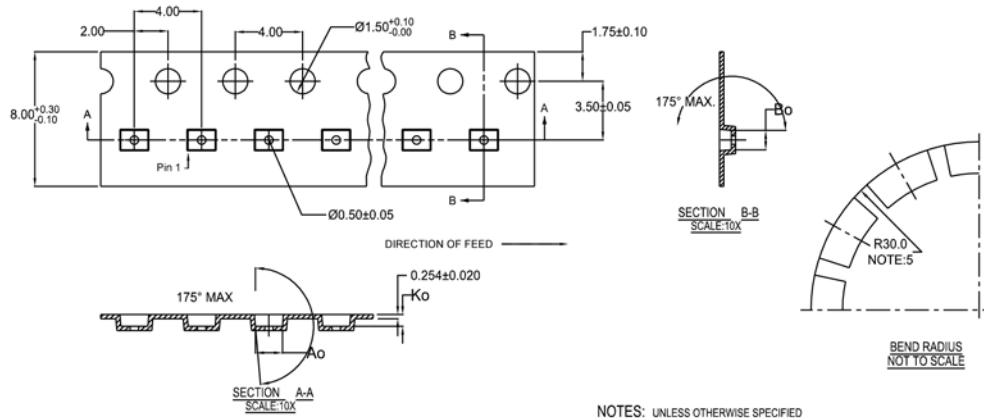
REEL DIMENSIONS inches (millimeters)



Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

TAPE FORMAT for MicroPak

Package Designator	Tape Section	Number Cavities	Cavity Status	Cover Tape Status
L8X	Leader (Start End)	125 (typ)	Empty	Sealed
	Carrier	5000	Filled	Sealed
	Trailer (Hub End)	75 (typ)	Empty	Sealed



10	300056	2.30 ± 0.05	1.78 ± 0.05	0.68 ± 0.05
8	300038	1.78 ± 0.05	1.78 ± 0.05	0.68 ± 0.05
6	300033	1.60 ± 0.05	1.15 ± 0.05	0.70 ± 0.05

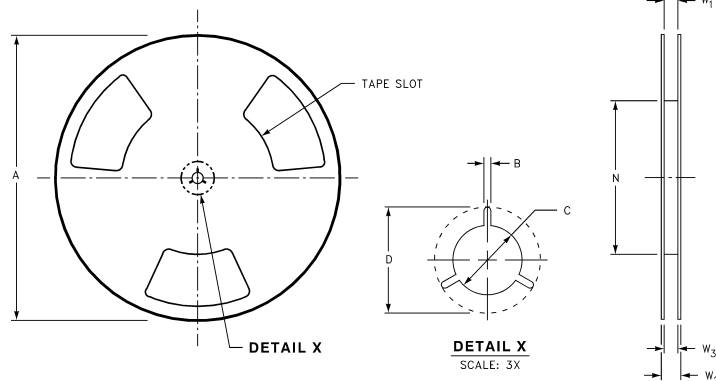
NOTES: UNLESS OTHERWISE SPECIFIED

1. ACCUMULATED 50 SPROCKETS, SPROCKET HOLE PITCH IS 200.00 ± 0.30MM
2. NO INDICATED CORNER RADIUS IS 0.127MM
3. CAMBER NOT TO EXCEED 1MM IN 100MM
4. SMALLEST ALLOWABLE BENDING RADIUS
5. POCKET POSITION RELATIVE TO SPROCKET HOLE MEASURED AS TRUE POSITION OF POCKET, NOT POCKET HOLE



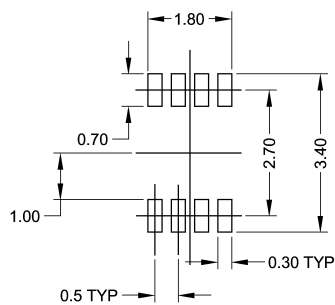
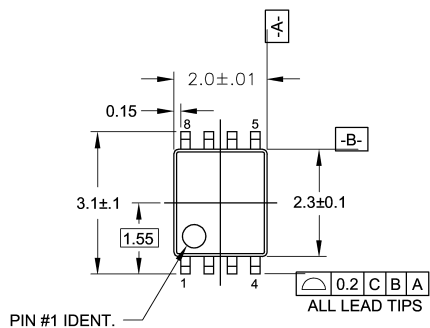
SCALE: 6X

REEL DIMENSIONS inches (millimeters)

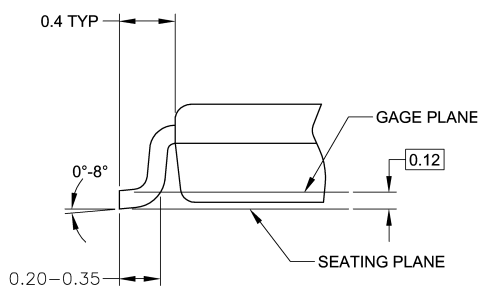
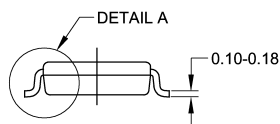
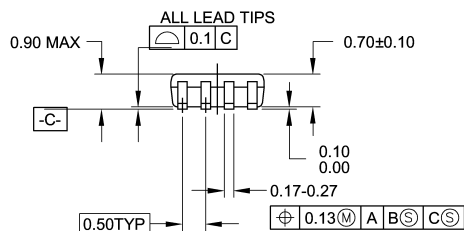


Tape Size	A	B	C	D	N	W1	W2	W3
8 mm	7.0 (177.8)	0.059 (1.50)	0.512 (13.00)	0.795 (20.20)	2.165 (55.00)	0.331 + 0.059/-0.000 (8.40 + 1.50/-0.00)	0.567 (14.40)	W1 + 0.078/-0.039 (W1 + 2.00/-1.00)

**Physical Dimensions** inches (millimeters) unless otherwise noted



**LAND PATTERN RECOMMENDATION**



**DETAIL A**

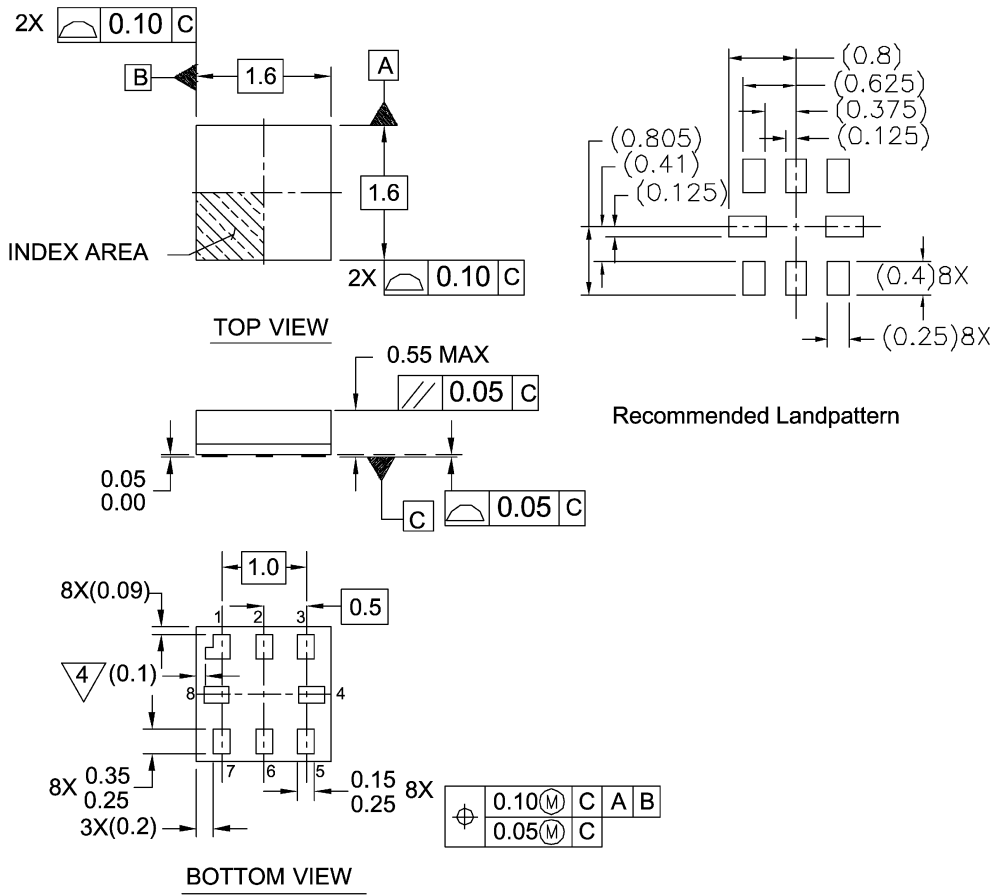
**NOTES:**

- A. CONFORMS TO JEDEC REGISTRATION MO-187
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MAB08AREVC

**8-Lead US8, JEDEC MO-187, Variation CA 3.1mm Wide  
Package Number MAB08A**

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



Notes:

1. PACKAGE CONFORMS TO JEDEC MO-255 VARIATION UAAD
2. DIMENSIONS ARE IN MILLIMETERS
3. DRAWING CONFORMS TO ASME Y.14M-1994

4 PIN 1 FLAG, END OF PACKAGE OFFSET.

MAC08AREVC

**Pb-Free 8-Lead MicroPak, 1.6 mm Wide  
Package Number MAC08A**

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Definition of terms

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