



THE DATASHEET OF NVTFS4C13NTAG



NVTFS4C13N

MOSFET – Power, Single N-Channel, μ 8FL 30 V, 9.4 m Ω , 40 A

Features

- Low $R_{DS(on)}$ to Minimize Conduction Losses
- Low Capacitance to Minimize Driver Losses
- Optimized Gate Charge to Minimize Switching Losses
- NVTFS4C13NWF – Wettable Flanks Product
- NVT Prefix for Automotive and Other Applications Requiring Unique Site and Control Change Requirements; AEC-Q101 Qualified and PPAP Capable
- These Devices are Pb-Free, Halogen Free/BFR Free and are RoHS Compliant

MAXIMUM RATINGS ($T_J = 25^\circ\text{C}$ unless otherwise stated)

Parameter	Symbol	Value	Unit
Drain-to-Source Voltage	V_{DS}	30	V
Gate-to-Source Voltage	V_{GS}	± 20	V
Continuous Drain Current $R_{\theta JA}$ (Notes 1, 2, 4)	I_D	$T_A = 25^\circ\text{C}$	14 A
		$T_A = 100^\circ\text{C}$	10
Power Dissipation $R_{\theta JA}$ (Note 1, 2, 4)	P_D	$T_A = 25^\circ\text{C}$	3.0 W
		$T_A = 100^\circ\text{C}$	1.5
Continuous Drain Current $R_{\theta JC}$ (Note 1, 3, 4)	I_D	$T_C = 25^\circ\text{C}$	40 A
		$T_C = 100^\circ\text{C}$	28 A
Power Dissipation $R_{\theta JC}$ (Note 1, 3, 4)	P_D	$T_C = 25^\circ\text{C}$	26 W
		$T_C = 100^\circ\text{C}$	13
Pulsed Drain Current	$T_A = 25^\circ\text{C}, t_p = 10 \mu\text{s}$	I_{DM}	152 A
Operating Junction and Storage Temperature	T_J, T_{stg}	-55 to +175	$^\circ\text{C}$
Source Current (Body Diode)	I_S	24	A
Single Pulse Drain-to-Source Avalanche Energy ($T_J = 25^\circ\text{C}, I_L = 14 \text{ A}_{pk}, L = 0.1 \text{ mH}$)	E_{AS}	10	mJ
Lead Temperature for Soldering Purposes (1/8" from case for 10 s)	T_L	260	$^\circ\text{C}$

Stresses exceeding those listed in the Maximum Ratings table may damage the device. If any of these limits are exceeded, device functionality should not be assumed, damage may occur and reliability may be affected.

THERMAL RESISTANCE MAXIMUM RATINGS

Parameter	Symbol	Value	Unit
Junction-to-Case – Steady State (Drain) (Notes 1 and 4)	$R_{\theta JC}$	5.8	$^\circ\text{C}/\text{W}$
Junction-to-Ambient – Steady State (Notes 1 and 2)	$R_{\theta JA}$	50	

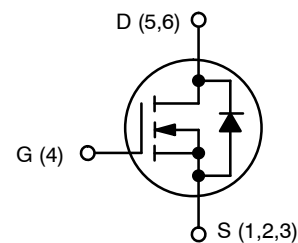
1. The entire application environment impacts the thermal resistance values shown, they are not constants and are only valid for the particular conditions noted.
2. Surface-mounted on FR4 board using a 650 mm² 2 oz. Cu pad.
3. Assumes heat-sink sufficiently large to maintain constant case temperature independent of device power.
4. Continuous DC current rating. Maximum current for pulses as long as 1 second is higher but is dependent on pulse duration and duty cycle.



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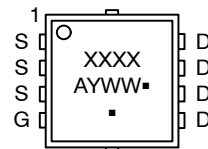
$V_{(BR)DSS}$	$R_{DS(ON)} \text{ MAX}$	$I_D \text{ MAX}$
30 V	9.4 m Ω @ 10 V	40 A
	14 m Ω @ 4.5 V	



N-CHANNEL MOSFET



MARKING DIAGRAM



4C13 = Specific Device Code for NVMTS4C13N

13WF = Specific Device Code of NVTFS4C13NWF

A = Assembly Location

Y = Year

WW = Work Week

▪ = Pb-Free Package

(Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information on page 5 of this data sheet.

NVTFS4C13N

ELECTRICAL CHARACTERISTICS ($T_J = 25^\circ\text{C}$ unless otherwise specified)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
OFF CHARACTERISTICS						
Drain-to-Source Breakdown Voltage	$V_{(BR)DSS}$	$V_{GS} = 0\text{ V}, I_D = 250\ \mu\text{A}$	30			V
Drain-to-Source Breakdown Voltage Temperature Coefficient	$V_{(BR)DSS}/T_J$			14.9		$\text{mV}/^\circ\text{C}$
Zero Gate Voltage Drain Current	I_{DSS}	$V_{GS} = 0\text{ V}, V_{DS} = 24\text{ V}$	$T_J = 25^\circ\text{C}$		1.0	μA
			$T_J = 125^\circ\text{C}$		10	
Gate-to-Source Leakage Current	I_{GSS}	$V_{DS} = 0\text{ V}, V_{GS} = \pm 20\text{ V}$			± 100	nA

ON CHARACTERISTICS (Note 5)

Gate Threshold Voltage	$V_{GS(TH)}$	$V_{GS} = V_{DS}, I_D = 250\ \mu\text{A}$	1.3		2.1	V
Negative Threshold Temperature Coefficient	$V_{GS(TH)}/T_J$			4.8		$\text{mV}/^\circ\text{C}$
Drain-to-Source On Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}, I_D = 30\text{ A}$		7.5	9.4	$\text{m}\Omega$
		$V_{GS} = 4.5\text{ V}, I_D = 12\text{ A}$		11.2	14	
Forward Transconductance	g_{FS}	$V_{DS} = 1.5\text{ V}, I_D = 15\text{ A}$		40		S
Gate Resistance	R_G	$T_A = 25^\circ\text{C}$		1.0		Ω

CHARGES AND CAPACITANCES

Input Capacitance	C_{ISS}	$V_{GS} = 0\text{ V}, f = 1\text{ MHz}, V_{DS} = 15\text{ V}$		770		pF
Output Capacitance	C_{OSS}			443		
Reverse Transfer Capacitance	C_{RSS}			127		
Capacitance Ratio	C_{RSS}/C_{ISS}	$V_{GS} = 0\text{ V}, V_{DS} = 15\text{ V}, f = 1\text{ MHz}$		0.165		
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		7.8		nC
Threshold Gate Charge	$Q_{G(TH)}$			1.4		
Gate-to-Source Charge	Q_{GS}			2.9		
Gate-to-Drain Charge	Q_{GD}			3.7		
Gate Plateau Voltage	V_{GP}			3.6		V
Total Gate Charge	$Q_{G(TOT)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}; I_D = 30\text{ A}$		15.2		nC

SWITCHING CHARACTERISTICS (Note 6)

Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 4.5\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		9		ns
Rise Time	t_r			35		
Turn-Off Delay Time	$t_{d(OFF)}$			13		
Fall Time	t_f			5		
Turn-On Delay Time	$t_{d(ON)}$	$V_{GS} = 10\text{ V}, V_{DS} = 15\text{ V}, I_D = 15\text{ A}, R_G = 3.0\ \Omega$		6.0		ns
Rise Time	t_r			26		
Turn-Off Delay Time	$t_{d(OFF)}$			16		
Fall Time	t_f			3.0		

DRAIN-SOURCE DIODE CHARACTERISTICS

Forward Diode Voltage	V_{SD}	$V_{GS} = 0\text{ V}, I_S = 30\text{ A}$	$T_J = 25^\circ\text{C}$	0.82	1.1	V
			$T_J = 125^\circ\text{C}$	0.69		
Reverse Recovery Time	t_{RR}	$V_{GS} = 0\text{ V}, dI_S/dt = 100\text{ A}/\mu\text{s}, I_S = 30\text{ A}$		23.4		ns
Charge Time	t_a			12.1		
Discharge Time	t_b			11.3		
Reverse Recovery Charge	Q_{RR}			9.7		nC

- Pulse Test: pulse width $\leq 300\ \mu\text{s}$, duty cycle $\leq 2\%$.
- Switching characteristics are independent of operating junction temperatures.

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TYPICAL CHARACTERISTICS

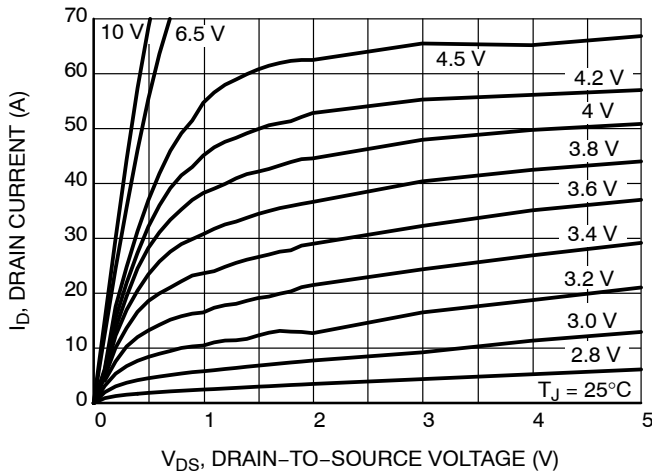


Figure 1. On-Region Characteristics

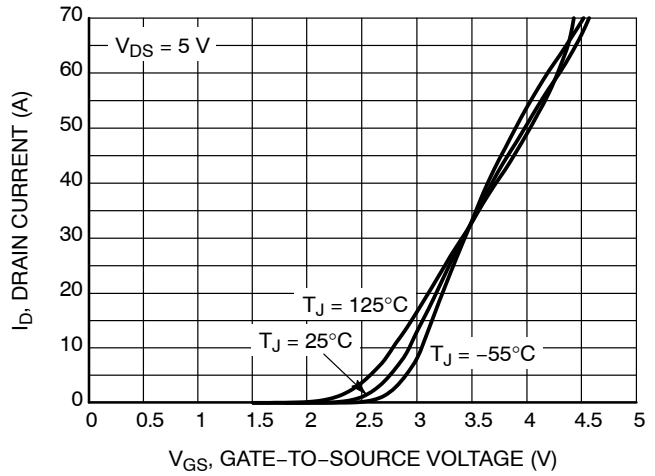


Figure 2. Transfer Characteristics

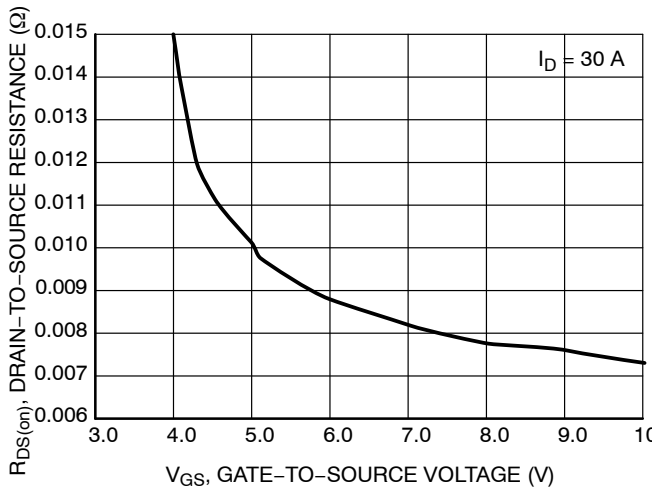


Figure 3. On-Resistance vs. V_{GS}

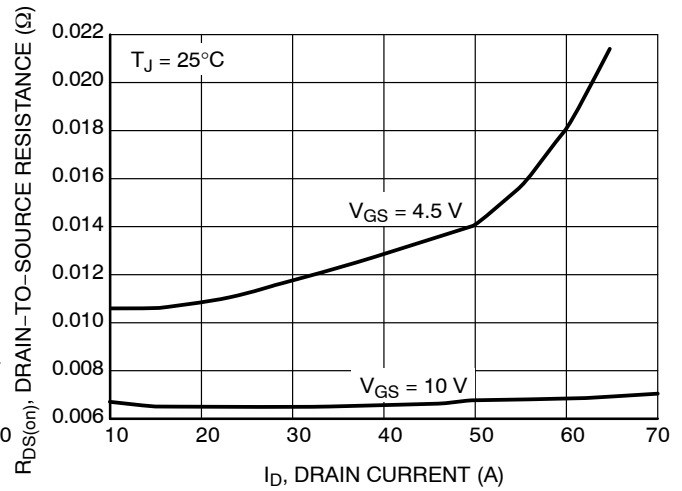


Figure 4. On-Resistance vs. Drain Current and Gate Voltage

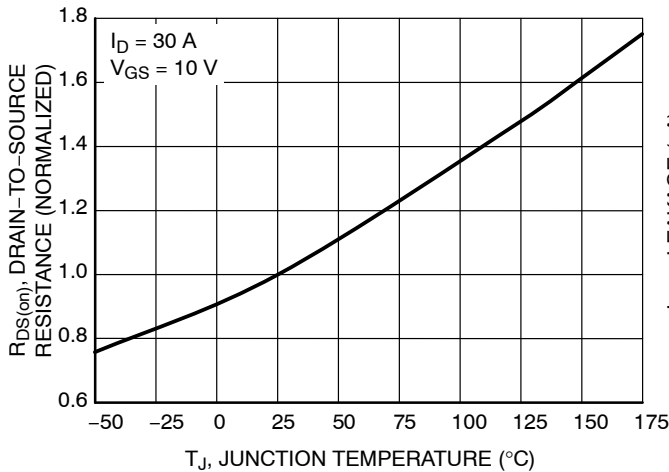


Figure 5. On-Resistance Variation with Temperature

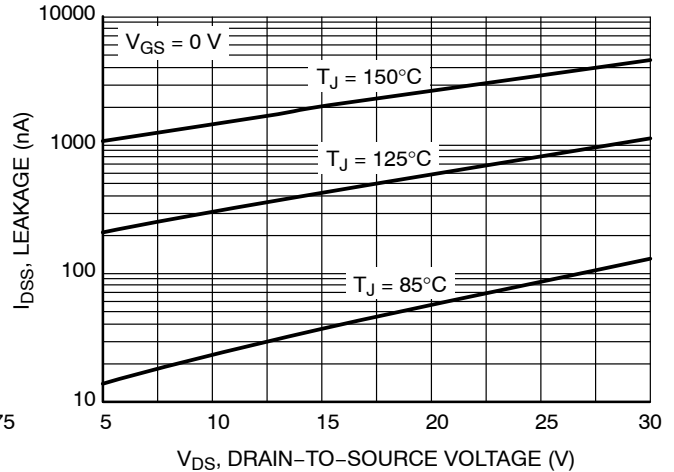


Figure 6. Drain-to-Source Leakage Current vs. Voltage

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TYPICAL CHARACTERISTICS

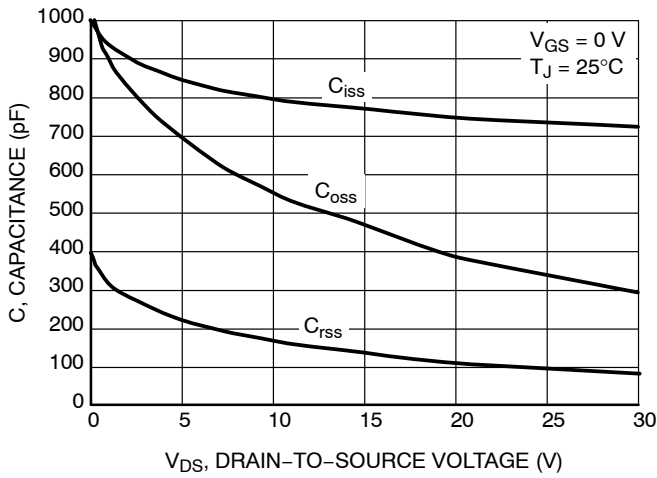


Figure 7. Capacitance Variation

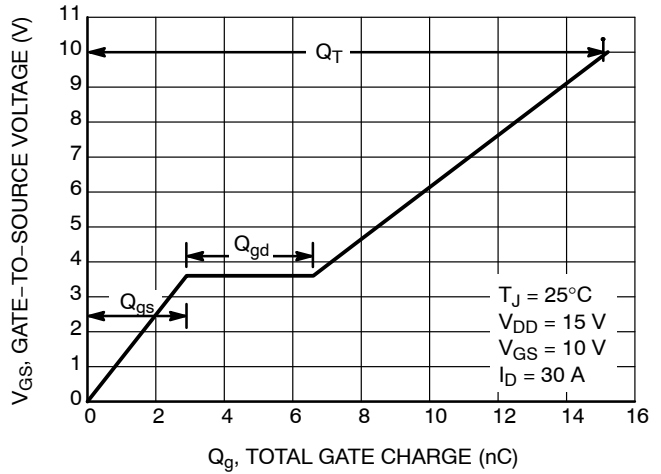


Figure 8. Gate-to-Source and Drain-to-Source Voltage vs. Total Charge

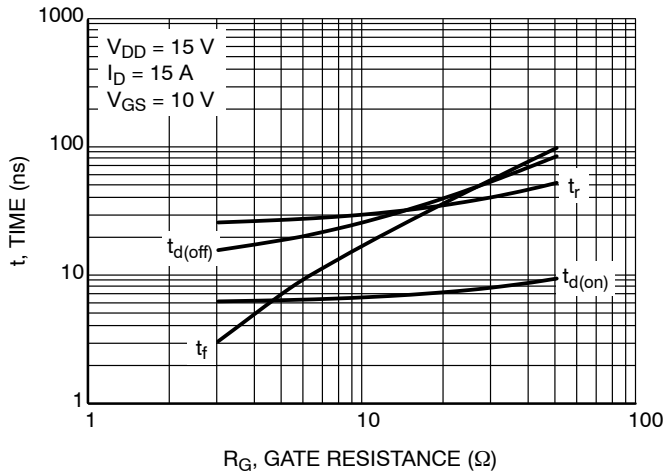


Figure 9. Resistive Switching Time Variation vs. Gate Resistance

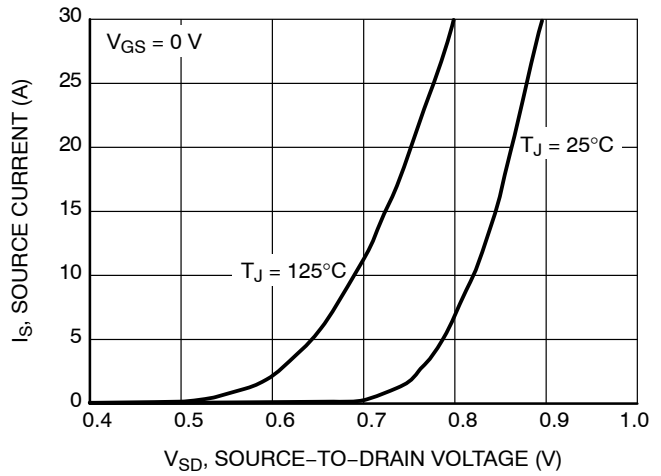


Figure 10. Diode Forward Voltage vs. Current

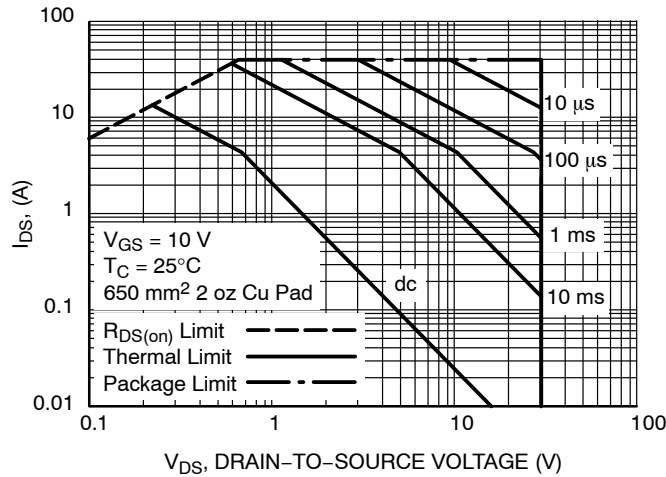


Figure 11. Maximum Rated Forward Biased Safe Operating Area

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TYPICAL CHARACTERISTICS

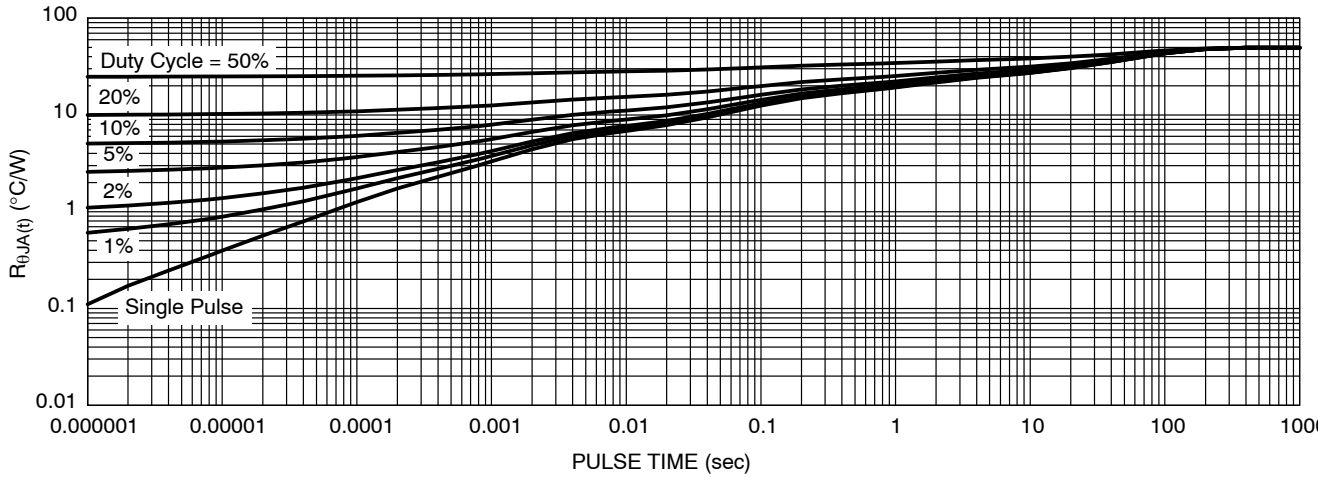


Figure 12. Thermal Response

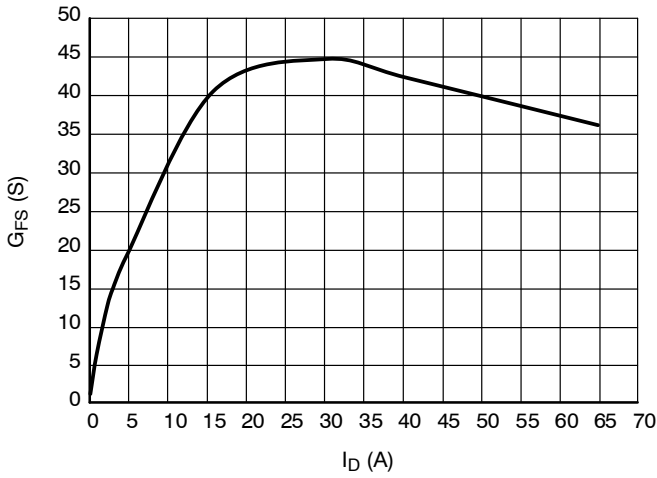


Figure 13. G_{FS} vs. I_D

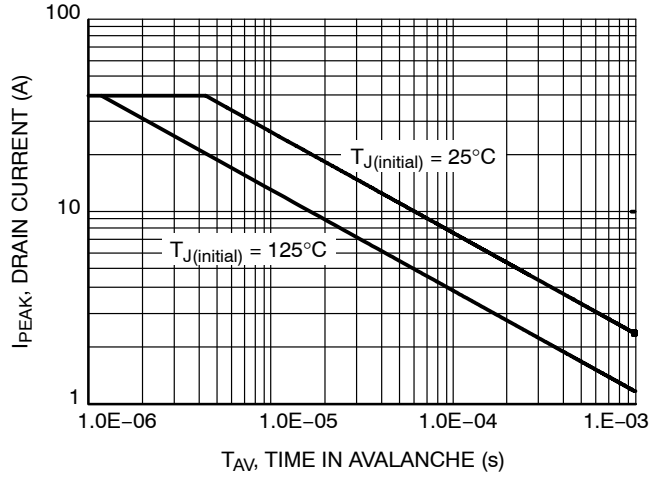


Figure 14. Avalanche Characteristics

ORDERING INFORMATION

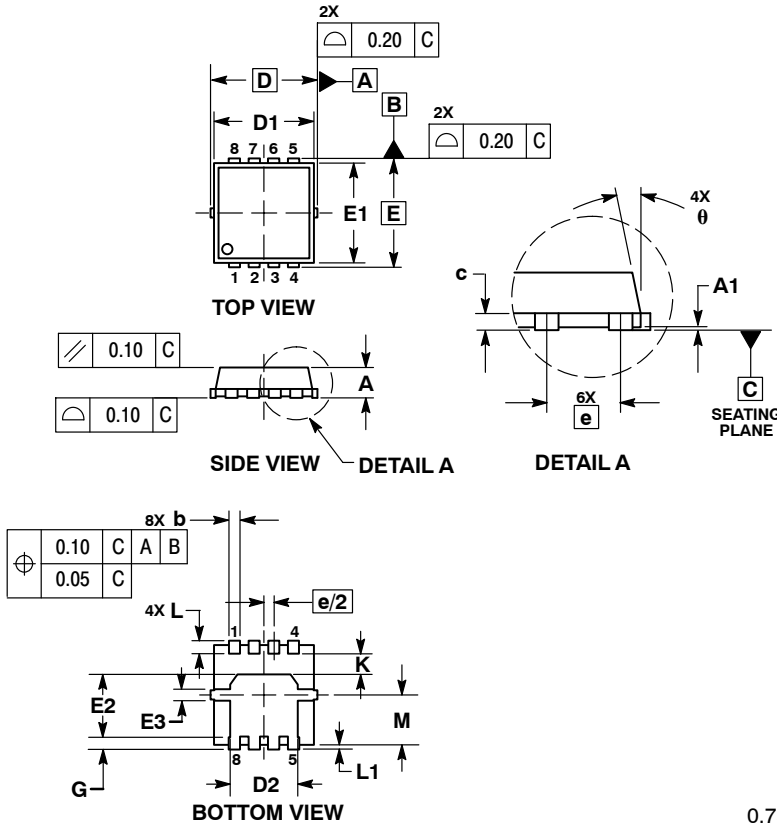
Device	Package	Shipping [†]
NVTFS4C13NTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFS4C13NWFTAG	WDFN8 (Pb-Free)	1500 / Tape & Reel
NVTFS4C13NTWG	WDFN8 (Pb-Free)	5000 / Tape & Reel
NVTFS4C13NWFTWG	WDFN8 (Pb-Free)	5000 / Tape & Reel

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NVTF54C13N

PACKAGE DIMENSIONS

WDFN8 3.3x3.3, 0.65P
CASE 511AB
ISSUE D

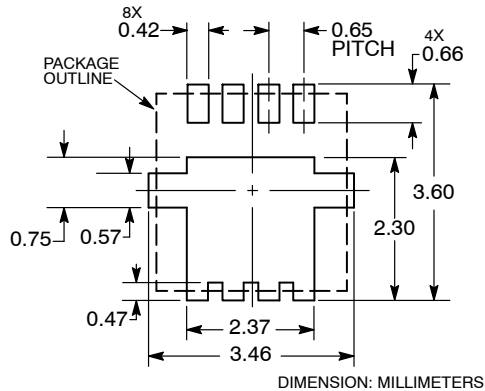


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION D1 AND E1 DO NOT INCLUDE MOLD FLASH PROTRUSIONS OR GATE BURRS.

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.70	0.75	0.80	0.028	0.030	0.031
A1	0.00	---	0.05	0.000	---	0.002
b	0.23	0.30	0.40	0.009	0.012	0.016
c	0.15	0.20	0.25	0.006	0.008	0.010
D	3.30 BSC			0.130 BSC		
D1	2.95	3.05	3.15	0.116	0.120	0.124
D2	1.98	2.11	2.24	0.078	0.083	0.088
E	3.30 BSC			0.130 BSC		
E1	2.95	3.05	3.15	0.116	0.120	0.124
E2	1.47	1.60	1.73	0.058	0.063	0.068
E3	0.23	0.30	0.40	0.009	0.012	0.016
e	0.65 BSC			0.026 BSC		
G	0.30	0.41	0.51	0.012	0.016	0.020
K	0.65	0.80	0.95	0.026	0.032	0.037
L	0.30	0.43	0.56	0.012	0.017	0.022
L1	0.06	0.13	0.20	0.002	0.005	0.008
M	1.40	1.50	1.60	0.055	0.059	0.063
θ	0°	---	12°	0°	---	12°

SOLDERING FOOTPRINT*



*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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