



**THE DATASHEET OF  
STD150NH02L-1**





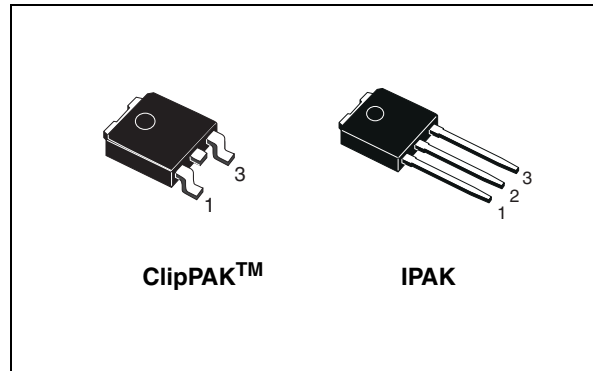
# STD150NH02L-1 STD150NH02L

N-channel 24V - 0.003Ω - 150A - ClipPAK™ - IPAK  
STripFET™ III Power MOSFET

## General features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub>	I <sub>D</sub>
STD150NH02L	24V	<0.0035Ω	150A
STD150NH02L-1	24V	<0.0035Ω	150A

- R<sub>DS(on)</sub> \* Qg industry's benchmark
- Conduction losses reduced
- Switching losses reduced
- Low threshold device



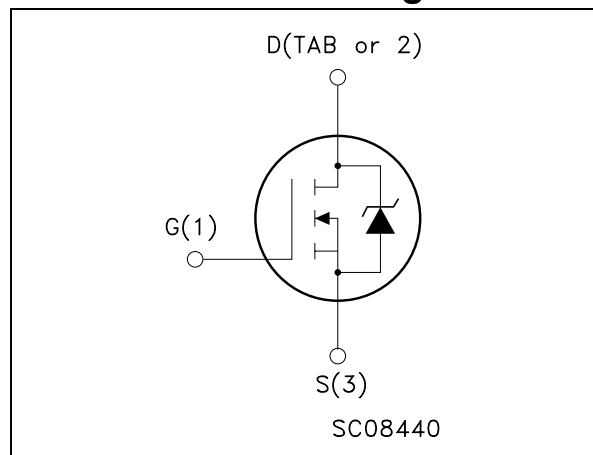
## Description

The STD150NH02L utilizes the latest advanced design rules of ST's proprietary STripFET™ technology. This novel 0.6μ process utilizes also unique metallization techniques that couple to a "bondless" assembly technique result in outstanding performance with standard DPAK outline. It is therefore ideal in high performance DC-DC converter applications where efficiency it to be achieved at very high out currents.

## Applications

- Switching application

## Internal schematic diagram



## Order codes

Part number	Marking	Package	Packaging
STD150NH02LT4	D150NH02L	ClipPAK™	Tape & reel
STD150NH02L-1	D150NH02L	IPAK	Tube

# Contents

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# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{\text{spike}}^{(1)}$	Drain-source voltage rating	30	V
$V_{\text{DS}}$	Drain-source voltage ( $V_{\text{GS}} = 0$ )	24	V
$V_{\text{DGR}}$	Drain-gate voltage ( $R_{\text{GS}} = 20\text{K}\Omega$ )	24	V
$V_{\text{GS}}$	Drain-source voltage	$\pm 20$	V
$I_{\text{D}}$	Drain current (continuous) at $T_{\text{C}} = 25^{\circ}\text{C}$	150	A
$I_{\text{D}}$	Drain current (continuous) at $T_{\text{C}}=100^{\circ}\text{C}$	107	A
$I_{\text{DM}}^{(2)}$	Drain current (pulsed)	600	A
$P_{\text{TOT}}$	Total dissipation at $T_{\text{C}} = 25^{\circ}\text{C}$	125	W
	Derating factor	0.83	W/ $^{\circ}\text{C}$
$E_{\text{AS}}^{(3)}$	Single pulse avalanche energy	500	mJ
$T_{\text{stg}}$	Storage temperature	-55 to 175	$^{\circ}\text{C}$
$T_{\text{J}}$	Max. operating junction temperature		

1. Garanted when external  $R_{\text{g}} = 4.7 \Omega$  and  $t_{\text{f}} < t_{\text{fmax}}$ .

2. Pulse width limited by safe operating area

3. Starting  $T_{\text{J}} = 25^{\circ}\text{C}$ ,  $I_{\text{D}} = 75\text{A}$ ,  $V_{\text{DD}} = 10\text{V}$

**Table 2. Thermal data**

Symbol	Parameter	Value	Unit
$R_{\text{thJC}}$	Thermal resistance junction-case Max	1.2	$^{\circ}\text{C}/\text{W}$
$R_{\text{thJA}}$	Thermal resistance junction-ambient Max	100	$^{\circ}\text{C}/\text{W}$
$T_{\text{I}}$	Maximum lead temperature for soldering purpose	275	$^{\circ}\text{C}$

## 2 Electrical characteristics

(T<sub>CASE</sub>=25°C unless otherwise specified)

**Table 3. On<sup>(1)</sup> /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
V <sub>(BR)DSS</sub>	Drain-source breakdown voltage	I <sub>D</sub> = 25mA, V <sub>GS</sub> = 0	24			V
I <sub>DSS</sub>	Zero gate voltage drain current (V <sub>GS</sub> = 0)	V <sub>DS</sub> = 20V V <sub>DS</sub> = 20V, T <sub>C</sub> = 125°C			1 10	μA μA
I <sub>GSS</sub>	Gate body leakage current (V <sub>DS</sub> = 0)	V <sub>GS</sub> = ±20V			±100	nA
V <sub>GS(th)</sub>	Gate threshold voltage	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA	1	1.8		V
R <sub>DS(on)</sub>	Static drain-source on resistance	V <sub>GS</sub> = 10V, I <sub>D</sub> = 75A V <sub>GS</sub> = 5V, I <sub>D</sub> = 37.5A		0.003 0.004	0.0035 0.0065	Ω Ω

1. Pulsed: Pulse duration = 300 μs, duty cycle 1.5%

**Table 4. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
g <sub>fs</sub> <sup>(1)</sup>	Forward transconductance	V <sub>DS</sub> = 10 V, I <sub>D</sub> = 75A		60		S
C <sub>iss</sub> C <sub>oss</sub> C <sub>rss</sub>	Input capacitance Output capacitance Reverse transfer capacitance	V <sub>DS</sub> = 15V, f = 1 MHz, V <sub>GS</sub> = 0		4450 1126 141		pF pF pF
Q <sub>g</sub> Q <sub>gs</sub> Q <sub>gd</sub>	Total gate charge Gate-source charge Gate-drain charge	V <sub>DD</sub> = 16V, I <sub>D</sub> = 150A V <sub>GS</sub> = 10V		69 13 9	93	nC nC nC
Q <sub>oss</sub> <sup>(2)</sup>	Output charge	V <sub>DS</sub> = 16V, V <sub>GS</sub> = 0V		27		nC
Q <sub>gls</sub> <sup>(3)</sup>	Third-quadrant gate charge	V <sub>DS</sub> < 0V, V <sub>GS</sub> = 10V		64		nC
R <sub>G</sub>	Gate input resistance	f = 1MHz gate DC Bias = 0 Test signal level = 20mV Open drain		1.6		Ω

1. Pulsed: pulse duration=300μs, duty cycle 1.5%

2. Q<sub>oss</sub> = C<sub>oss</sub> \* Δ V<sub>in</sub>, C<sub>oss</sub> = C<sub>gd</sub> + C<sub>ds</sub>. See Appendix A

3. Gate charge for synchronous operation

**Table 5. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 10V, I_D = 75A,$ $R_G = 4.7\Omega, V_{GS} = 10V$ <i>Figure 13 on page 8</i>		14		ns
$t_r$	Rise time			224		ns
$t_{d(off)}$	Turn-off delay time			69		ns
$t_f$	Fall time			40	54	ns

**Table 6. Source drain diode**

Symbol	Parameter	Test conditions	Min	Typ.	Max	Unit
$I_{SD}$	Source-drain current				150	A
$I_{SDM}$	Source-drain current (pulsed)				600	A
$V_{SD}^{(1)}$	Forward on voltage	$I_{SD} = 75A, V_{GS} = 0$			1.15	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 150A,$ $di/dt = 100A/\mu s,$ $V_{DD} = 15V, T_J = 150^\circ C$ <i>Figure 15 on page 8</i>		47		ns
$Q_{rr}$	Reverse recovery charge			58		$\mu C$
$I_{RRM}$	Reverse recovery current			2.5		A

1. Pulsed: pulse duration=300 $\mu s$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 1. Safe operating area

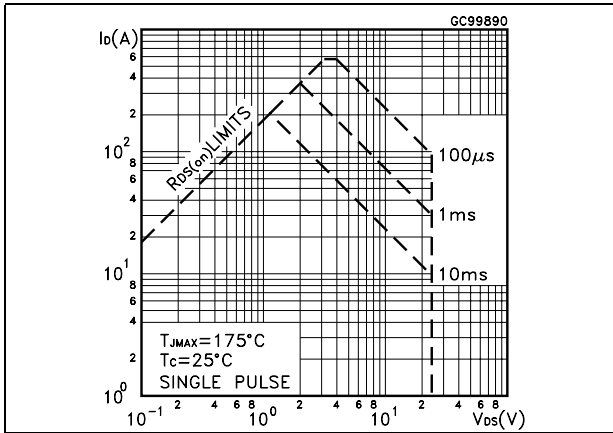


Figure 2. Thermal impedance

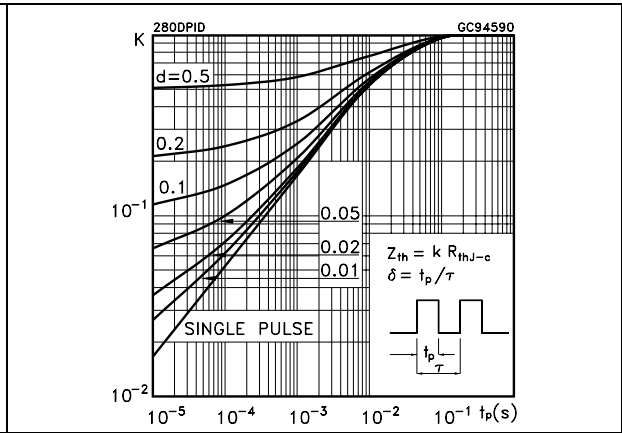


Figure 3. Output characteristics

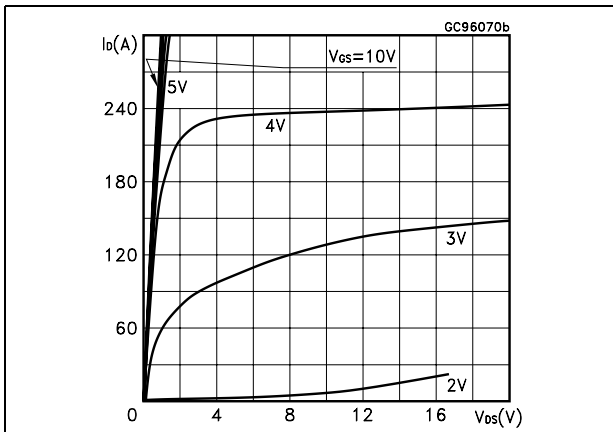


Figure 4. Transfer characteristics

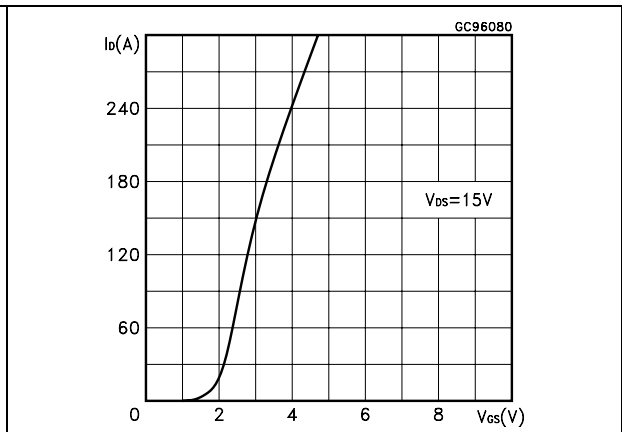


Figure 5. Transconductance

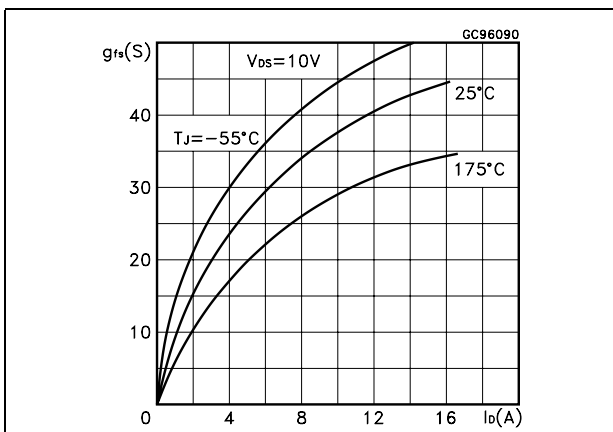


Figure 6. Static drain-source on resistance

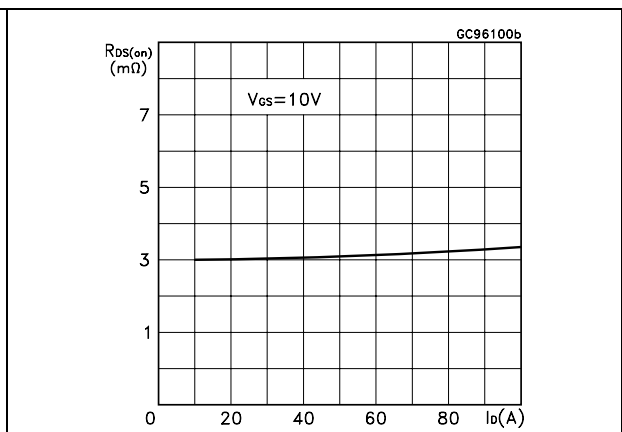


Figure 7. Gate charge vs gate-source voltage Figure 8. Capacitance variations

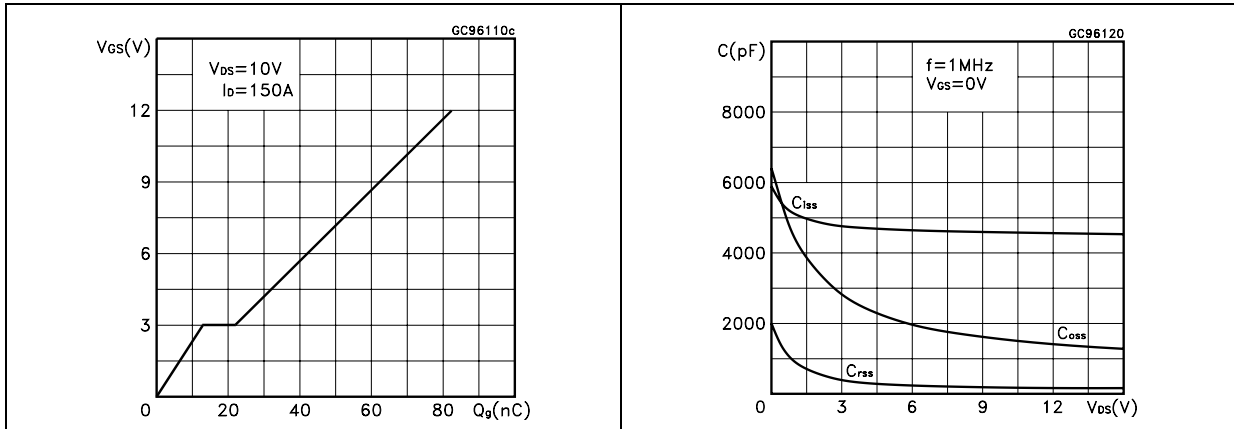


Figure 9. Normalized gate threshold voltage vs temperature Figure 10. Normalized on resistance vs temperature

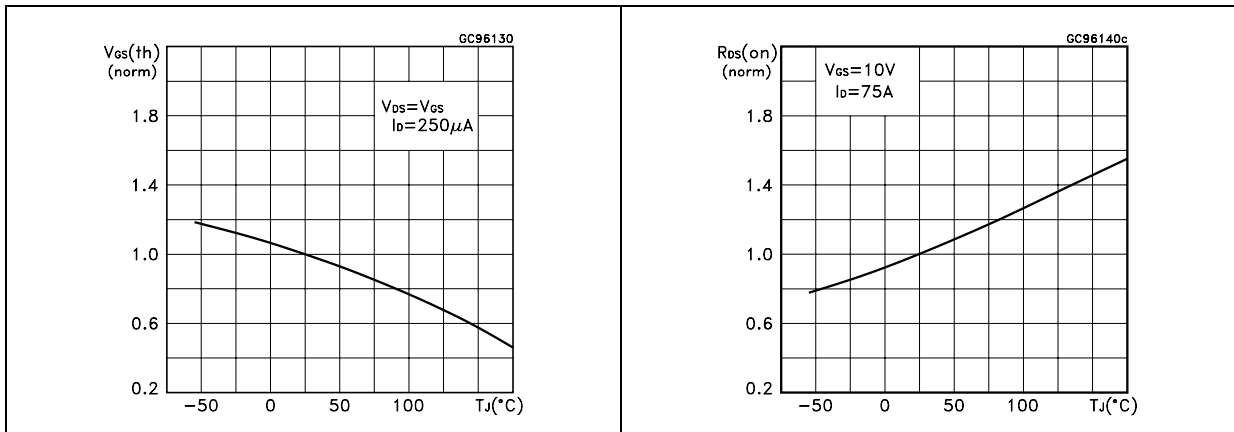
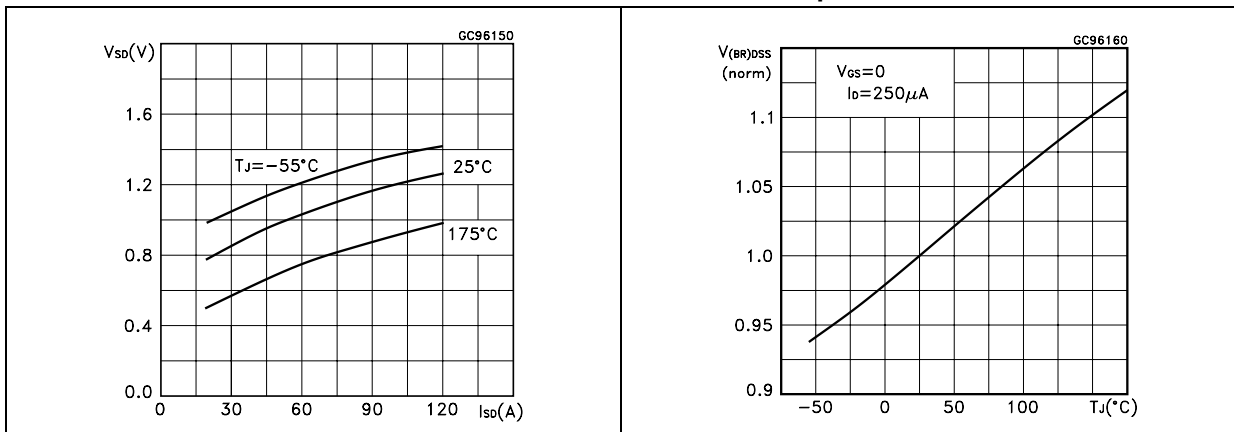


Figure 11. Source-drain diode forward characteristics Figure 12. Normalized breakdown voltage vs temperature



### 3 Test circuit

Figure 13. Switching times test circuit for resistive load

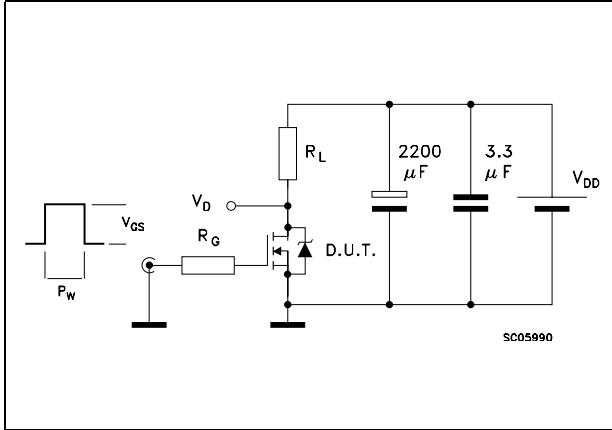


Figure 14. Gate charge test circuit

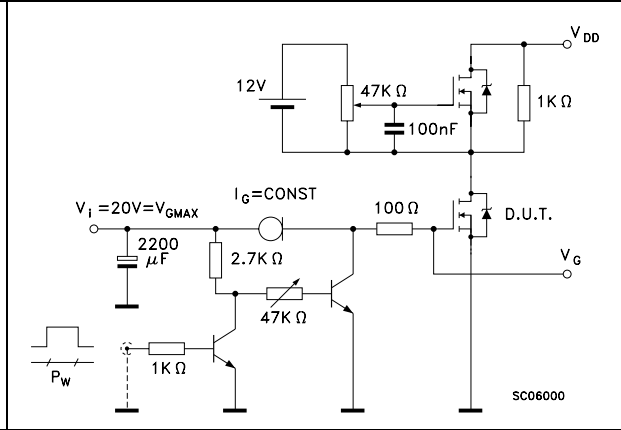


Figure 15. Test circuit for inductive load switching and diode recovery times

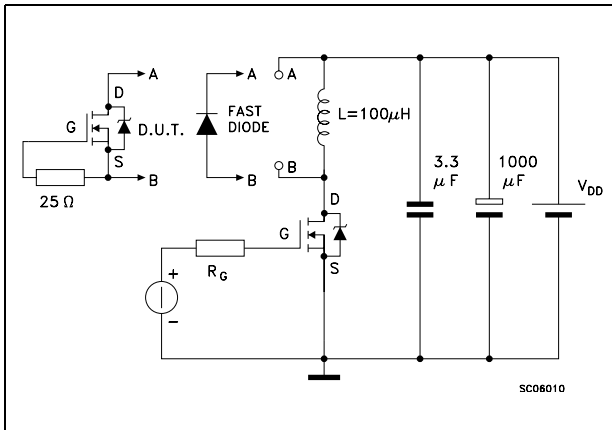


Figure 16. Unclamped Inductive load test circuit

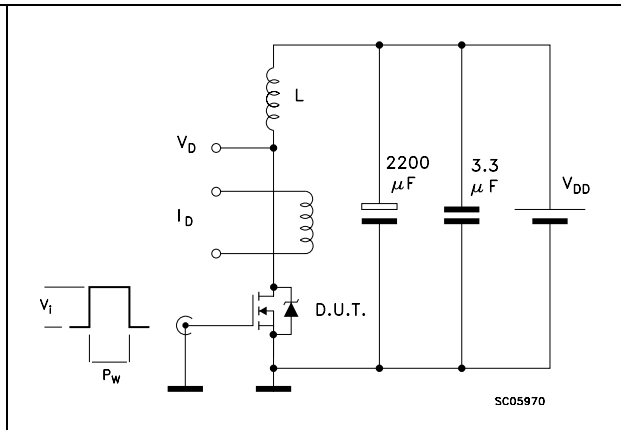
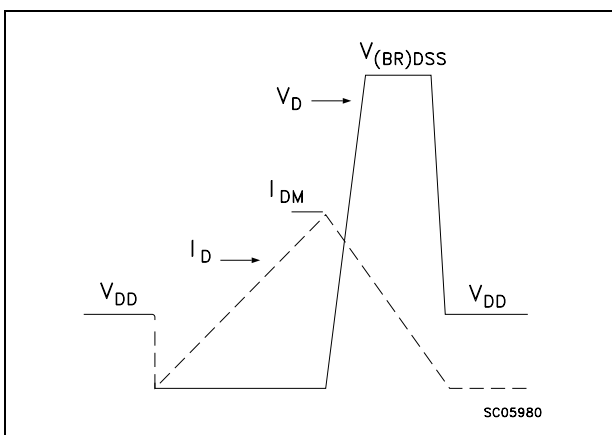


Figure 17. Unclamped inductive waveform

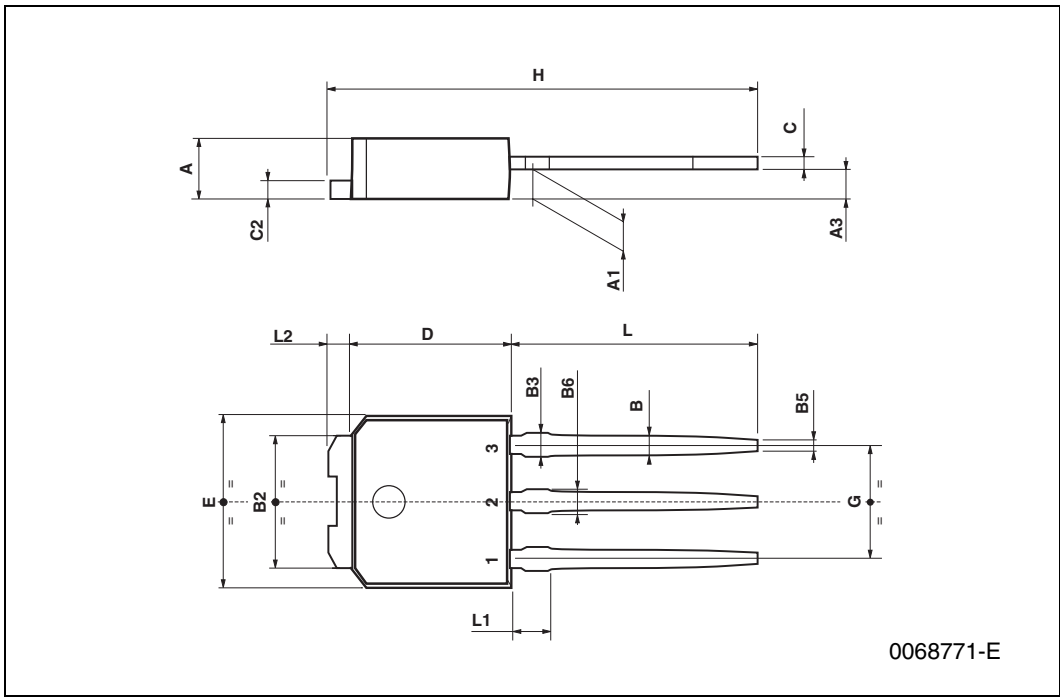


## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in ECOPACK® packages. These packages have a Lead-free second level interconnect . The category of second level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label. ECOPACK is an ST trademark. ECOPACK specifications are available at: [www.st.com](http://www.st.com)

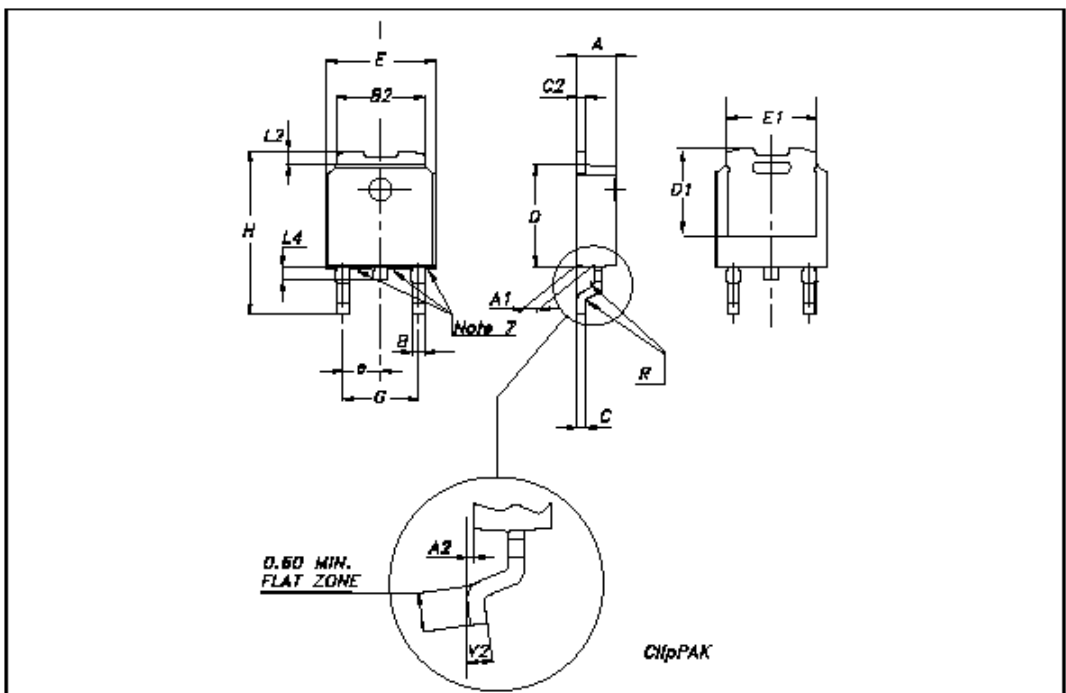
**TO-251 (IPAK) MECHANICAL DATA**

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.2		2.4	0.086		0.094
A1	0.9		1.1	0.035		0.043
A3	0.7		1.3	0.027		0.051
B	0.64		0.9	0.025		0.031
B2	5.2		5.4	0.204		0.212
B3			0.85			0.033
B5		0.3			0.012	
B6			0.95			0.037
C	0.45		0.6	0.017		0.023
C2	0.48		0.6	0.019		0.023
D	6		6.2	0.236		0.244
E	6.4		6.6	0.252		0.260
G	4.4		4.6	0.173		0.181
H	15.9		16.3	0.626		0.641
L	9		9.4	0.354		0.370
L1	0.8		1.2	0.031		0.047
L2		0.8	1		0.031	0.039



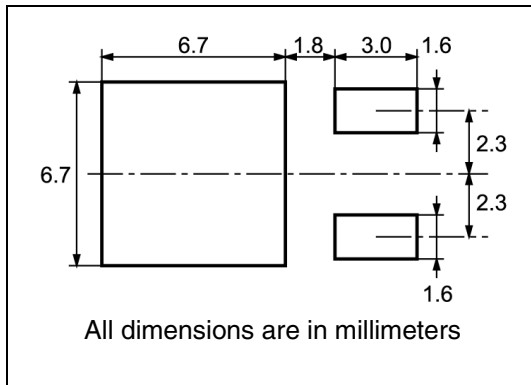
**ClipPAK™**

DIM.	mm.			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A	2.20		2.40	0.087		0.094
A1	0.90		1.10	0.035		0.043
A2	0.03		0.23	0.001		0.009
B	0.64		0.90	0.025		0.035
B2	5.20		5.40	0.204		0.213
C	0.45		0.60	0.018		0.024
C2	0.48		0.60	0.019		0.024
D	6.00		6.20	0.236		0.244
D1		5.10			0.200	
E	6.40		6.60	0.252		0.260
E1		5.20			0.204	
e		2.28			0.089	
G	4.40		4.60	0.173		0.181
H	9.35		10.10	0.368		0.398
L2		0.8			0.031	
L4	0.60		1.00	0.024		0.039
V2	0°		8°	0°		0°



# 5 Packaging mechanical data

## DPAK FOOTPRINT



## TAPE AND REEL SHIPMENT

40 mm min. Access hole at slot location

Full radius

Tape slot in core for tape start 2.5mm min. width

G measured at hub

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A		330		12.992
B	1.5		0.059	
C	12.8	13.2	0.504	0.520
D	20.2		0.795	
G	16.4	18.4	0.645	0.724
N	50		1.968	
T		22.4		0.881

BASE QTY	BULK QTY
2500	2500

DIM.	mm		inch	
	MIN.	MAX.	MIN.	MAX.
A0	6.8	7	0.267	0.275
B0	10.4	10.6	0.409	0.417
B1		12.1		0.476
D	1.5	1.6	0.059	0.063
D1	1.5		0.059	
E	1.65	1.85	0.065	0.073
F	7.4	7.6	0.291	0.299
K0	2.55	2.75	0.100	0.108
P0	3.9	4.1	0.153	0.161
P1	7.9	8.1	0.311	0.319
P2	1.9	2.1	0.075	0.082
R	40		1.574	
W	15.7	16.3	0.618	0.641

10 pitches cumulative tolerance on tape +/- 0.2 mm

User Direction of Feed

Center line of cavity

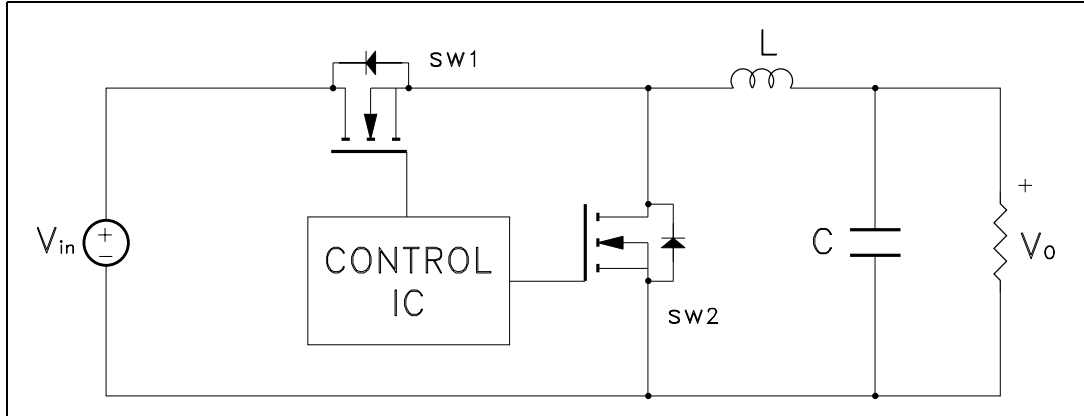
For machine ref. only including draft and radii concentric around B0

FEED DIRECTION

Bending radius R min.

## Appendix A Buck converter - power losses estimation

Figure 18. Buck converter: power losses estimation



The power losses associated with the FETs in a synchronous buck converter can be estimated using the equations shown in the table below. The formulas give a good approximation, for the sake of performance comparison, of how different pairs of devices affect the converter efficiency. However a very important parameter, the working temperature, is not considered. The real device behavior is really dependent on how the heat generated inside the devices is removed to allow for a safer working junction temperature.

- The low side (SW2) device requires:
  - Very low  $R_{DS(on)}$  to reduce conduction losses
  - Small  $Q_{gs}$  to reduce the gate charge losses
  - Small  $C_{oss}$  to reduce losses due to output capacitance
  - Small  $Q_{rr}$  to reduce losses on SW1 during its turn-on
  - The  $C_{gd}/C_{gs}$  ratio lower than  $V_{th}/V_{gg}$  ratio especially with low drain to source voltage to avoid the cross conduction phenomenon;
- The high side (SW1) device requires:
  - Small  $R_g$  and  $L_s$  to allow higher gate current peak and to limit the voltage feedback on the gate
  - Small  $Q_g$  to have a faster commutation and to reduce gate charge losses
  - Low  $R_{DS(on)}$  to reduce the conduction losses.

**Table 7. Power losses calculation**

		High side switching (SW1)	Low side switch (SW2)
Pconduction		$R_{DS(on)SW1} * I_L^2 * \delta$	$R_{DS(on)SW2} * I_L^2 * (1 - \delta)$
Pswitching		$V_{in} * (Q_{gsth(SW1)} + Q_{gd(SW1)}) * f * \frac{I_L}{I_g}$	Zero Voltage Switching
Pdiode	Recovery (1)	Not applicable	$V_{in} * Q_{rr(SW2)} * f$
	Conduction	Not applicable	$V_{f(SW2)} * I_L * t_{deadtime} * f$
Pgate(Q <sub>G</sub> )		$Q_{g(SW1)} * V_{gg} * f$	$Q_{gls(SW2)} * V_{gg} * f$
P <sub>Qoss</sub>		$\frac{V_{in} * Q_{oss(SW1)} * f}{2}$	$\frac{V_{in} * Q_{oss(SW2)} * f}{2}$

1. Dissipated by SW1 during turn-on

**Table 8. Paramiters meaning**

Parameter	Meaning
d	Duty-cycle
Q <sub>gsth</sub>	Post threshold gate charge
Q <sub>gls</sub>	Third quadrant gate charge
Pconduction	On state losses
Pswitching	On-off transition losses
Pdiode	Conduction and reverse recovery diode losses
Pgate	Gate drive losses
P <sub>Qoss</sub>	Output capacitance losses

## 6 Revision history

**Table 9. Revision history**

<b>Date</b>	<b>Revision</b>	<b>Changes</b>
09-Sep-2004	6	Preliminary data
21-Jun-2005	7	Complete version with curves
28-Jul-2006	8	The document has been reformatted
20-Dec-2006	9	Typo mistake on <a href="#">Table 3</a> .

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