



# THE DATASHEET OF STD65N3LLH5





# STD65N3LLH5 STU65N3LLH5

N-channel 30 V, 0.0061  $\Omega$ , 65 A, DPAK, IPAK  
STripFET™ V Power MOSFET

## Features

Type	V <sub>DSS</sub>	R <sub>DS(on)</sub> max	I <sub>D</sub>
STD65N3LLH5	30 V	0.0069 $\Omega$	65 A
STU65N3LLH5	30 V	0.0073 $\Omega$	65 A

- R<sub>DS(on)</sub> \* Q<sub>g</sub> industry benchmark
- Extremely low on-resistance R<sub>DS(on)</sub>
- Very low switching gate charge
- High avalanche ruggedness
- Low gate drive power losses

## Application

Switching applications

## Description

This STripFET™V Power MOSFET technology is among the latest improvements, which have been especially tailored to achieve very low on-state resistance providing also one of the best-in-class figure of merit.

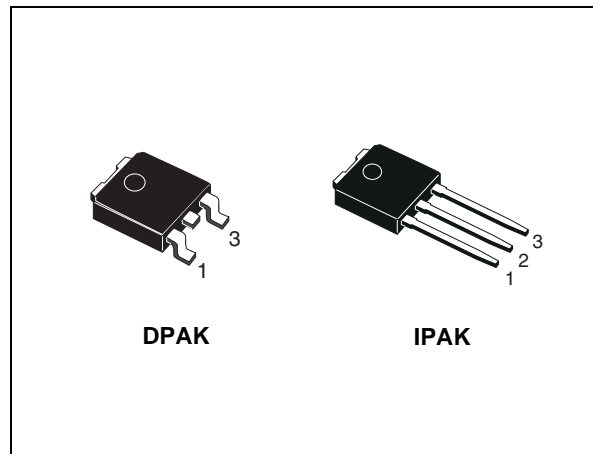


Figure 1. Internal schematic diagram

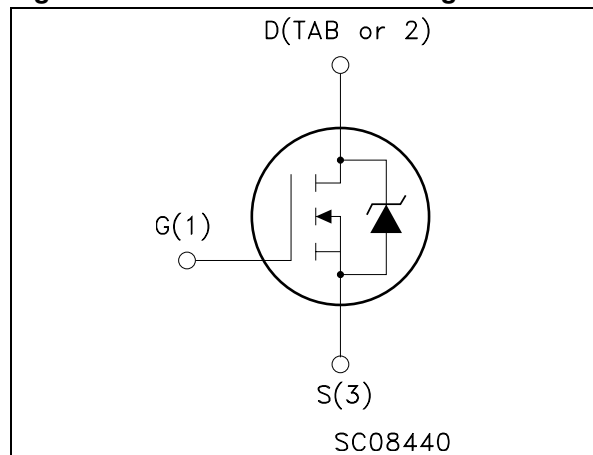


Table 1. Device summary

Order code	Marking	Package	Packaging
STD65N3LLH5	65N3LLH5	DPAK	Tape and reel
STU65N3LLH5	65N3LLH5	IPAK	Tube

# Contents

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# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage ( $V_{GS}=0$ )	30	V
$V_{GS}$	Gate-source voltage	$\pm 22$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	65	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	46	A
$I_{DM}^{(1)}$	Drain current (pulsed)	260	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	50	W
	Derating factor	0.3	W/ $^\circ\text{C}$
$E_{AS}^{(2)}$	Single pulse avalanche energy	TBD	mJ
$T_j$ $T_{stg}$	Operating junction temperature Storage temperature	-55 to 175	$^\circ\text{C}$

1. Pulse width limited by safe operating area.

2. Starting  $T_j = 25\text{ }^\circ\text{C}$ ,  $I_d = 32.5\text{ A}$ ,  $V_{dd} = 12\text{ V}$ .

**Table 3. Thermal resistance**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	3	$^\circ\text{C/W}$
$R_{thj-amb}$	Thermal resistance junction-case max	100	$^\circ\text{C/W}$
$T_j$	Maximum lead temperature for soldering purpose	275	$^\circ\text{C}$

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified).

**Table 4. Static**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown Voltage	$I_D = 250\ \mu\text{A}$ , $V_{GS} = 0$	30			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 30\text{ V}$ $V_{DS} = 30\text{ V}$ , $T_c = 125\text{ °C}$			1 10	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 22\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 250\ \mu\text{A}$	1	1.8	3	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 32.5\text{ A}$ SMD version		0.0061	0.0069	$\Omega$
		$V_{GS} = 10\text{ V}$ , $I_D = 32.5\text{ A}$		0.0065	0.0073	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 32.5\text{ A}$ SMD version		0.0084	0.0093	$\Omega$
		$V_{GS} = 4.5\text{ V}$ , $I_D = 32.5\text{ A}$		0.0088	0.0097	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 25\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0$	-	1290	-	pF
$C_{oss}$	Output capacitance			240		
$C_{rss}$	Reverse transfer capacitance			32		
$Q_g$	Total gate charge	$V_{DD} = 15\text{ V}$ , $I_D = 65\text{ A}$	-	8	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 4.5\text{ V}$		3.6		
$Q_{gd}$	Gate-drain charge	( <i>Figure 14</i> )		3.4		
$R_g$	Intrinsic gate resistance	$f = 1\text{ MHz}$ Gate DC Bias = 0 test signal level = 20 mV open drain		1.7		$\Omega$

**Table 6. Switching on/off (resistive load)**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$ $t_r$	Turn-on delay time Rise time	$V_{DD}=10\text{ V}$ , $I_D=65\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ ( <i>Figure 13</i> and <i>Figure 18</i> )	-	8.6 11.2	-	ns ns
$t_{d(off)}$ $t_f$	Turn-off delay time Fall time	$V_{DD}=10\text{ V}$ , $I_D=25\text{ A}$ , $R_G=4.7\ \Omega$ , $V_{GS}=10\text{ V}$ ( <i>Figure 13</i> and <i>Figure 18</i> )	-	32.4 6	-	ns ns

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$ $I_{SDM}$	Source-drain current Source-drain current (pulsed) <sup>(1)</sup>		-		65 260	A A
$V_{SD}$	Forward on voltage	$I_{SD}=32.5\text{ A}$ , $V_{GS}=0$	-		1.1	V
$t_{rr}$ $Q_{rr}$ $I_{RRM}$	Reverse recovery time Reverse recovery charge Reverse recovery current	$I_{SD}=32.5\text{ A}$ , $di/dt=100\text{ A}/\mu\text{s}$ , $V_{DD}=20\text{ V}$ , ( <i>Figure 15</i> )	-	22 15 1.4		ns nC A

1. Pulsed: pulse duration = 300μs, duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

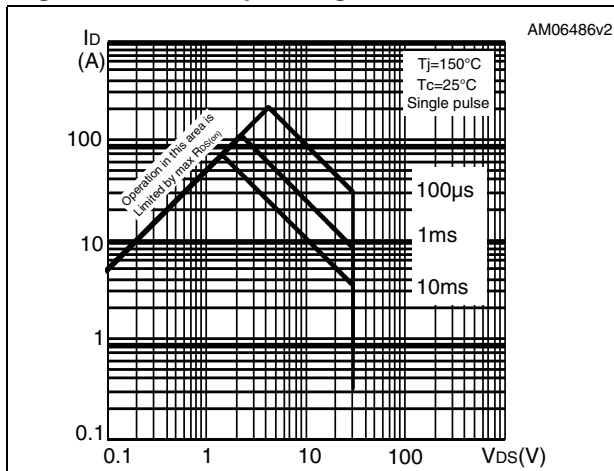


Figure 3. Thermal impedance

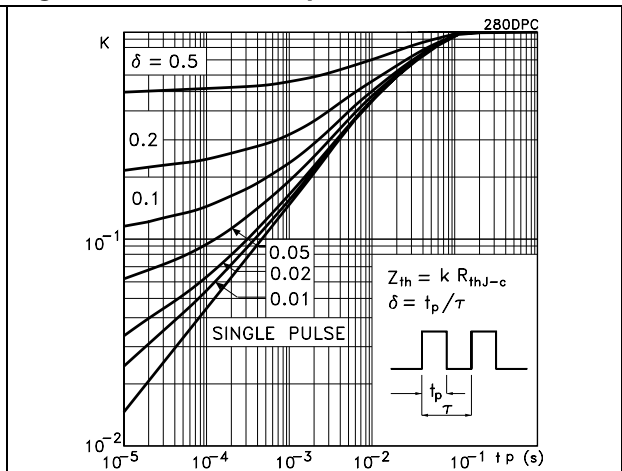


Figure 4. Output characteristics

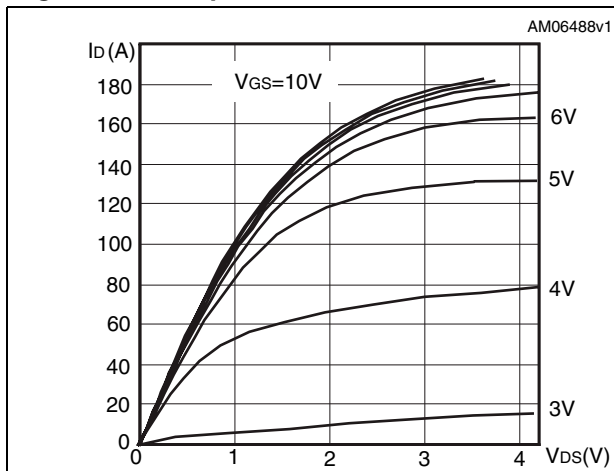


Figure 5. Transfer characteristics

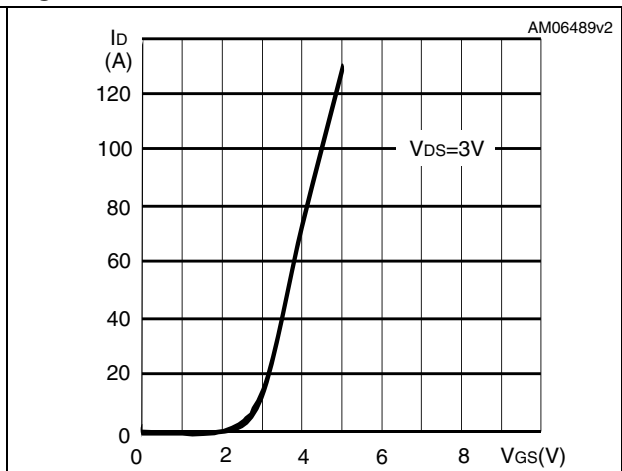


Figure 6. Normalized BV<sub>DSS</sub> vs temperature

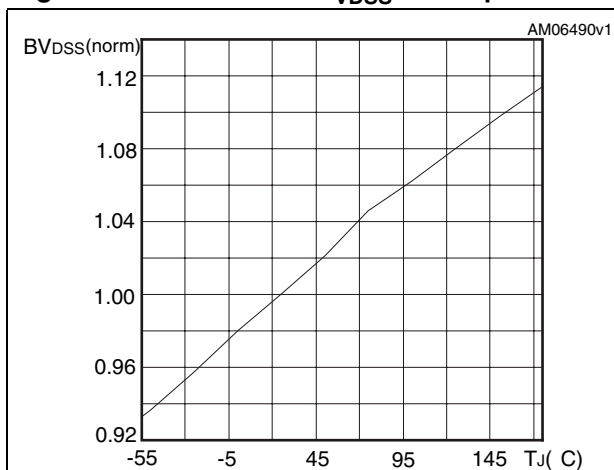


Figure 7. Static drain-source on resistance

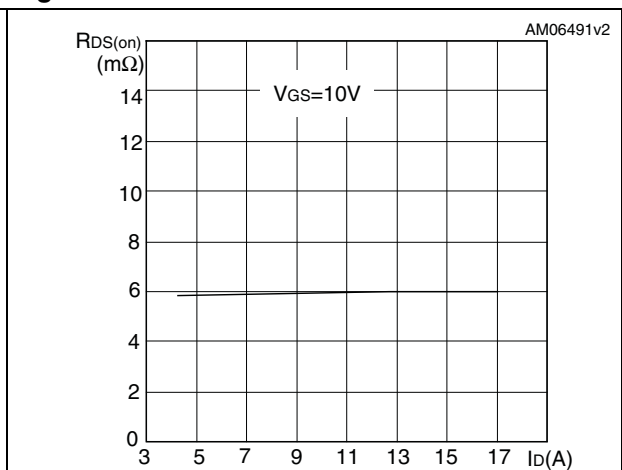


Figure 8. Gate charge vs gate-source voltage Figure 9. Capacitance variations

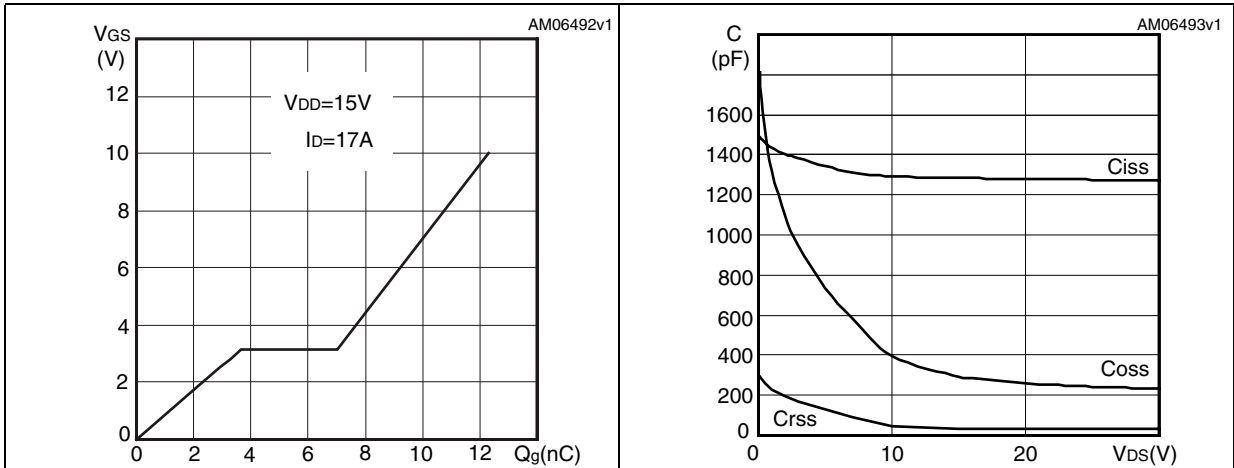


Figure 10. Normalized gate threshold voltage vs temperature Figure 11. Normalized on resistance vs temperature

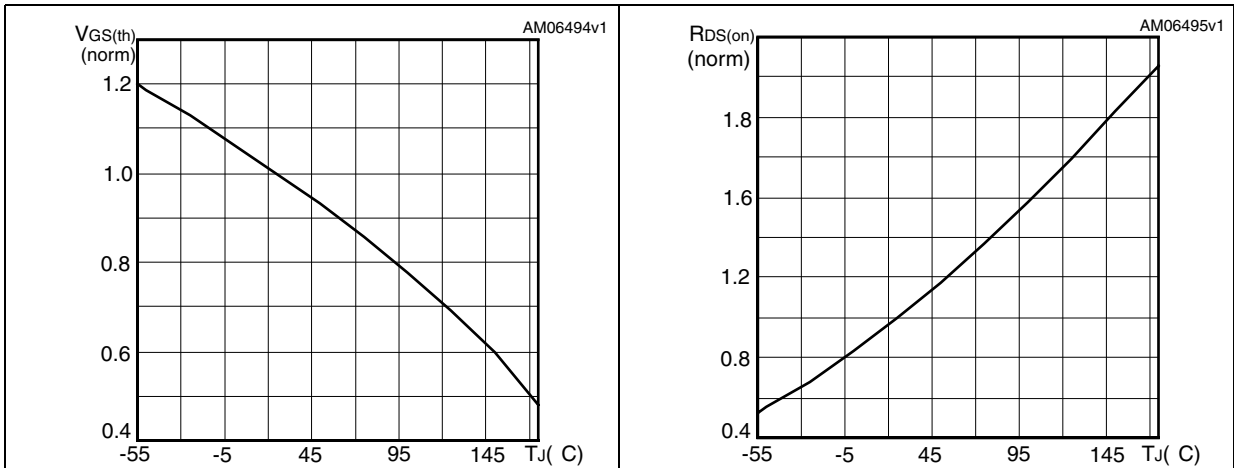
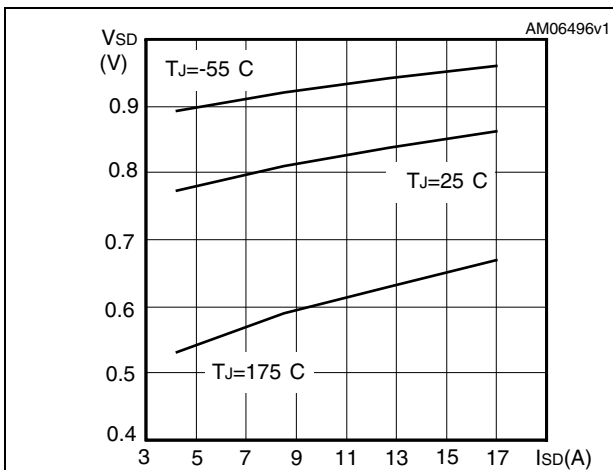
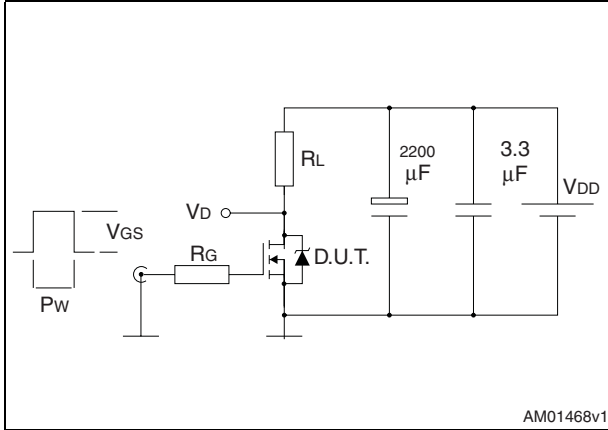


Figure 12. Source-drain diode forward characteristics



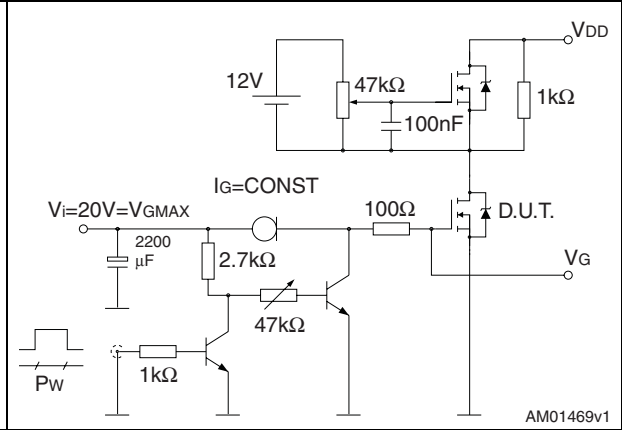
### 3 Test circuits

**Figure 13. Switching times test circuit for resistive load**



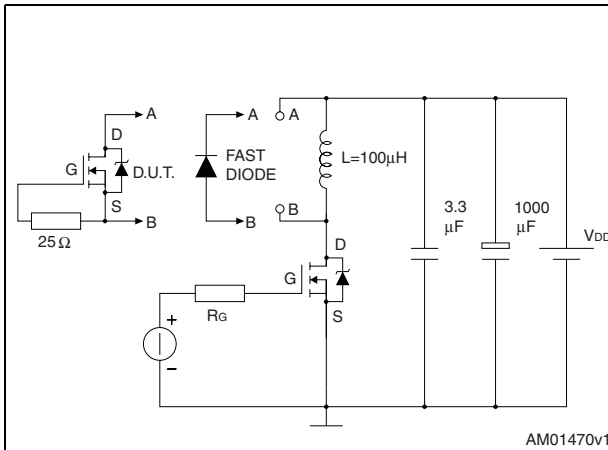
AM01468v1

**Figure 14. Gate charge test circuit**



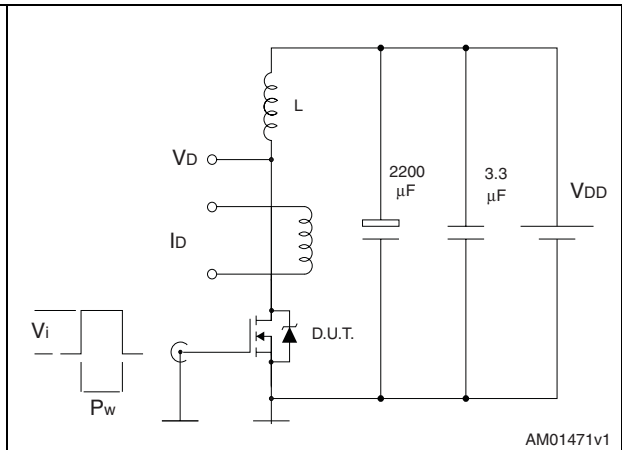
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**Figure 15. Test circuit for inductive load switching and diode recovery times**



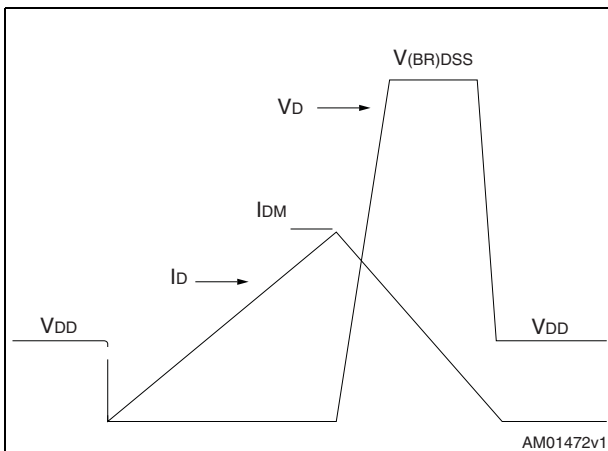
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**Figure 16. Unclamped inductive load test circuit**



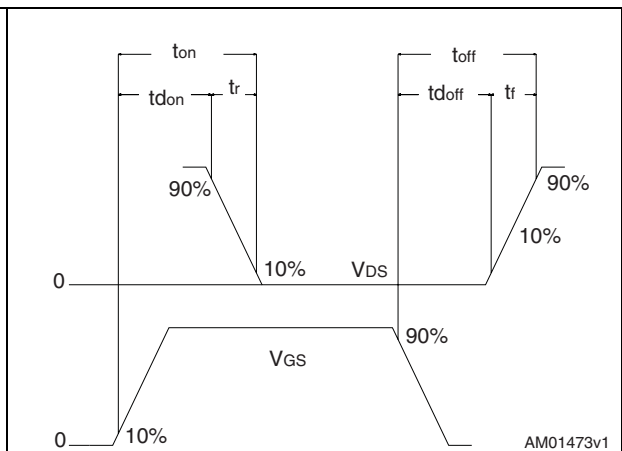
AM01471v1

**Figure 17. Unclamped inductive waveform**



AM01472v1

**Figure 18. Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.



Figure 20. DPAK (TO-252) drawing

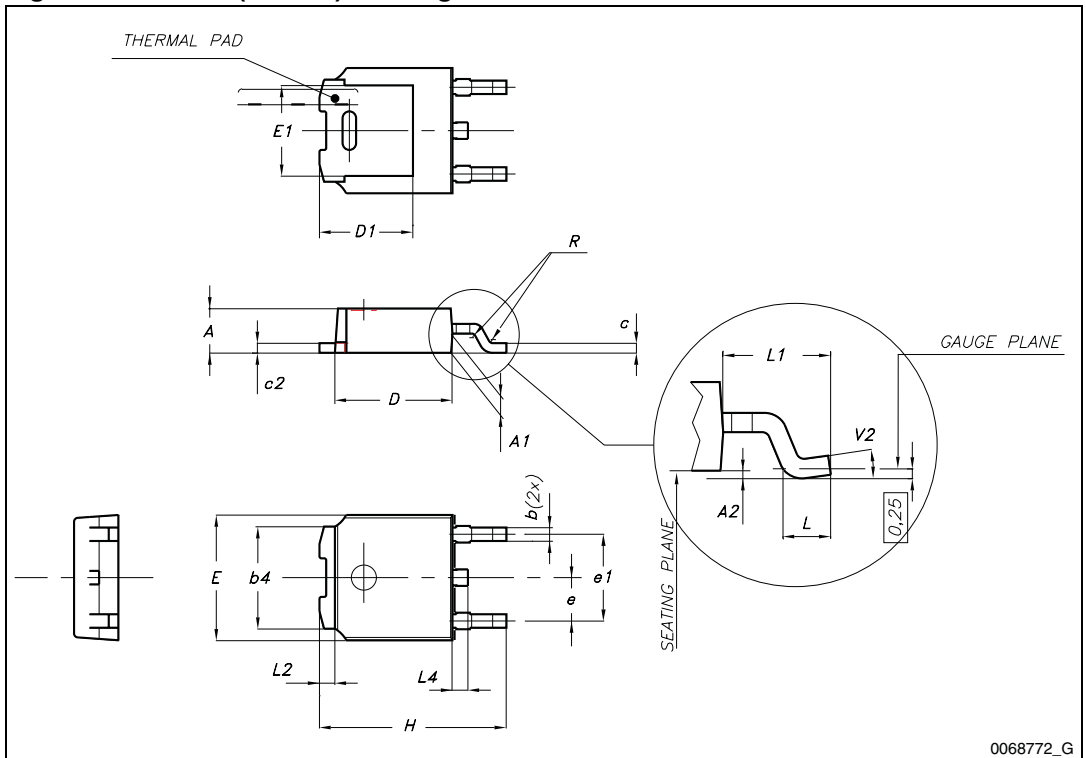
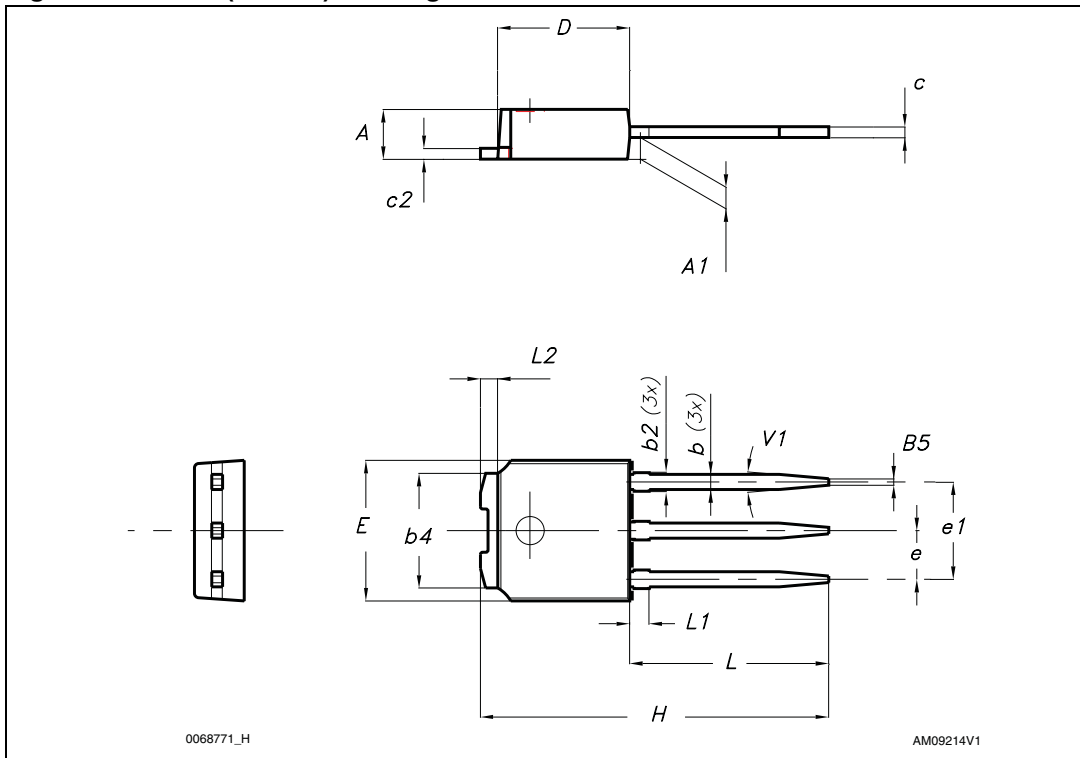


Table 9. IPAK (TO-251) mechanical data

Dim.	mm.		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.3	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

Figure 21. IPAK (TO-251) drawing



## 5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 22. Tape for DPAK (TO-252)

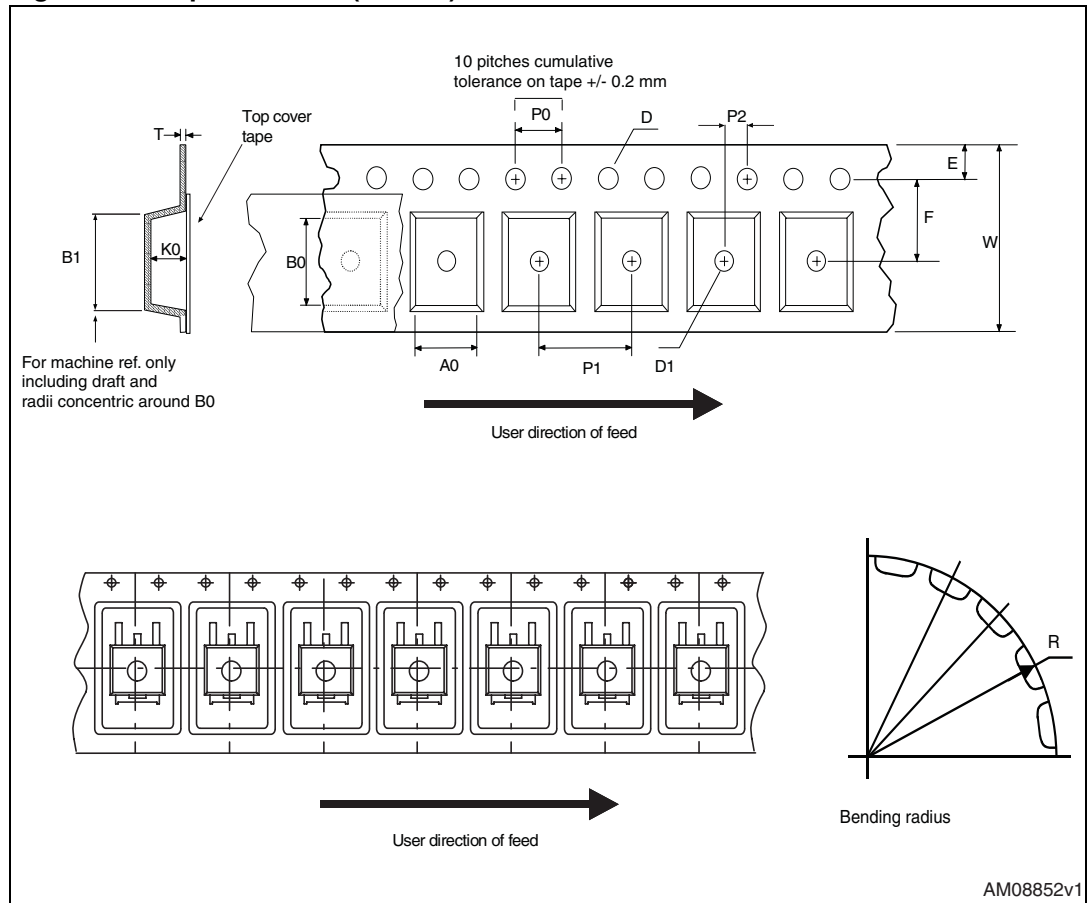
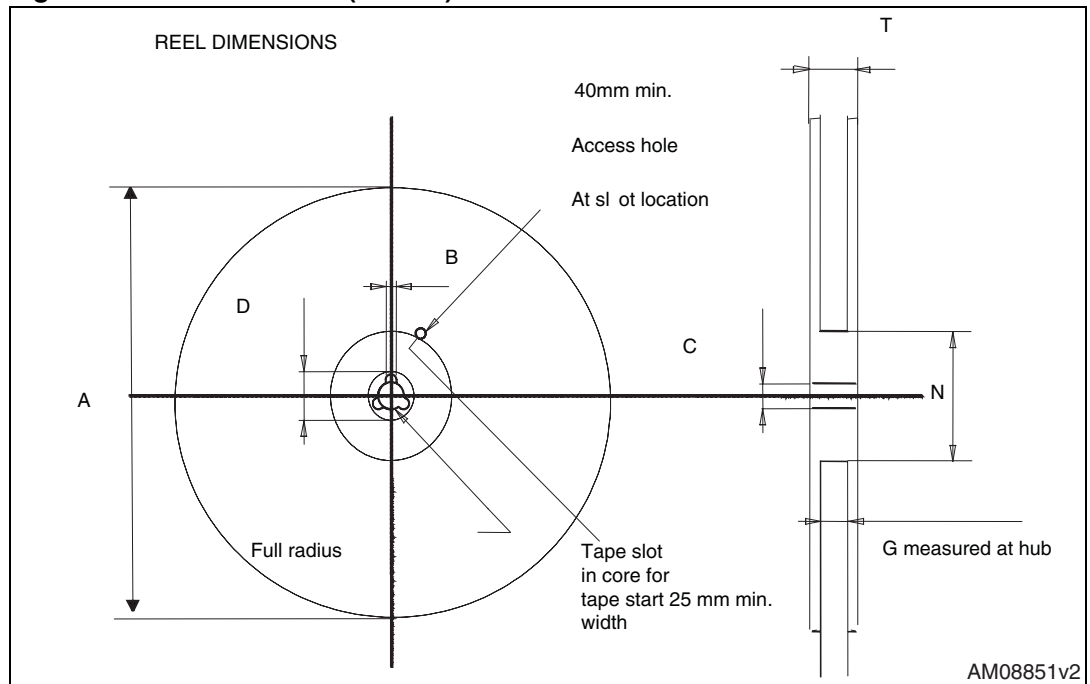


Figure 23. Reel for DPAK (TO-252)



## 6 Revision history

Table 11. Document revision history

Date	Revision	Changes
19-May-2011	1	First release.

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