



**THE DATASHEET OF
MAX6470TA25BD3+T**






300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

General Description

The MAX6469–MAX6484 are low-dropout linear regulators with a fully integrated microprocessor reset circuit. Each is available with preset output voltages from +1.5V to +3.3V in 100mV increments and delivers up to 300mA of load current. These devices consume only 82 μ A of supply current. The low supply current, low dropout voltage, and integrated reset functionality make these devices ideal for battery-powered portable equipment.

The MAX6469–MAX6484 include a reset output that indicates when the regulator output drops below standard microprocessor supply tolerances (-7.5% or -12.5% of nominal output voltage). This eliminates the need for an external microprocessor supervisor, while ensuring that supply voltages and clock oscillators have stabilized before processor activity is enabled. Push-pull and open-drain active-low reset outputs are available, with reset timeout periods of 2.5ms, 20ms, 150ms, or 1200ms (min).

The MAX6469/MAX6470/MAX6473–MAX6478/MAX6481–MAX6484 also have a shutdown feature that reduces the supply current to 0.1 μ A (typ). The MAX6471–MAX6474/MAX6479–MAX6482 offer a manual reset input to assert a microprocessor reset while the regulator output is within specification. The MAX6475/MAX6476/MAX6483/MAX6484 feature a remote feedback sense pin for use with an external NPN transistor for higher-current applications. The MAX6469–MAX6476 are available in 6-pin SOT23 and 8-pin TDFN packages. The MAX6477–MAX6484 are available in a 3 \times 3 chip-scale package (UCSP™). All devices are specified for operation from -40°C to +85°C.

Applications

Handheld Instruments (PDAs, Palmtops)
 PCMCIA Cards/USB Devices
 Cellular/Cordless Telephones
 CD/DVD Drives
 Notebook Computers
 Digital Cameras
 Bluetooth Modules/Wireless LAN

UCSP is a trademark of Maxim Integrated Products, Inc.

Pin Configurations appear at end of data sheet.

Typical Operating Circuits appear at end of data sheet.

Features

- ◆ 3 \times 3 UCSP, 6-Pin SOT23, and 8-Pin TDFN Packages
- ◆ Preset +1.5V to +3.3V Output (100mV Increments)
- ◆ SET Pin for Adjustable Output Voltage
- ◆ 75 μ V_{RMS} LDO Output Voltage Noise (MAX6477–MAX6484)
- ◆ \pm 2.0% Accuracy Over Temperature
- ◆ Guaranteed 300mA Output Current
- ◆ Low Dropout Voltage
55mV at 150mA
114mV at 300mA
- ◆ 82 μ A Supply Current, 0.1 μ A Shutdown Current
- ◆ Input Reverse Current, Thermal and Short-Circuit Protection
- ◆ Microprocessor Reset with Four Timeout Options
- ◆ Push-Pull or Open-Drain RESET
- ◆ Manual Reset Input
- ◆ Remote Feedback Sense

Ordering Information

| PART* | TEMP RANGE | PIN-PACKAGE |
|-------------------|----------------|--------------|
| MAX6469UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6469TA__D_-T** | -40°C to +85°C | 8 TDFN-EP*** |
| MAX6470UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6470TA__D_-T** | -40°C to +85°C | 8 TDFN-EP*** |

Ordering Information continued at end of data sheet.

*Devices are also available in a lead(Pb)-free/RoHS-compliant packages. Specify lead(Pb)-free by substituting a +T instead of a -T when ordering.

**Future product—contact factory for availability.

***EP = Exposed pad.

Note: The first “_” are placeholders for the output voltage levels of the devices. Desired output voltages are set by the suffix found in the Output Voltage Suffix Guide (Table 1). The third “_” is a placeholder for the reset threshold accuracy. Desired reset threshold accuracy is set by the suffix found in the Reset Threshold Accuracy Guide (Table 2). The “_” following the D is a placeholder for the reset timeout delay time. Desired reset timeout delay time is set by the suffix found in the Reset Timeout Delay Guide (Table 3). For example, the MAX6481BL30BD4-T has a 3.0V output voltage, 12.5% reset threshold tolerance, and a 1200ms (min) reset timeout delay. Sample stock is generally available on standard versions only (Table 4). Standard versions require a minimum order increment of 2.5k units. Nonstandard versions must be ordered in 10k-unit increments. Contact factory for availability.



300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND, unless otherwise noted.)

| | |
|---|------------------------------------|
| IN, SHDN, OUT, FB | -0.3V to +7V |
| MR, SET | -0.3V to (V _{IN} + 0.3V) |
| RESET (push-pull) | -0.3V to (V _{OUT} + 0.3V) |
| RESET (open drain) | -0.3V to +7V |
| OUT Short Circuit | Continuous |
| Input/Output Current (all pins except IN and OUT) | 20mA |
| Continuous Power Dissipation (T _A = +70°C) | |
| 3 x 3 UCSP (derate 10.5mW/°C above +70°C) | 840mW |

| | |
|---|-----------------|
| 6-Pin SOT23 (derate 9.1mW/°C above +70°C) | 727mW |
| 8-Pin TDFN (derate 24.4mW/°C above +70°C) | 1951mW |
| Operating Temperature Range | -40°C to +85°C |
| Junction Temperature | +150°C |
| Storage Temperature Range | -65°C to +150°C |
| Lead Temperature (soldering, 10s) | +300°C |
| Soldering Temperature (reflow) | |
| Lead(Pb)-free packages | +260°C |
| Packages containing lead(Pb) | +240°C |

Note 1: The MAX6477-MAX6484 are constructed using a unique set of packaging techniques that impose a limit on the thermal profile the devices can be exposed to during board-level solder attach and rework. This limit permits only the use of the solder profiles recommended in the industry-standard specification, JEDEC 020A, paragraph 7.6, Table 3 for IR/VPR and Convection reflow. Pre-heating is required. Hand or wave soldering is not allowed.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN} = (V_{OUT} + 0.5V) or +2.5V, whichever is greater, C_{OUT} = 3.3μF, T_A = -40°C to +85°C. Typical specifications are at T_A = +25°C, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|---|-------------------|--|------------------|-------|-------|-------|
| Input Voltage Range | V _{IN} | | 2.5 | | 5.5 | V |
| Input Undervoltage Lockout | V _{UVLO} | V _{IN} falling | 2.25 | | 2.47 | V |
| Supply Current (Ground Current) | I _Q | I _{OUT} = 0A | | 82 | 136 | μA |
| | | I _{OUT} = 300mA | | 96 | | |
| Shutdown Supply Current | I _{SHDN} | T _A = +25°C | | 0.1 | 1 | μA |
| REGULATOR CIRCUIT | | | | | | |
| Output Current | | | 300 | | | mA |
| Output Voltage Accuracy (Fixed Output Voltage Operation, Table 1) MAX6469-MAX6476 | | 1mA ≤ I _{OUT} ≤ 150mA, T _A = +25°C | -1.3 | | +1.3 | % |
| | | 1mA ≤ I _{OUT} ≤ 150mA, T _A = -40°C to +85°C | -2.3 | | +2.3 | |
| | | 1mA ≤ I _{OUT} ≤ 300mA, T _A = -40°C to +85°C | -2.7 | | +2.7 | |
| Output Voltage Accuracy (Fixed Output Voltage Operation, Table 1) MAX6477-MAX6484 | | 2mA ≤ I _{OUT} ≤ 100mA, T _A = +25°C | -1.1 | | +1.1 | % |
| | | 2mA ≤ I _{OUT} ≤ 100mA, T _A = -40°C to +85°C | -2.0 | | +2.0 | |
| | | 2mA ≤ I _{OUT} ≤ 300mA, T _A = -40°C to +85°C (Note 3) | -2.5 | | +2.5 | |
| Adjustable Output Voltage Range | | | V _{SET} | | 5.0 | V |
| SET Reference Voltage | V _{SET} | | 1.200 | 1.229 | 1.258 | V |
| SET Dual Mode™ Threshold | | | | 185 | | mV |
| SET Input Leakage Current | I _{SET} | V _{SET} = 0V, +1.2V (Note 3) | | ±20 | ±100 | nA |

Dual Mode is a trademark of Maxim Integrated Products, Inc.

300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

MAX6469-MAX6484

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = (V_{OUT} + 0.5V)$ or $+2.5V$, whichever is greater, $C_{OUT} = 3.3\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical specifications are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | | MIN | TYP | MAX | UNITS |
|---|-------------------|---|-------------------|---------------------|------|---------------------|---------------|
| Dropout Voltage (Notes 3, 4) | ΔV_{DO} | $V_{OUT} = +3.3V$ (fixed output operation) | $I_{OUT} = 50mA$ | | 23 | 32 | mV |
| | | | $I_{OUT} = 150mA$ | | 55 | 90 | |
| | | | $I_{OUT} = 300mA$ | | 114 | 180 | |
| | | $V_{OUT} = +3.0V$ (fixed output operation) | $I_{OUT} = 50mA$ | | 25 | 40 | |
| | | | $I_{OUT} = 150mA$ | | 61 | 100 | |
| | | | $I_{OUT} = 300mA$ | | 114 | 190 | |
| | | $V_{OUT} = +2.8V$ (fixed output operation) | $I_{OUT} = 50mA$ | | 26 | 50 | |
| | | | $I_{OUT} = 150mA$ | | 65 | 110 | |
| | | | $I_{OUT} = 300mA$ | | 137 | 210 | |
| | | $V_{OUT} = +2.5V$ (fixed output operation) | $I_{OUT} = 50mA$ | | 30 | 60 | |
| | | | $I_{OUT} = 150mA$ | | 75 | 150 | |
| | | | $I_{OUT} = 300mA$ | | 158 | 250 | |
| Output Current Limit | | $V_{IN} \geq 2.5V$ (Note 3) | 450 | | | | mA |
| Input Reverse Leakage Current (OUT to IN Leakage Current) | | $V_{IN} = 4V$, $V_{OUT} = 5.5V$, \overline{SHDN} deasserted | | 0.01 | 1.5 | | μA |
| Startup Time Response | | Rising edge of V_{IN} or \overline{SHDN} to V_{OUT} within specification, $R_L = 68\Omega$, $SET = GND$, $I_{OUT} = 10mA$ | | 20 | | | μs |
| \overline{SHDN} Input Low Voltage | V_{IL} | | | | | $0.3 \times V_{IN}$ | V |
| \overline{SHDN} Input High Voltage | V_{IH} | | | $0.7 \times V_{IN}$ | | | V |
| \overline{SHDN} Input Current | | $V_{\overline{SHDN}} = V_{IN}$ or V_{GND} | -1 | 0.1 | +1 | | μA |
| Thermal-Shutdown Temperature | T_{SHDN} | | | 180 | | | $^\circ C$ |
| Thermal-Shutdown Hysteresis | ΔT_{SHDN} | | | 20 | | | $^\circ C$ |
| Line Regulation | | $V_{OUT} = 1.5V$, $2.5V \leq V_{IN} \leq 5.5V$, $I_{OUT} = 10mA$ | | 0.09 | | | %/V |
| Load Regulation | | $V_{OUT} = 1.5V$, $V_{IN} = 2.5V$, $1mA \leq I_{OUT} \leq 150mA$ | | 0.2 | | | % |
| Output Voltage Noise | | 10Hz to 100kHz, $C_{IN} = 0.1\mu F$, $I_{OUT} = 100mA$, $V_{OUT} = 1.5V$ | MAX6469-MAX6476 | | 150 | | μV_{RMS} |
| | | | MAX6477-MAX6484 | | 75 | | |
| RESET CIRCUIT | | | | | | | |
| V_{OUT} Reset Threshold (V_{FB} for MAX6475/MAX6476/ MAX6483/MAX6484) (Note 5) | V_{THOUT} | MAX64_____A | 90 | 92.5 | 95 | | % V_{OUT} |
| | | MAX64_____B | 85 | 87.5 | 90 | | |
| V_{OUT} to Reset Delay (V_{FB} for MAX6475/MAX6476/ MAX6483/MAX6484) | | | | 35 | | | μs |
| Reset Timeout Period (Note 6) | t_{RP} | D1 | 2.5 | 3.75 | 5.0 | | ms |
| | | D2 | 20 | 30 | 40 | | |
| | | D3 | 150 | 225 | 300 | | |
| | | D4 | 1200 | 1800 | 2400 | | |

300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

ELECTRICAL CHARACTERISTICS (continued)

($V_{IN} = (V_{OUT} + 0.5V)$ or $+2.5V$, whichever is greater, $C_{OUT} = 3.3\mu F$, $T_A = -40^\circ C$ to $+85^\circ C$. Typical specifications are at $T_A = +25^\circ C$, unless otherwise noted.) (Note 2)

| PARAMETER | SYMBOL | CONDITIONS | MIN | TYP | MAX | UNITS |
|--|-----------|---|----------------------|-----|----------------------|-----------|
| \overline{MR} Input Low Voltage | V_{IL} | | | | $0.3 \times V_{OUT}$ | V |
| \overline{MR} Input High Voltage | V_{IH} | (Note 3) | $0.7 \times V_{OUT}$ | | | V |
| \overline{MR} Minimum Input Pulse | | | 1 | | | μs |
| \overline{MR} Glitch Rejection | | | | 120 | | ns |
| \overline{MR} to Reset Delay | | | | 200 | | ns |
| \overline{MR} Pullup Resistance | | \overline{MR} to OUT | 25 | 40 | 70 | $k\Omega$ |
| \overline{RESET} Output Voltage (Open Drain) | V_{OL} | $V_{OUT} \geq 1.0V$, $I_{SINK} = 50\mu A$, \overline{RESET} asserted | | | 0.3 | V |
| | | $V_{OUT} \geq 1.5V$, $I_{SINK} = 3.2mA$, \overline{RESET} asserted | | | 0.4 | |
| Open-Drain Reset Output Leakage Current | I_{LKG} | (Note 3) | | | 1 | μA |
| \overline{RESET} Output Voltage Push-Pull | V_{OL} | $V_{OUT} \geq 1.0V$, $I_{SINK} = 50\mu A$, \overline{RESET} asserted | | | 0.3 | V |
| | | $V_{OUT} \geq 1.5V$, $I_{SINK} = 3.2mA$, \overline{RESET} asserted | | | 0.4 | |
| | V_{OH} | $V_{OUT} \geq 2.0V$, $I_{SOURCE} = 500\mu A$, \overline{RESET} deasserted | $0.8 \times V_{OUT}$ | | | |

Note 2: All devices are 100% production tested at $+25^\circ C$ and are guaranteed by correlation for $T_A = T_{MIN}$ to T_{MAX} .

Note 3: Guaranteed by design.

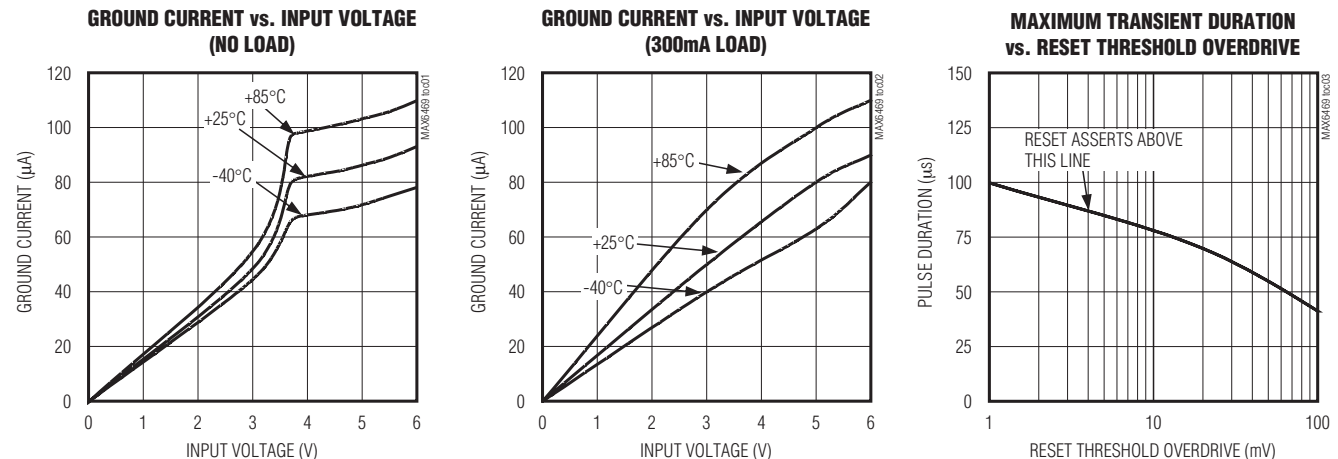
Note 4: Dropout voltage is defined as $(V_{IN} - V_{OUT})$ when V_{OUT} is 2% below the value of V_{OUT} for $V_{IN} = V_{OUT(NOM)} + 1V$.

Note 5: MAX6473/MAX6474/MAX6481/MAX6482 are guaranteed by design for $V_{OUT} < 2.5V$.

Note 6: Select the reset timeout period using the *Reset Timeout Delay Guide* (Table 3). Insert the appropriate suffix in the part number when ordering.

Typical Operating Characteristics

($V_{IN} = 5V$, $V_{OUT} = 3.3V$, $C_{OUT} = 3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

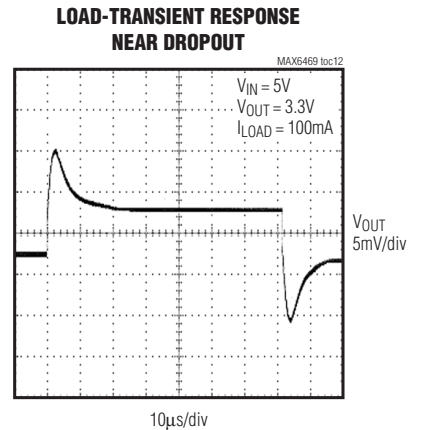
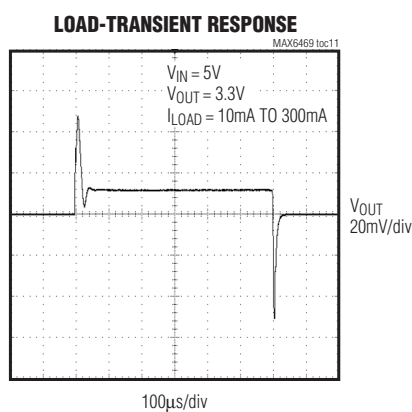
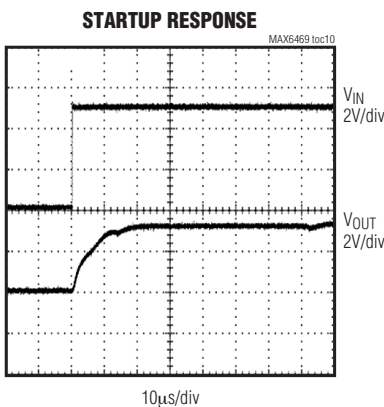
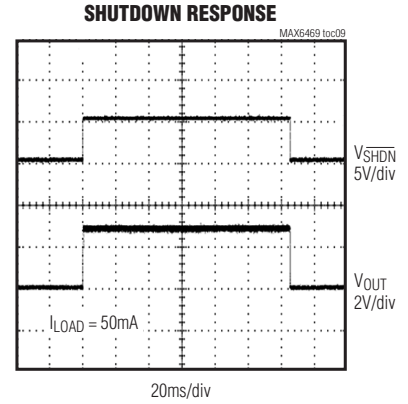
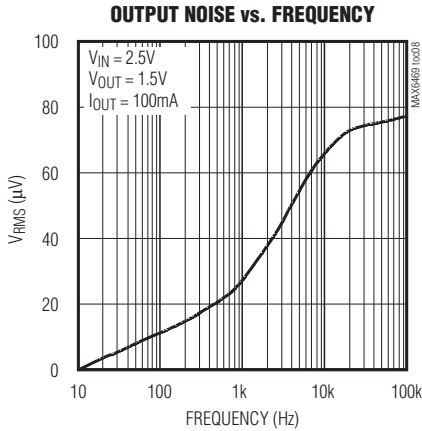
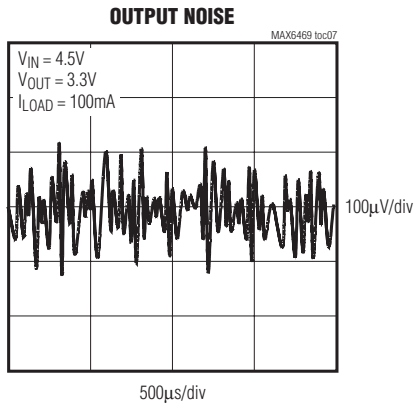
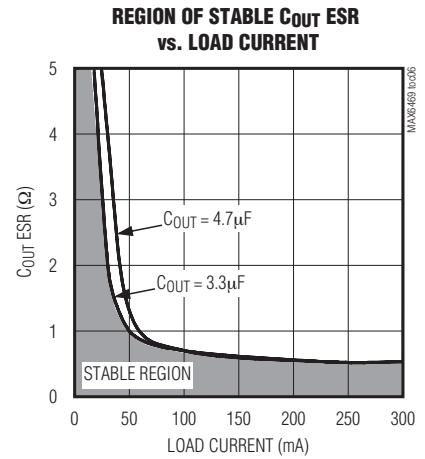
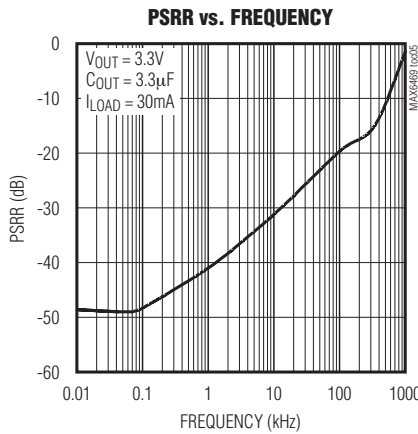
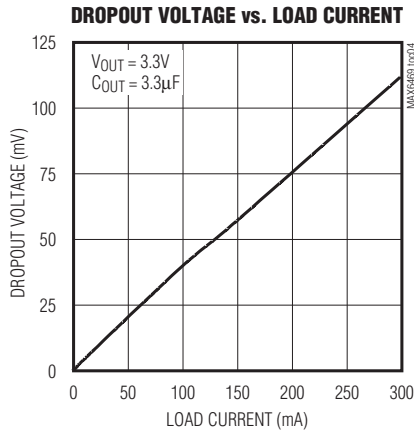


300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

Typical Operating Characteristics (continued)

($V_{IN} = 5V$, $V_{OUT} = 3.3V$, $C_{OUT} = 3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)

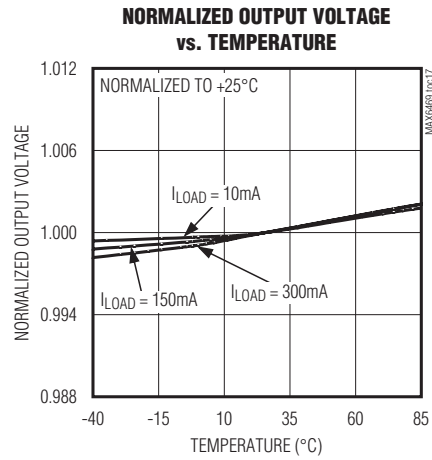
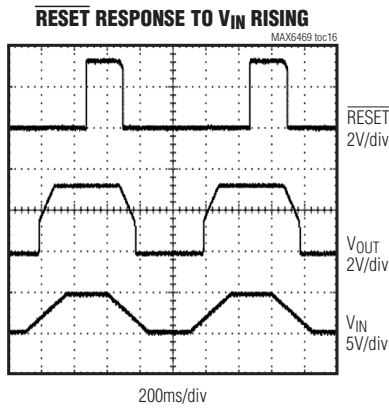
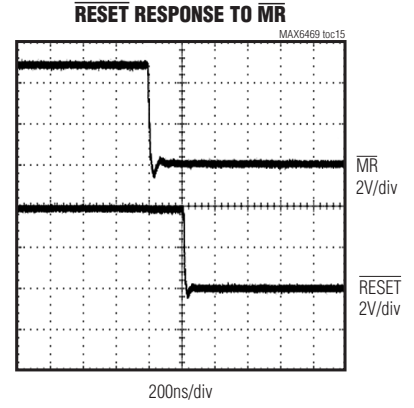
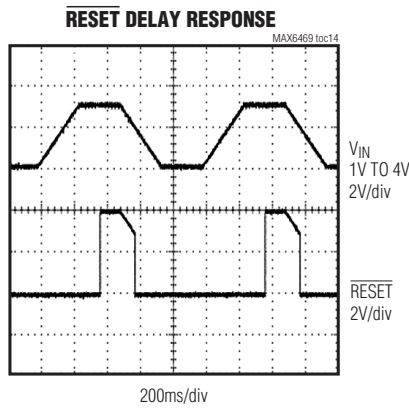
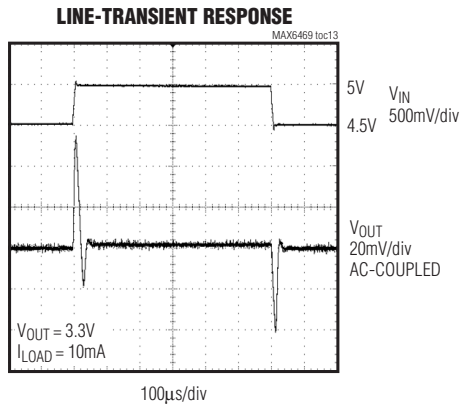
MAX6469-MAX6484



300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

Typical Operating Characteristics (continued)

($V_{IN} = 5V$, $V_{OUT} = 3.3V$, $C_{OUT} = 3.3\mu F$, $T_A = +25^\circ C$, unless otherwise noted.)



300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

MAX6469/MAX6470/MAX6477/MAX6478 Pin Description

| PIN | | BUMP | NAME | FUNCTION |
|-----------------|---------|-----------------|---------------------------|--|
| MAX6469/MAX6470 | | MAX6477/MAX6478 | | |
| SOT23 | TDFN-EP | UCSP | | |
| 1 | 1, 2 | A1 | IN | Regulator Input. Bypass IN to GND with a 0.1μF capacitor. |
| 2 | 3 | A2 | GND | Ground. This pin also functions as a heatsink. Solder to large pads or the circuit-board ground plane to maximize thermal dissipation. |
| 3 | 4 | A3 | $\overline{\text{SHDN}}$ | Active-Low Shutdown Input. Connect $\overline{\text{SHDN}}$ to V_{IN} for normal operation. |
| 4 | 5 | C3 | $\overline{\text{RESET}}$ | Active-Low Reset Output. $\overline{\text{RESET}}$ remains low while V_{OUT} is below the reset threshold. $\overline{\text{RESET}}$ remains low for the duration of the reset timeout period after the reset conditions are terminated. $\overline{\text{RESET}}$ is available in open-drain and push-pull configurations. |
| 5 | 6 | C2 | SET | Feedback Input for Externally Setting the Output Voltage. Connect SET to GND to select the preset output voltage. Connect SET to an external resistor-divider network for adjustable output operation. |
| 6 | 7, 8 | C1 | OUT | Regulator Output. Bypass OUT to GND with a minimum 3.3μF low-ESR capacitor. |
| — | — | — | EP | Exposed Paddle (TDFN Only). EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal-resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

MAX6471/MAX6472/MAX6479/MAX6480 Pin Description

| PIN | | BUMP | NAME | FUNCTION |
|-----------------|---------|-----------------|---------------------------|---|
| MAX6471/MAX6472 | | MAX6479/MAX6480 | | |
| SOT23 | TDFN-EP | UCSP | | |
| 1 | 1, 2 | A1 | IN | Regulator Input. Bypass IN to GND with a 0.1μF capacitor. |
| 2 | 3 | A2 | GND | Ground. This pin also functions as a heatsink. Solder to large pads or the circuit-board ground plane to maximize thermal dissipation. |
| 3 | 4 | A3 | $\overline{\text{MR}}$ | Active-Low Manual Reset Input. The reset output is asserted while $\overline{\text{MR}}$ is pulled low and remains asserted for the duration of the reset timeout period after $\overline{\text{MR}}$ transitions from low to high. Leave $\overline{\text{MR}}$ unconnected or connect to V_{OUT} if not used. $\overline{\text{MR}}$ has an internal pullup resistor of 40kΩ (typ) to V_{OUT} . |
| 4 | 5 | C3 | $\overline{\text{RESET}}$ | Active-Low Reset Output. $\overline{\text{RESET}}$ remains low while V_{OUT} is below the reset threshold or while $\overline{\text{MR}}$ is held low. $\overline{\text{RESET}}$ remains low for the duration of the reset timeout period after the reset conditions are terminated. $\overline{\text{RESET}}$ is available in open-drain and push-pull configurations. |
| 5 | 6 | C2 | SET | Feedback Input for Externally Setting the Output Voltage. Connect SET to GND to select the preset output voltage. Connect SET to an external resistor-divider network for adjustable output operation. |
| 6 | 7, 8 | C1 | OUT | Regulator Output. Bypass OUT to GND with a minimum 3.3μF low-ESR capacitor. |
| — | — | — | EP | Exposed Paddle (TDFN Only). EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal-resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

MAX6469-MAX6484

300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

MAX6473/MAX6474/MAX6481/MAX6482 Pin Description

| PIN | | BUMP | NAME | FUNCTION |
|-----------------|---------|-----------------|---------------------------|---|
| MAX6473/MAX6474 | | MAX6481/MAX6482 | | |
| SOT23 | TDFN-EP | UCSP | | |
| 1 | 1, 2 | A1 | IN | Regulator Input. Bypass IN to GND with a 0.1µF capacitor. |
| 2 | 3 | A2 | GND | Ground. This pin also functions as a heatsink. Solder to large pads or the circuit-board ground plane to maximize thermal dissipation. |
| 3 | 4 | A3 | $\overline{\text{SHDN}}$ | Active-Low Shutdown Input. Connect $\overline{\text{SHDN}}$ to V_{IN} for normal operation. |
| 4 | 5 | C3 | $\overline{\text{RESET}}$ | Active-Low Reset Output. $\overline{\text{RESET}}$ remains low while V_{OUT} is below the reset threshold or while $\overline{\text{MR}}$ is held low. $\overline{\text{RESET}}$ remains low for the duration of the reset timeout period after the reset conditions are terminated. $\overline{\text{RESET}}$ is available in open-drain and push-pull configurations. |
| 5 | 6 | C2 | $\overline{\text{MR}}$ | Active-Low Manual Reset Input. The reset output is asserted while $\overline{\text{MR}}$ is pulled low and remains asserted for the duration of the reset timeout period after $\overline{\text{MR}}$ transitions from low to high. Leave $\overline{\text{MR}}$ unconnected or connect to V_{OUT} if not used. $\overline{\text{MR}}$ has an internal pullup resistor of 40kΩ (typ) to V_{OUT} . |
| 6 | 7, 8 | C1 | OUT | Regulator Output. Bypass OUT to GND with a minimum 3.3µF (min) low-ESR capacitor. |
| — | — | — | EP | Exposed Paddle (TDFN Only). EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal-resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

MAX6475/MAX6476/MAX6483/MAX6484 Pin Description

| PIN | | BUMP | NAME | FUNCTION |
|-----------------|---------|-----------------|---------------------------|--|
| MAX6475/MAX6476 | | MAX6483/MAX6484 | | |
| SOT23 | TDFN-EP | UCSP | | |
| 1 | 1, 2 | A1 | IN | Regulator Input. Bypass IN to GND with a 0.1µF capacitor. |
| 2 | 3 | A2 | GND | Ground. This pin also functions as a heatsink. Solder to large pads or the circuit-board ground plane to maximize thermal dissipation. |
| 3 | 4 | A3 | $\overline{\text{SHDN}}$ | Active-Low Shutdown Input. Connect $\overline{\text{SHDN}}$ to V_{IN} for normal operation. |
| 4 | 5 | C3 | $\overline{\text{RESET}}$ | Active-Low Reset Output. $\overline{\text{RESET}}$ remains low while FB is below the reset threshold. $\overline{\text{RESET}}$ remains low for the duration of the reset timeout period after the reset conditions are terminated. $\overline{\text{RESET}}$ is available in open-drain and push-pull configurations. |
| 5 | 6 | C2 | FB | Feedback Input for Linear Regulator Controller or Remote Sense Applications. Connect FB to the external load (V_{CC}) to obtain the fixed output voltage. |
| 6 | 7, 8 | C1 | OUT | Regulator Output. Bypass OUT to GND with a minimum 3.3µF low-ESR capacitor. |
| — | — | — | EP | Exposed Paddle (TDFN Only). EP is internally connected to GND. Connect EP to the ground plane to provide a low thermal-resistance path from the IC junction to the PCB. Do not use as the electrical connection to GND. |

300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

Detailed Description

The MAX6469–MAX6484 are ultra-low, quiescent current, low-dropout linear regulators with an integrated microprocessor reset circuit. These devices guarantee 300mA (min) drive capabilities and are available with preset output voltages in 100mV increments between +1.5V and +3.3V. The internal reset circuit monitors the regulator output voltage and asserts the reset output when the regulator output is below the microprocessor supply tolerance.

Regulator

The regulator core operates with +2.5V to +5.5V input voltage range. The output voltage is offered in 100mV increments between +1.5V and +3.3V (contact factory for other output voltage options). The MAX6469–MAX6472/MAX6477–MAX6480 offer an adjustable output voltage implemented with an external resistor-divider network between OUT, SET, and GND (Figure 1). SET must be connected to either GND for fixed V_{OUT} or to an external divider for adjustable V_{OUT} . The MAX6469–MAX6472/MAX6477–MAX6480 automatically determine the feedback path depending on the connection of SET. The *Typical Operating Circuit* shows a typical connection for the MAX6469. OUT is an internally regulated low-dropout (LDO) linear regulator that powers a microprocessor.

Reset Circuit

The reset supervisor circuit is fully integrated in the MAX6469–MAX6484 and uses the same reference voltage as the regulator. Two supply tolerance reset thresholds, -7.5% and -12.5%, are provided for each type of device.

-7.5% Reset: Reset does not assert until the regulator output voltage is at least -5% out of tolerance and always asserts before the regulator output voltage is -10% out of tolerance.

-12.5% Reset: Reset does not assert until the regulator output voltage is at least -10% out of tolerance and always asserts before the regulator output voltage is -15% out of tolerance.

RESET Output

A μP 's reset input starts the μP in a known state. The MAX6469–MAX6484 μP supervisory circuits assert $\overline{\text{RESET}}$ during power-up, power-down, and brownout conditions. $\overline{\text{RESET}}$ asserts when the input voltage is below the undervoltage lockout threshold. $\overline{\text{RESET}}$ asserts when V_{OUT} is below the reset threshold and remains asserted for at least the minimum selected reset timeout period (t_{RP} , Table 3) after V_{IN} rises above the undervoltage lockout threshold and V_{OUT} rises above

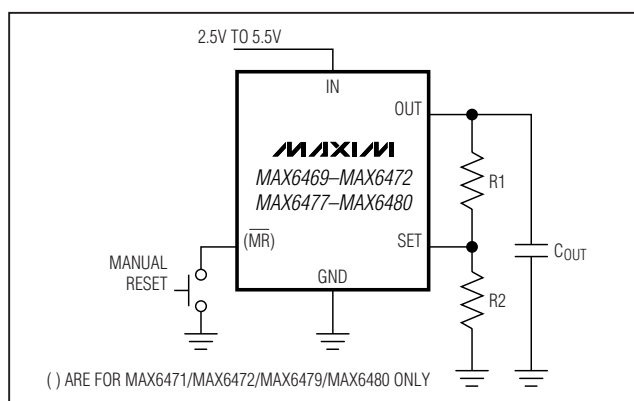


Figure 1. Adjustable Output Voltage Configuration

the reset threshold. $\overline{\text{RESET}}$ asserts when $\overline{\text{MR}}$ is pulled low (MAX6471–MAX6474/MAX6479–MAX6482). $\overline{\text{RESET}}$ asserts when $\overline{\text{SHDN}}$ is pulled low (MAX6469/MAX6470/MAX6473–MAX6478/MAX6481–MAX6484).

Shutdown (MAX6469/MAX6470/MAX6473–MAX6478/MAX6481–MAX6484 only)

$\overline{\text{SHDN}}$ allows the regulator to shut down, thereby reducing the total I_{IN} consumption of the device. $\overline{\text{SHDN}}$ provides a digitally controlled active-low shutdown. In shutdown mode, the pass transistor, control circuit, and reference turn off to reduce the supply current to below 0.1 μA . Connect $\overline{\text{SHDN}}$ to IN for normal operation.

Manual Reset Input (MAX6471–MAX6474/MAX6479–MAX6482 only)

Many μP -based products require manual reset capability, allowing the operator, a test technician, or external logic circuitry to initiate a reset. A logic low on $\overline{\text{MR}}$ asserts reset while the regulator output voltage is still within tolerance.

Reset remains asserted while $\overline{\text{MR}}$ is low and for the reset timeout period (t_{RP}) after $\overline{\text{MR}}$ returns high. The $\overline{\text{MR}}$ input has an internal pullup of 40k Ω (typ) to OUT. $\overline{\text{MR}}$ can be driven with TTL/CMOS logic levels or with open-drain/collector outputs. Connect a normally open switch from $\overline{\text{MR}}$ to GND to create a manual reset function; external debounce circuitry is not required. If $\overline{\text{MR}}$ is driven from long cables or the device is used in a noisy environment, connect a 0.1 μF capacitor from $\overline{\text{MR}}$ to GND to provide additional noise immunity.

Feedback Input (MAX6475/MAX6476/MAX6483/MAX6484 only)

The feedback input (FB) connects to an internal resistor-divider network (*Functional Diagram*). FB is not internally connected to V_{OUT} , and as a result can be used to

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remotely sense the output voltage of the device. Using FB with an external npn transistor, the current drive capability can be increased according to the following equation (Figure 2):

$$I_{OUT(TOTAL)} = I_{OUT} \times (\beta + 1)$$

The external npn pass transistor must meet specifications for current gain, power dissipation, and collector current. The beta influences the maximum output current the circuit can deliver. The largest guaranteed output current is given by $I_{LOAD(max)} = 300mA \times \beta$ (min). The transistor's rated power dissipation must exceed the actual power dissipated in the transistor. The power dissipated (PD) equals the maximum load current ($I_{LOAD(max)}$) times the maximum input-to-output voltage differential: $PD = I_{LOAD(max)} \times (V_{IN(max)} - V_{OUT})$. The rated transistor collector current must exceed the maximum load current.

Reverse Leakage Protection

Reverse OUT to IN Current

An internal circuit monitors the MAX6469-MAX6484 input and output voltages. When the output voltage is greater than the input voltage, the internal IN-to-OUT pass transistor and parasitic diode turn off. An external voltage applied to OUT does not reverse charge a battery or power source applied to IN (the leakage path from OUT to IN is 0.01µA typ). When the output voltage exceeds the input voltage, OUT powers the device and shutdown must be logic high (greater than 0.7 × V_{OUT}). RESET asserts until IN exceeds OUT and OUT is above the specified V_{THOUT} threshold (based on the selected or adjusted regulator OUT nominal voltage).

Reverse OUT to Ground Current

The MAX6469-MAX6484 maintain a low OUT-to-GND reverse-current flow when the IN power source is removed. When IN floats (input battery removed) and SHDN is pulled up to V_{OUT} (by an external diode), the

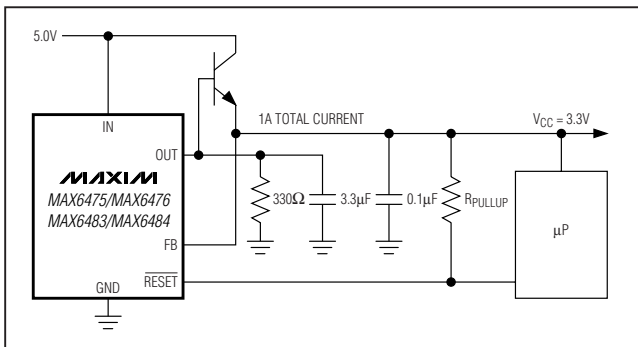


Figure 2. High-Current, External Transistor Application

OUT-to-GND current through the LDO is 40µA (typ). The regulator output can be held up with an external super capacitor or backup battery at OUT until the IN battery is replaced. The RESET output is asserted while the IN battery is removed to place the system in a low-power mode. Volatile memory content is maintained until the super capacitor or battery voltage drops below RAM standby specifications. RESET deasserts when the IN battery has been replaced and OUT exceeds the desired reset threshold. For nonrechargeable backup battery applications, place a reverse diode between OUT and the backup battery (to prevent battery charging). The external diode does not affect the regulator's dropout voltage because it is not between the LDO output and the processor/memory VCC supply. The diode can be replaced with a current-limiting resistor for rechargeable backup battery applications.

Current Limit

The MAX6469-MAX6484 include an internal current-limit circuit that monitors and controls the pass transistor's gate voltage, limiting the output current to 450mA (min). The output can be shorted to ground indefinitely without damaging the part.

Thermal Shutdown

When the junction temperature (T_J) exceeds +180°C (typ), the thermal sensor signals the shutdown logic, turning off the pass transistor and allowing the IC to

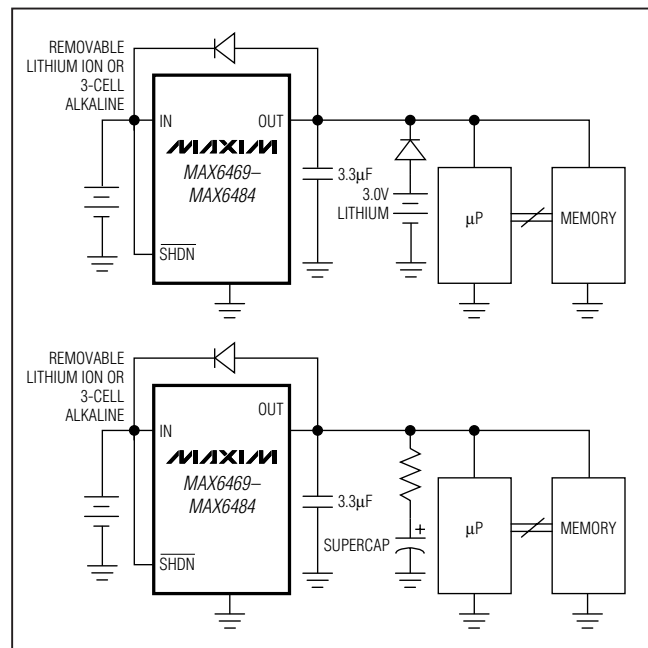


Figure 3. Battery Backup

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cool. The thermal sensor turns the pass transistor on again after the IC's junction temperature cools by 20°C, resulting in a pulsed output during continuous thermal overload conditions. Thermal overload protection is designed to protect the MAX6469–MAX6484 in the event of fault conditions. For continuous operation, do not exceed the absolute maximum junction temperature rating of $T_{JMAX} = +150^{\circ}\text{C}$.

Operating Region and Power Dissipation

The MAX6469–MAX6484's maximum power dissipation depends on the thermal resistance of the case and circuit board, the temperature difference between the die junction and the ambient air, and the rate of airflow. The power dissipation across the device is:

$$P = I_{OUT} (V_{IN} - V_{OUT})$$

The maximum power dissipation is:

$$P_{MAX} = (T_J - T_A) / (\theta_{JB} + \theta_{BA})$$

where $T_J - T_A$ is the temperature difference between the die junction and the surrounding air, θ_{JB} (or θ_{JC}) is the thermal resistance of the package, and θ_{BA} is the thermal resistance through the PC board, copper traces, and other materials to the surrounding air. The MAX6469–MAX6476 TDFN package $\theta_{JC} = 41^{\circ}\text{C}/\text{W}$, and the MAX6469–MAX6476 SOT package $\theta_{JC} = 110^{\circ}\text{C}/\text{W}$.

The MAX6469–MAX6484's ground pin (GND) performs the dual function of providing an electrical connection to the system ground and channeling heat away. Connect GND to the system ground using a large pad or ground plane. For continuous operation, do not exceed the absolute maximum junction temperature rating of $T_{JMAX} = +150^{\circ}\text{C}$.

Applications Information

Output Voltage Selection

The MAX6469–MAX6484 feature dual-mode operation: they operate in either a preset output voltage mode or an adjustable mode. In preset voltage mode, internal feedback resistors set the MAX6469–MAX6484's output from +1.5V to +3.3V (Table 1). Select this mode by connecting SET to ground (MAX6469–MAX6472/MAX6477–MAX6480). In adjustable mode, select an output between 1.25V and 5.5V using two external resistors connected as a voltage-divider to SET (Figure 1). The output voltage is set by the following equation:

$$V_{OUT} = V_{SET} (1 + R_1 / R_2)$$

where $V_{SET} = 1.23\text{V}$. To simplify resistor selection:

$$R_1 = R_2 (V_{OUT} / V_{SET} - 1)$$

Choose $R_2 = 50\text{k}\Omega$ to maintain stability, accuracy and high-frequency power-supply rejection. Avoid selecting resistor values greater than 100kΩ. In preset voltage mode, the impedance between SET and ground should always be less than 50kΩ. In most applications, connect SET directly to ground.

Low-Noise UCSP Output

MAX6477–MAX6484 UCSP products include internal filtering to yield low output noise without an additional external bypass capacitor. The devices yield 75μV_{RMS} (typ) output noise (for $V_{OUT} = 3.0\text{V}$) and 150μV_{RMS} (for $V_{OUT} = 3.3\text{V}$). This low-noise feature makes the MAX6477–MAX6484 ideal for audio applications.

Capacitor Selection and Regulator Stability

For stable operation over the full temperature range and with load currents up to 300mA, use a 3.3μF (min) ceramic output capacitor with an ESR <0.2Ω. To reduce noise and improve load transient response, stability, and power-supply rejection, use large output capacitor values such as 10μF.

Note that some ceramic capacitors exhibit large capacitance and ESR variation with temperature. With capacitor dielectrics such as Z5U and Y5V, use 4.7μF or more to ensure stability over temperature. With X7R or X5R capacitor dielectrics, 3.3μF should be sufficient at all operating temperatures. Higher ESR capacitors require more capacitance to maintain stability. A graph of the Region of Stable ESR vs. Load Current is shown in the *Typical Operating Characteristics*.

To improve power-supply rejection and transient response, use a 1μF capacitor between IN and GND.

The MAX6469–MAX6484 remain stable with purely resistive loads or current loads up to 300mA.

Reset Transient Immunity

The reset circuit is relatively immune to short-duration, falling V_{OUT} transients. The *Typical Operating Characteristics* section shows a graph of the Maximum Transient Duration vs. Reset Threshold Overdrive for which reset is not asserted. The graph was produced using falling V_{OUT} transients starting at V_{OUT} and ending below the reset threshold by the magnitude indicated (reset threshold overdrive). The graph shows the maximum pulse width that a falling V_{OUT} transient can typically have without triggering a reset pulse. As the amplitude of the transient increases (i.e., goes further below the reset threshold), the maximum allowable pulse width decreases. Typically, a V_{OUT} transient that goes only 10mV below the reset threshold and lasts for 75μs does not trigger a reset pulse.

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Power Dissipation Consideration

For the SOT23 package, any pin except the SET pin can be used as a heatsink. If the SET pin is used as a heatsink, excessive parasitic capacitance can affect stability. For the TDFN package, the exposed metal pad on the back side of a package connects to GND of the chip. This metal pad can be used as a heatsink.

UCSP Consideration

For general UCSP package information and PC layout considerations, refer to Maxim Application Note: *Wafer-Level Chip-Scale Package*.

UCSP Reliability

The chip-scale package (UCSP) represents a unique packaging form factor that might not perform equally to a packaged product through traditional mechanical reliability tests. CSP reliability is integrally linked to the user's assembly methods, circuit-board material, and usage environment. The user should closely review these areas when considering a CSP package. Performance through operating life test and moisture resistance remains uncompromised, because it is primarily determined by the wafer-fabrication process.

Mechanical stress performance is a greater consideration for a CSP package. CSPs are attached through direct solder contact to the user's PC board, forgoing the inherent stress relief of a packaged product's lead frame. Solder-joint contact integrity must be considered. Information on Maxim's qualification plan, test data, and recommendations are detailed in the UCSP application note on Maxim's website at www.maxim-ic.com.

Table 1. Output Voltage Suffix Guide

| SUFFIX | OUTPUT VOLTAGE (V) |
|--------|--------------------|
| 15 | 1.5 |
| 16 | 1.6 |
| 17 | 1.7 |
| 18 | 1.8 |
| 19 | 1.9 |
| 20 | 2.0 |
| 21 | 2.1 |
| 22 | 2.2 |
| 23 | 2.3 |
| 24 | 2.4 |
| 25 | 2.5 |
| 26 | 2.6 |
| 27 | 2.7 |
| 28 | 2.8 |
| 285 | 2.85 |
| 29 | 2.9 |
| 30 | 3.0 |
| 31 | 3.1 |
| 32 | 3.2 |
| 33 | 3.3 |

Note: Factory-trimmed custom output voltages may be available; contact factory for availability.

Table 2. Reset Threshold Accuracy Guide

| SUFFIX | V _{OUT} RESET TOLERANCE (%) |
|--------|--------------------------------------|
| A | -7.5 |
| B | -12.5 |

Table 3. Reset Timeout Delay Guide

| SUFFIX | MINIMUM RESET TIMEOUT PERIOD (ms) |
|--------|-----------------------------------|
| D1 | 2.5 |
| D2 | 20 |
| D3 | 150 |
| D4 | 1200 |

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Table 4. Standard Versions

| DEVICE | TOP MARK |
|------------------------|----------|
| MAX6469 TA15BD3 | ADO |
| MAX6469TA18AD3 | ADP |
| MAX6469TA25BD3 | ADQ |
| MAX6469TA28AD3 | ACT |
| MAX6469TA30BD3 | ADR |
| MAX6469TA33AD3 | ADS |
| MAX6470 TA15BD3 | ADT |
| MAX6470TA18AD3 | ADU |
| MAX6470TA25BD3 | ADV |
| MAX6470TA28AD3 | ADW |
| MAX6470TA30BD3 | ADY |
| MAX6470TA33AD3 | ACU |
| MAX6471 TA15AD3 | ADZ |
| MAX6471TA18BD3 | AEA |
| MAX6471TA25AD3 | AEB |
| MAX6471TA28BD3 | AEC |
| MAX6471TA30AD3 | AED |
| MAX6471TA33BD3 | AEE |
| MAX6472 TA15AD3 | AEF |
| MAX6472TA18BD3 | ACW |
| MAX6472TA25AD3 | AEG |
| MAX6472TA28BD3 | AEH |
| MAX6472TA30AD3 | AEI |
| MAX6472TA33BD3 | AEJ |
| MAX6473 TA15AD3 | AEK |
| MAX6473TA18BD3 | AEL |
| MAX6473TA25AD3 | AEM |
| MAX6473TA28BD3 | AEN |
| MAX6473TA30AD3 | AEO |
| MAX6473TA33BD3 | AEP |
| MAX6474 TA15AD3 | AEQ |
| MAX6474TA18BD3 | AER |
| MAX6474TA25AD3 | AES |

| DEVICE | TOP MARK |
|------------------------|----------|
| MAX6474TA28BD3 | AET |
| MAX6474TA30AD3 | AEU |
| MAX6474TA33BD3 | AEV |
| MAX6475 TA15BD3 | AEW |
| MAX6475TA18AD3 | AEX |
| MAX6475TA25BD3 | AEY |
| MAX6475TA28AD3 | AEZ |
| MAX6475TA30BD3 | AFA |
| MAX6475TA33AD3 | ACZ |
| MAX6476 TA15BD3 | AFB |
| MAX6476TA18AD3 | AFC |
| MAX6476TA25BD3 | AFD |
| MAX6476TA28AD3 | AFE |
| MAX6476TA30BD3 | AEF |
| MAX6476TA33AD3 | AFG |
| MAX6477 BL15BD3 | ABW |
| MAX6477BL18AD3 | ABG |
| MAX6477BL25BD3 | ABX |
| MAX6477BL28AD3 | ABY |
| MAX6477BL30BD3 | ABZ |
| MAX6477BL33AD3 | ACA |
| MAX6478 BL15BD3 | ACB |
| MAX6478BL18AD3 | ACC |
| MAX6478BL25BD3 | ACD |
| MAX6478BL28AD3 | ACE |
| MAX6478BL30BD3 | ACF |
| MAX6478BL33AD3 | ACG |
| MAX6479 BL15AD3 | ACH |
| MAX6479BL18BD3 | ACI |
| MAX6479BL25AD3 | ACJ |
| MAX6479BL28BD3 | ACK |
| MAX6479BL30AD3 | ACL |
| MAX6479BL33BD3 | ACM |

MAX6469-MAX6484

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Table 4. Standard Versions (continued)

| DEVICE | TOP MARK |
|------------------------|----------|
| MAX6480 BL15BD3 | ACN |
| MAX6480BL18AD3 | ACO |
| MAX6480BL25BD3 | ACP |
| MAX6480BL28AD3 | ACQ |
| MAX6480BL30BD3 | ACR |
| MAX6480BL33AD3 | ABJ |
| MAX6481 BL15BD3 | ACS |
| MAX6481BL18AD3 | ACT |
| MAX6481BL25BD3 | ACU |
| MAX6481BL28AD3 | ACV |
| MAX6481BL30BD3 | ACW |
| MAX6481BL33AD3 | ACX |
| MAX6482 BL15BD3 | ACY |
| MAX6482BL18AD3 | ACZ |
| MAX6482BL25BD3 | ADA |

| DEVICE | TOP MARK |
|------------------------|----------|
| MAX6482BL28AD3 | ADB |
| MAX6482BL30BD3 | ADC |
| MAX6482BL33AD3 | ADD |
| MAX6483 BL15BD3 | ADE |
| MAX6483BL18AD3 | ADF |
| MAX6483BL25BD3 | ADG |
| MAX6483BL28AD3 | ADH |
| MAX6483BL30BD3 | ADI |
| MAX6483BL33AD3 | ADJ |
| MAX6484 BL15BD3 | ADK |
| MAX6484BL18AD3 | ADL |
| MAX6484BL25BD3 | ADM |
| MAX6484BL28AD3 | ADN |
| MAX6484BL30BD3 | ADO |
| MAX6484BL33AD3 | ADP |

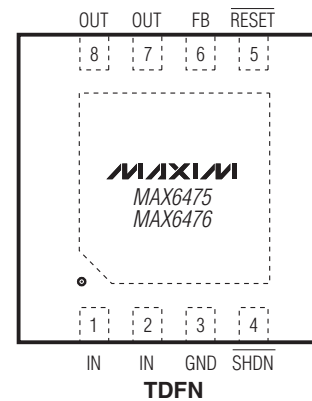
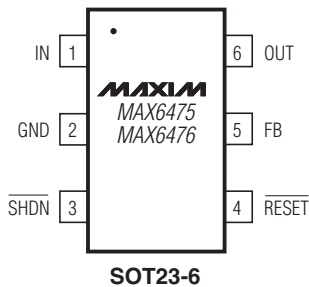
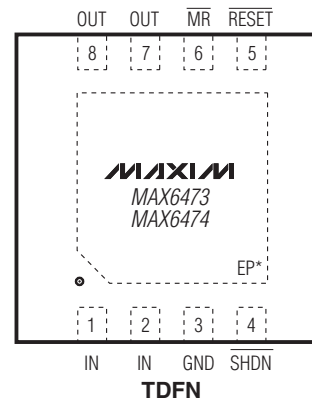
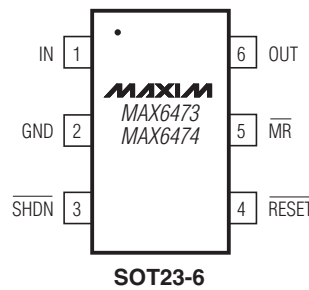
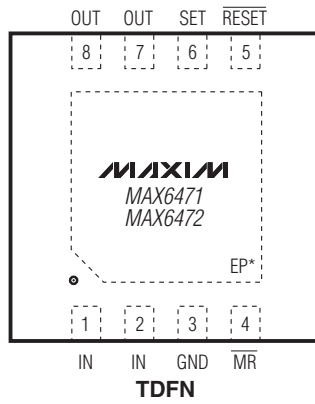
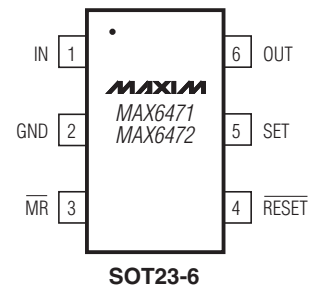
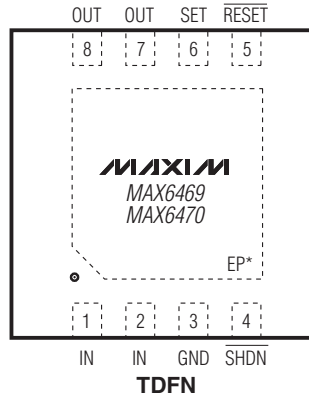
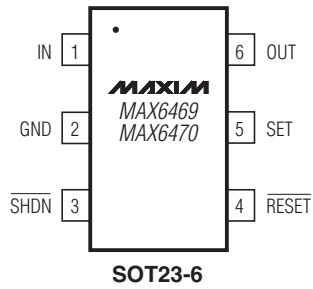
Sample stock is generally available on standard versions only. Standard versions require a minimum order increment of 2.5k units. Nonstandard versions must be ordered in 10k-unit increments. Contact factory for availability.

300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

Pin Configurations

MAX6469-MAX6484

TOP VIEW

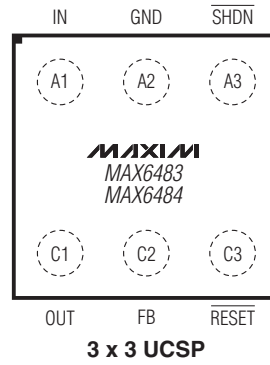
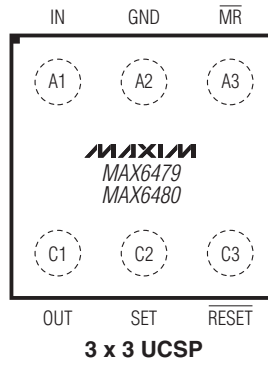
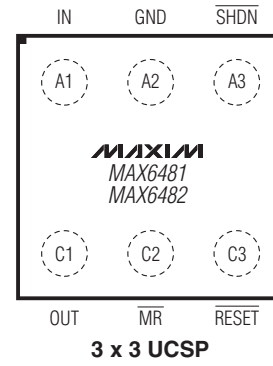
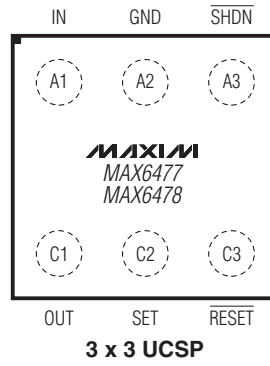


*EP = EXPOSED PAD.

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Pin Configurations (continued)

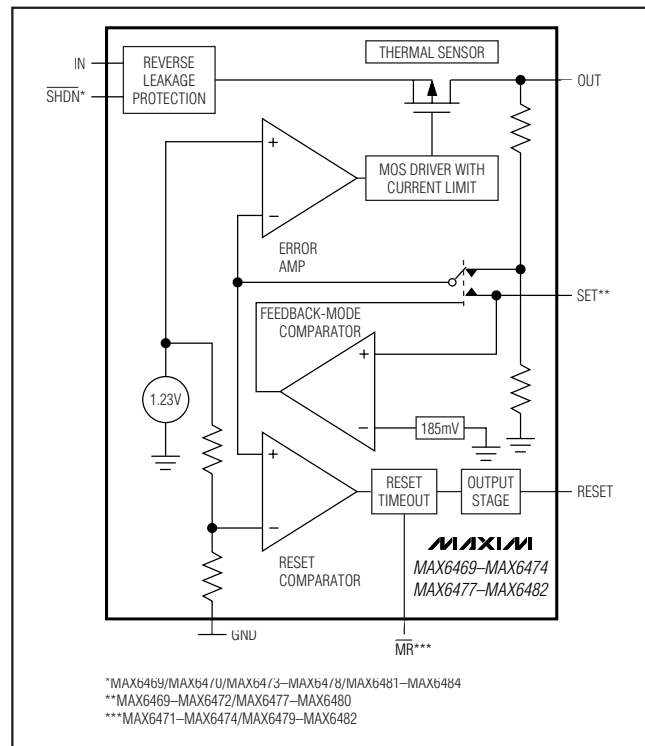
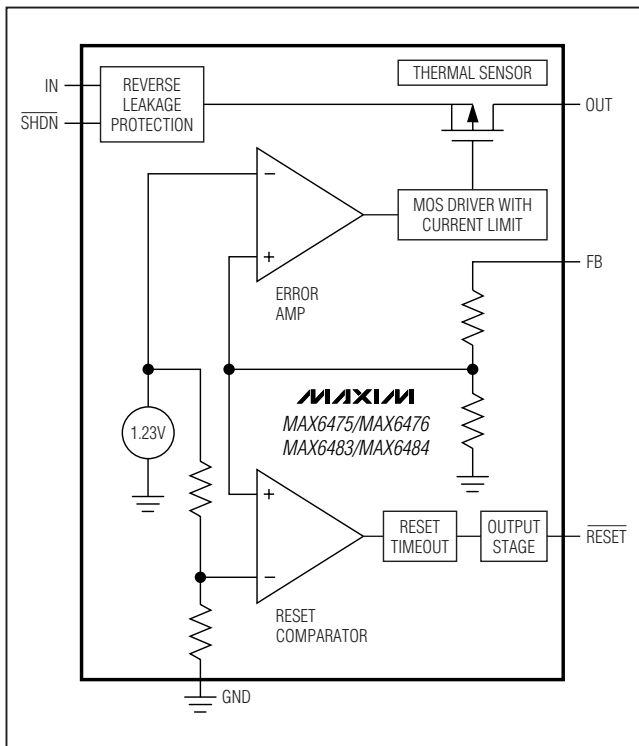
TOP VIEW



UCSP DEVICES SHOWN AS
MOUNTED ON PC BOARD.
BALL SOLDERED DOWN.

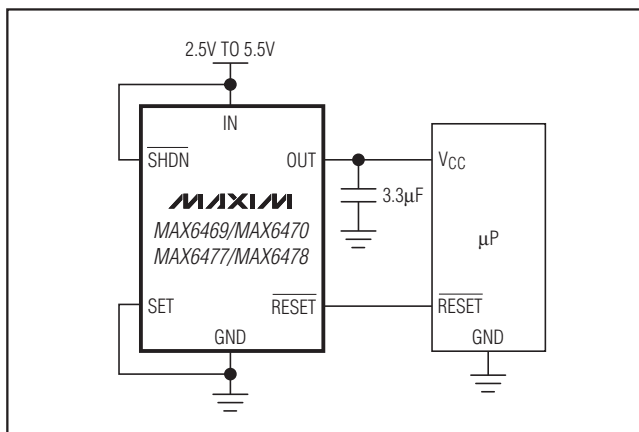
300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

Functional Diagrams



MAX6469-MAX6484

Typical Operating Circuit



Chip Information

PROCESS: BiCMOS

300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

Ordering Information (continued)

| PART* | TEMP RANGE | PIN-PACKAGE |
|-------------------|----------------|--------------|
| MAX6471UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6471TA__D_-T** | -40°C to +85°C | 8 TDFN-EP*** |
| MAX6472UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6472TA__D_-T** | -40°C to +85°C | 8 TDFN-EP*** |
| MAX6473UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6473TA__D_-T** | -40°C to +85°C | 8 TDFN-EP*** |
| MAX6474UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6474TA__D_-T** | -40°C to +85°C | 8 TDFN-EP*** |
| MAX6475UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6475TA__D_-T** | -40°C to +85°C | 8 TDFN-EP*** |

| PART* | TEMP RANGE | PIN-PACKAGE |
|-------------------|----------------|--------------|
| MAX6476UT__D_-T | -40°C to +85°C | 6 SOT23-6 |
| MAX6476TA__D_-T** | -40°C to +85°C | 8 TDFN-EP*** |
| MAX6477BL__D_-T | -40°C to +85°C | 6 UCSP-6 |
| MAX6478BL__D_-T | -40°C to +85°C | 6 UCSP-6 |
| MAX6479BL__D_-T | -40°C to +85°C | 6 UCSP-6 |
| MAX6480BL__D_-T | -40°C to +85°C | 6 UCSP-6 |
| MAX6481BL__D_-T | -40°C to +85°C | 6 UCSP-6 |
| MAX6482BL__D_-T | -40°C to +85°C | 6 UCSP-6 |
| MAX6483BL__D_-T | -40°C to +85°C | 6 UCSP-6 |
| MAX6484BL__D_-T | -40°C to +85°C | 6 UCSP-6 |

*Devices are also available in a lead(Pb)-free/RoHS-compliant packages. Specify lead(Pb)-free by substituting a +T instead of a -T when ordering.

**Future product—contact factory for availability.

***EP = Exposed pad.

Note: The first “_” are placeholders for the output voltage levels of the devices. Desired output voltages are set by the suffix found in the Output Voltage Suffix Guide (Table 1). The third “_” is a placeholder for the reset threshold accuracy. Desired reset threshold accuracy is set by the suffix found in the Reset Threshold Accuracy Guide (Table 2). The “_” following the D is a placeholder for the reset timeout delay time. Desired reset timeout delay time is set by the suffix found in the Reset Timeout Delay Guide (Table 3). For example, the MAX6481BL30BD4-T has a 3.0V output voltage, 12.5% reset threshold tolerance, and a 1200ms (min) reset timeout delay. Sample stock is generally available on standard versions only (Table 4). Standard versions require a minimum order increment of 2.5k units. Nonstandard versions must be ordered in 10k-unit increments. Contact factory for availability.

Selector Guide

| PART | SET | SHDN | MR | FB | PUSH-PULL RESET | OPEN-DRAIN RESET | PACKAGE |
|---------|-----|------|----|----|--------------------|---------------------|-----------------|
| MAX6469 | √ | √ | — | — | √ | — | SOT23-6/8-TDFN |
| MAX6470 | √ | √ | — | — | — | √ | SOT23-6/8-TDFN |
| MAX6471 | √ | — | √ | — | √ | — | SOT23-6/8-TDFN |
| MAX6472 | √ | — | √ | — | — | √ | SOT23-6/8-TDFN |
| MAX6473 | — | √ | √ | — | √ | — | SOT23-6/8-TDFN |
| MAX6474 | — | √ | √ | — | — | √ | SOT23-6/8-TDFN |
| MAX6475 | — | √ | — | √ | √ | — | SOT23-6/8-TDFN |
| MAX6476 | — | √ | — | √ | — | √ | SOT23-6/8-TDFN |
| MAX6477 | √ | √ | — | — | √ | — | 3 x 3 UCSP B9-3 |
| MAX6478 | √ | √ | — | — | — | √ | 3 x 3 UCSP B9-3 |
| MAX6479 | √ | — | √ | — | √ | — | 3 x 3 UCSP B9-3 |
| MAX6480 | √ | — | √ | — | — | √ | 3 x 3 UCSP B9-3 |
| MAX6481 | — | √ | √ | — | √ | — | 3 x 3 UCSP B9-3 |
| MAX6482 | — | √ | √ | — | — | √ | 3 x 3 UCSP B9-3 |
| MAX6483 | — | √ | — | √ | √ | — | 3 x 3 UCSP B9-3 |
| MAX6484 | — | √ | — | √ | — | √ | 3 x 3 UCSP B9-3 |

300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

Package Information

For the latest package outline information and land patterns (footprints), go to www.maxim-ic.com/packages. Note that a "+", "#", or "-" in the package code indicates RoHS status only. Package drawings may show a different suffix character, but the drawing pertains to the package regardless of RoHS status.

| PACKAGE TYPE | PACKAGE CODE | OUTLINE NO. | LAND PATTERN NO. |
|--------------|--------------|-------------------------|-------------------------|
| 6 SOT23-6 | U6F-6 | 21-0058 | 90-0175 |
| 8 TDFN-EP | T833-2 | 21-0137 | 90-0059 |
| 6 UCSP | B9-3 | 21-0093 | — |

MAX6469-MAX6484

300mA LDO Linear Regulators with Internal Microprocessor Reset Circuit

Revision History



| REVISION NUMBER | REVISION DATE | DESCRIPTION | PAGES CHANGED |
|-----------------|---------------|--|---------------|
| 0 | 07/02 | Initial release | — |
| 4 | 04/05 | Removed SOT23 standard versions from the data sheet | 13, 14 |
| 5 | 12/07 | Updated <i>Typical Operating Characteristics</i> and <i>Pin Descriptions</i> sections | 1, 5, 7, 8 |
| 6 | 2/11 | Added soldering temperatures to the <i>Absolute Maximum Ratings</i> section and corrected <i>MAX6471/MAX6472/MAX6479/MAX6480 Pin Description</i> section | 2, 7 |

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