



**THE DATASHEET OF  
PHD16N03T,118**



# PHD16N03T

TrenchMOS™ standard level FET

Rev. 01 — 18 August 2003

Product data

## 1. Product profile

### 1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHD16N03T in SOT428 (D-PAK).

### 1.2 Features

- Fast Switching
- TrenchMOS™ technology.

### 1.3 Applications

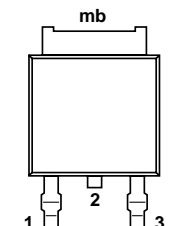
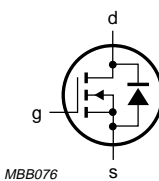
- DC-to-DC converters
- General purpose switch.

### 1.4 Quick reference data

- $V_{DS} \leq 30$  V
- $I_D \leq 13.1$  A
- $P_{tot} \leq 32.6$  W
- $R_{DSon} \leq 100$  m $\Omega$ .

## 2. Pinning information

Table 1: Pinning - SOT428, simplified outline and symbol

Pin	Description	Simplified outline	Symbol
1	gate (g)	 <p>Top view MBK091</p>	 <p>MBB076</p>
2	drain (d) [1]		
3	source (s)		
mb	mounting base; connected to drain (d)		

**SOT428 (D-PAK)**

[1] It is not possible to make connection to pin 2 of the SOT428 package.



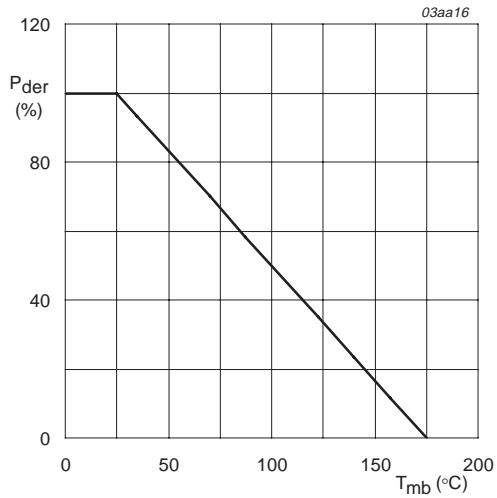
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### 3. Limiting values

**Table 2: Limiting values**

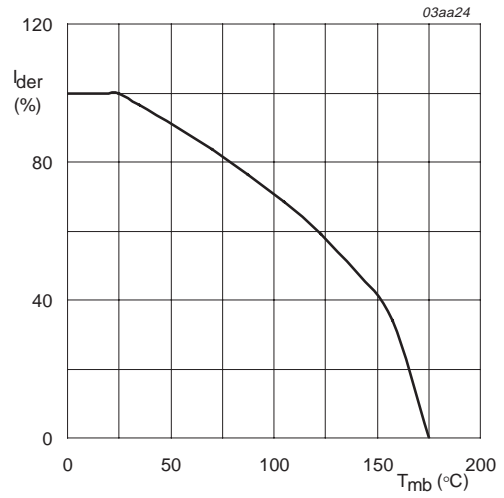
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
$V_{DS}$	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$	-	30	V
$V_{DGR}$	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 175\text{ °C}$ ; $R_{GS} = 20\text{ k}\Omega$	-	30	V
$V_{GS}$	gate-source voltage (DC)		-	$\pm 20$	V
$V_{GSM}$	peak gate-source voltage	$t_p \leq 50\text{ }\mu\text{s}$ ; pulsed; duty cycle = 25%	-	$\pm 30$	V
$I_D$	drain current (DC)	$T_{mb} = 25\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2 and 3</b>	-	13.1	A
		$T_{mb} = 100\text{ °C}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 2</b>	-	9.2	A
$I_{DM}$	peak drain current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$ ; <b>Figure 3</b>	-	52.4	A
$P_{tot}$	total power dissipation	$T_{mb} = 25\text{ °C}$ ; <b>Figure 1</b>	-	32.6	W
$T_{stg}$	storage temperature		-55	+175	°C
$T_j$	junction temperature		-55	+175	°C
<b>Source-drain diode</b>					
$I_S$	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	13.1	A
$I_{SM}$	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$ ; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	52.4	A



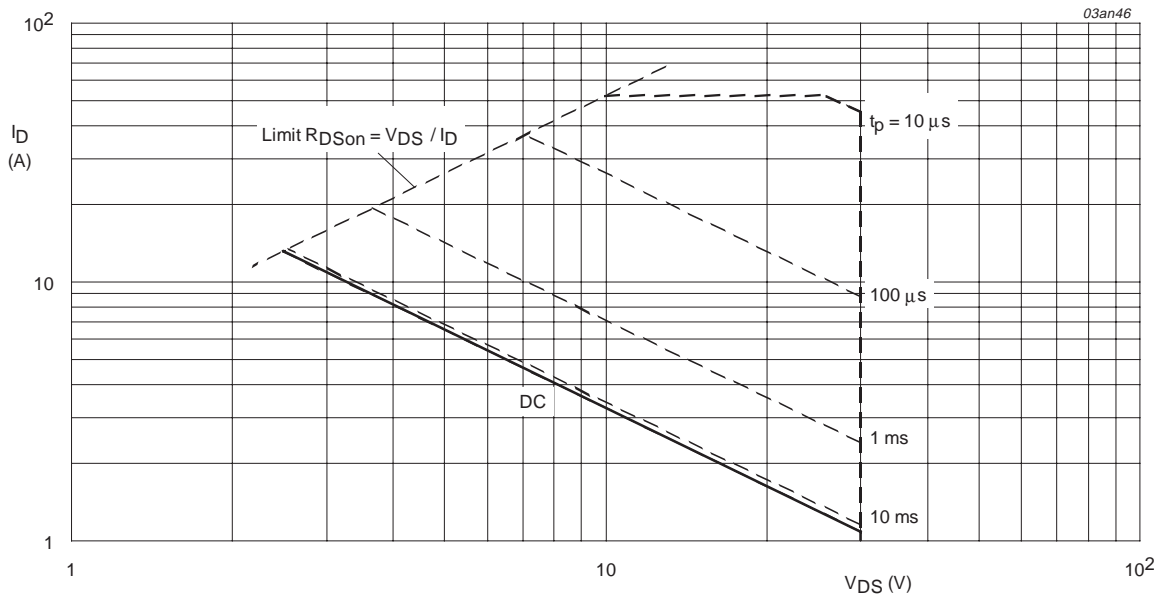
$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

Fig 1. Normalized total power dissipation as a function of mounting base temperature.



$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T<sub>mb</sub> = 25 °C; I<sub>DM</sub> is single pulse; V<sub>GS</sub> = 10 V.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

### 4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	4.6	K/W
$R_{th(j-a)}$	thermal resistance from junction to ambient	SOT428 minimum footprint; vertical in still air; mounted on a PCB	-	75	-	K/W
		SOT404 minimum footprint; vertical in still air; mounted on a PCB	-	50	-	K/W

#### 4.1 Transient thermal impedance

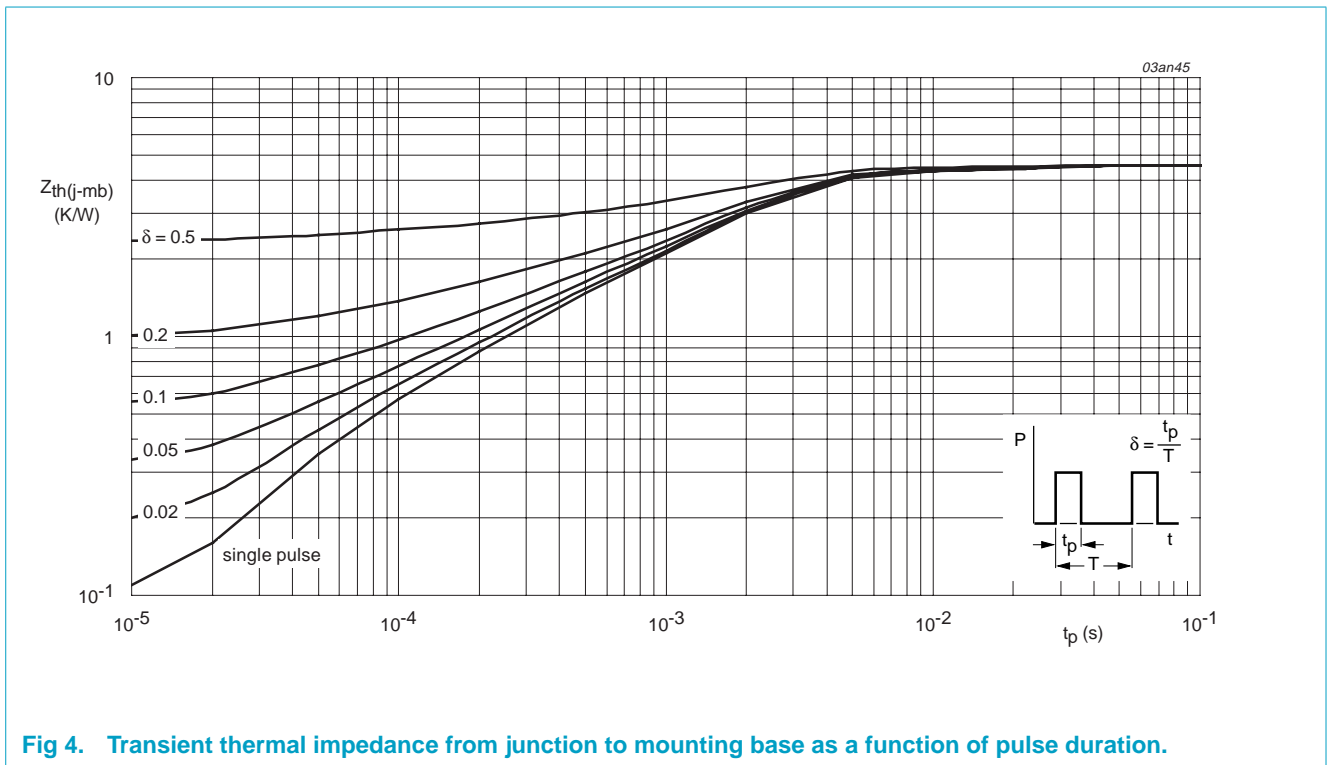


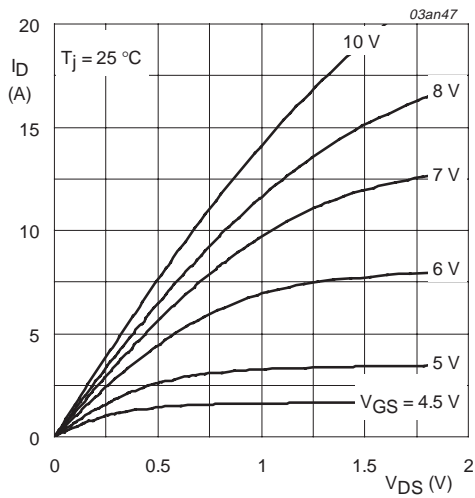
Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

## 5. Characteristics

**Table 4: Characteristics**

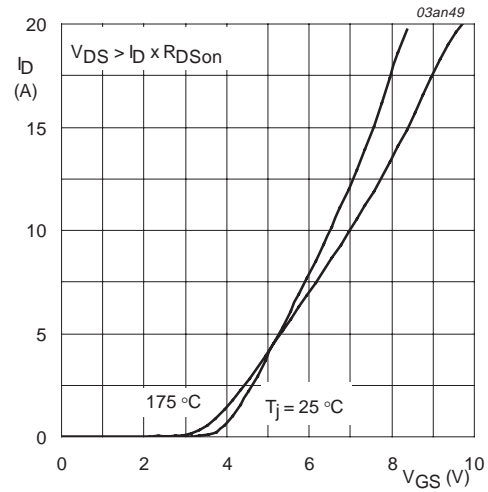
$T_j = 25\text{ °C}$  unless otherwise specified.

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250\text{ }\mu\text{A}$ ; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ °C}$	30	-	-	V
		$T_j = -55\text{ °C}$	27	-	-	V
$V_{GS(th)}$	gate-source threshold voltage	$I_D = 1\text{ mA}$ ; $V_{DS} = V_{GS}$ ; <b>Figure 9</b>				V
		$T_j = 25\text{ °C}$	2	3	4	V
		$T_j = 175\text{ °C}$	1	-	-	V
		$T_j = -55\text{ °C}$	-	-	4.4	V
$I_{DSS}$	drain-source leakage current	$V_{DS} = 30\text{ V}$ ; $V_{GS} = 0\text{ V}$ $T_j = 25\text{ °C}$	-	0.05	10	$\mu\text{A}$
		$T_j = 175\text{ °C}$	-	-	500	$\mu\text{A}$
$I_{GSS}$	gate-source leakage current	$V_{GS} = \pm 20\text{ V}$ ; $V_{DS} = 0\text{ V}$	-	10	100	nA
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}$ ; $I_D = 13\text{ A}$ ; <b>Figure 7 and 8</b> $T_j = 25\text{ °C}$	-	72	100	m $\Omega$
		$T_j = 175\text{ °C}$	-	137	190	m $\Omega$
<b>Dynamic characteristics</b>						
$Q_{g(tot)}$	total gate charge	$I_D = 15\text{ A}$ ; $V_{DD} = 15\text{ V}$ ; $V_{GS} = 10\text{ V}$ ; <b>Figure 13</b>	-	5.2	-	nC
$Q_{gs}$	gate-source charge		-	2.6	-	nC
$Q_{gd}$	gate-drain (Miller) charge		-	1.2	-	nC
$C_{iss}$	input capacitance	$V_{GS} = 0\text{ V}$ ; $V_{DS} = 30\text{ V}$ ; $f = 1\text{ MHz}$ ; <b>Figure 11</b>	-	180	-	pF
$C_{oss}$	output capacitance		-	85	-	pF
$C_{rss}$	reverse transfer capacitance		-	60	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DD} = 15\text{ V}$ ; $R_L = 0.6\text{ }\Omega$ ;	-	6	-	ns
$t_r$	rise time	$V_{GS} = 10\text{ V}$ ; $R_G = 56\text{ }\Omega$	-	45	-	ns
$t_{d(off)}$	turn-off delay time		-	12	-	ns
$t_f$	fall time		-	23	-	ns
<b>Source-drain diode</b>						
$V_{SD}$	source-drain (diode forward) voltage	$I_S = 10\text{ A}$ ; $V_{GS} = 0\text{ V}$ ; <b>Figure 12</b>	-	1	1.2	V



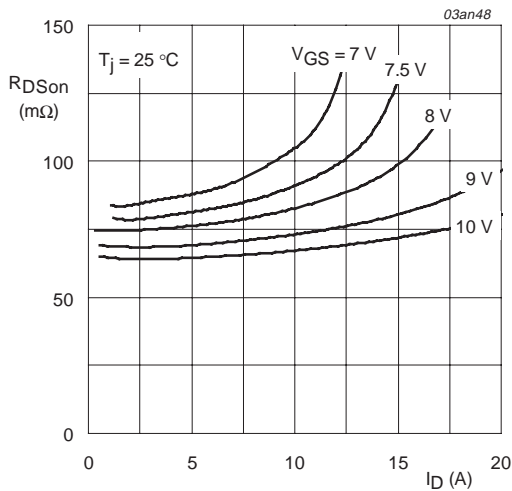
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



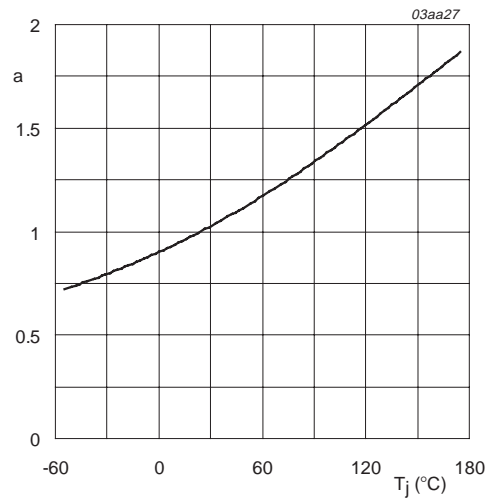
$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



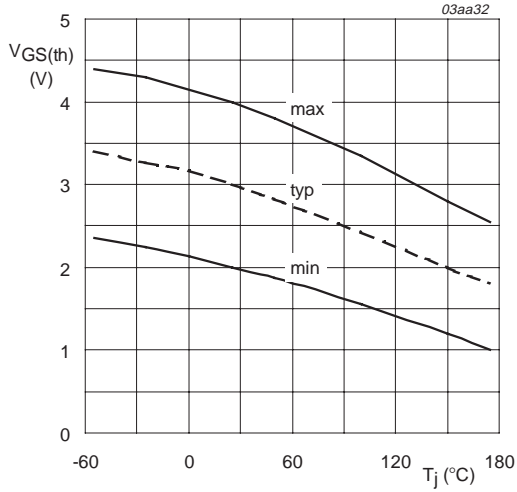
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



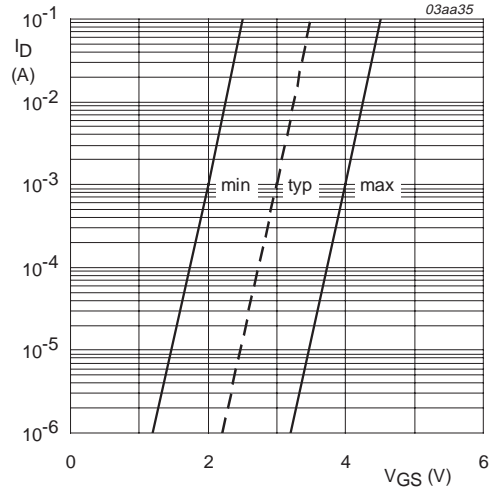
$$a = \frac{R_{DSon}}{R_{DSon}(25^\circ\text{C})}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



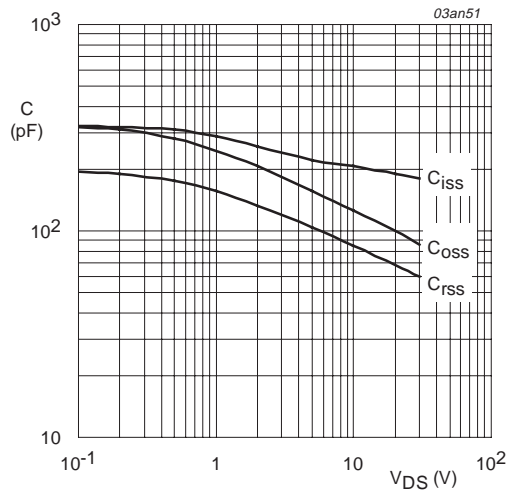
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



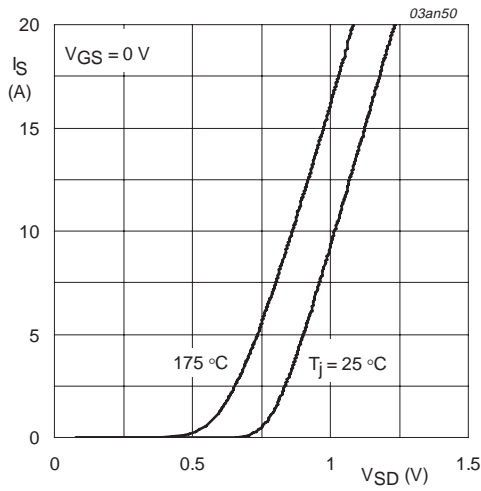
$T_J = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



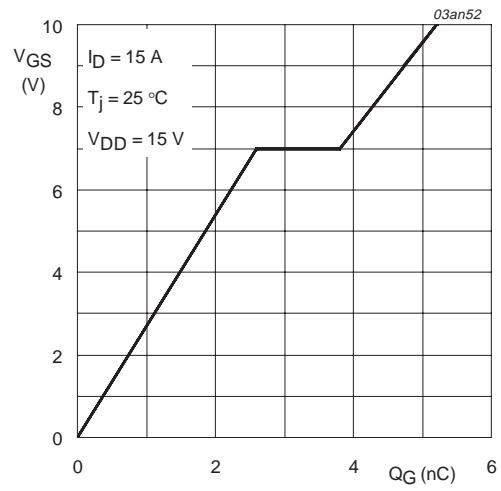
$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 11. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$T_j = 25\text{ }^\circ\text{C}$  and  $175\text{ }^\circ\text{C}$ ;  $V_{GS} = 0\text{ V}$

**Fig 12. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.**



$I_D = 15\text{ A}$ ;  $V_{DD} = 15\text{ V}$

**Fig 13. Gate-source voltage as a function of gate charge; typical values.**

6. Package outline

Plastic single-ended surface mounted package (Philips version of D-PAK); 3 leads (one lead cropped)

SOT428

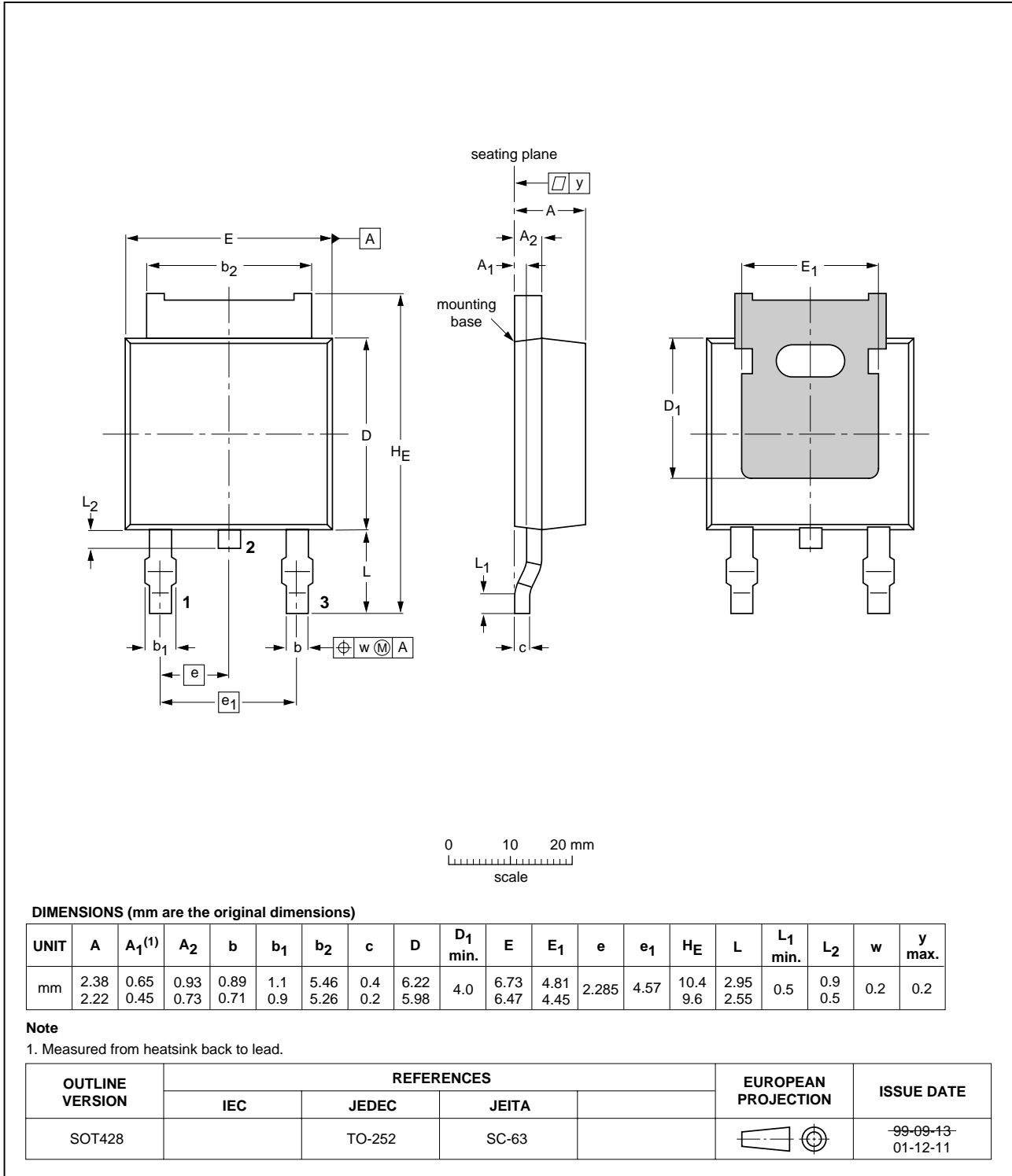


Fig 14. SOT428.

## 7. Revision history

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Table 5: Revision history

Rev	Date	CPCN	Description
01	20030818	-	Product data; initial version (9397 750 11672)

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## 8. Data sheet status

Level	Data sheet status <sup>[1]</sup>	Product status <sup>[2][3]</sup>	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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[3] For data sheets describing multiple type numbers, the highest-level product status determines the data sheet status.

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**Limiting values definition** — Limiting values given are in accordance with the Absolute Maximum Rating System (IEC 60134). Stress above one or more of the limiting values may cause permanent damage to the device. These are stress ratings only and operation of the device at these or at any other conditions above those given in the Characteristics sections of the specification is not implied. Exposure to limiting values for extended periods may affect device reliability.

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