

TRS3243 3-V to 5.5-V Multichannel RS-232 Line Driver and Receiver With ± 15 -kV ESD (HBM) Protection

1 Features

- Operates With 3-V to 5.5-V V_{CC} Supply
- Single-Chip and Single-Supply Interface for IBM[®] PC/AT[™] Serial Port
- RS-232 Bus-Pin ESD Protection of ± 15 kV Using Human-Body Model (HBM)
- Meets or Exceeds the Requirements of TIA/EIA-232-F and ITU V.28 Standards
- Three Drivers and Five Receivers
- Operates up to 250 kbps
- Low Active Current: 300- μ A Typical
- Low Standby Current: 1- μ A Typical
- External Capacitors: 4 \times 0.1 μ F
- Accepts 5-V Logic Input With 3.3-V Supply
- Always-Active Noninverting Receiver Output (ROUT2B)
- Operating Temperature
 - TRS3243C: 0°C to 70°C
 - TRS3243I: –40°C to 85°C
- Serial-Mouse Driveability
- Automatic Power-Down Feature to Disable Driver Outputs When No Valid RS-232 Signal Is Sensed

2 Applications

- Battery-Powered Systems
- Tablets
- Notebooks
- Laptops
- Hand-Held Equipment

3 Description

The TRS3243 device consists of three line drivers, and five line receivers, which is ideal for DE-9 DTE interface. A ± 15 -kV ESD (HBM) protection pin-to-pin (serial-port connection pins, including GND). Flexible power features save power automatically. Special outputs ROUT2B and INVALID are always enabled to allow checking for ring indicator and valid RS232 input.

Device Information⁽¹⁾

PART NUMBER	PACKAGE	BODY SIZE (NOM)
TRS3243	SSOP (28)	10.20 mm \times 5.30 mm
	TSSOP (28)	9.70 mm \times 4.40 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Simplified Schematic

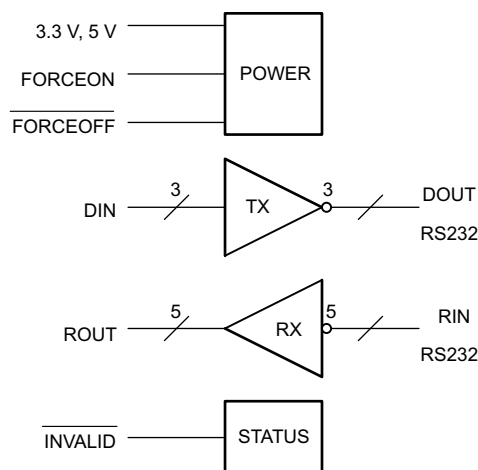


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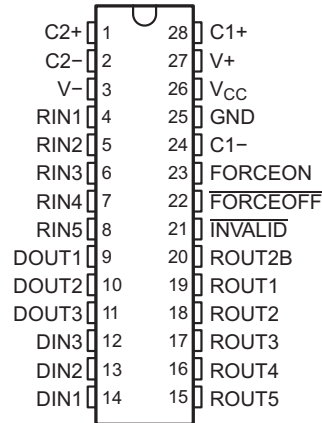
4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision A (September 2011) to Revision B	Page
<ul style="list-style-type: none"> • Added <i>Pin Functions</i> table, <i>ESD Ratings</i> table, <i>Thermal Information</i> table, <i>Typical Characteristics</i> section, <i>Detailed Description</i>, <i>Application and Implementation</i>, <i>Power Supply Recommendations</i>, <i>Layout</i>, <i>Device and Documentation Support</i> and <i>Mechanical, Packaging, and Orderable Information</i> sections 	1
<ul style="list-style-type: none"> • Deleted <i>Ordering Information</i> table 	3

5 Pin Configuration and Functions

DB, PW Packages
28-Pin SSOP, TSSOP
Top View



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
C1+	28	—	Positive lead of C1 capacitor
C1–	24	—	Negative lead on C1 capacitor
C2+	1	—	Positive lead of C2 capacitor
C2–	2	—	Negative lead of C2 capacitor
DIN1	14	I	Logic data input (from UART)
DIN2	13	I	
DIN3	12	I	
DOUT1	9	O	RS232 line data output (to remote RS232 system)
DOUT2	10	O	
DOUT3	11	O	
FORCEOFF	22	I	Low input forces DOUT1-5, ROUT1-5 high Z per Device Functional Modes
FORCEON	23	I	High forces drivers on. Low is automatic mode per Device Functional Modes
GND	25	—	Ground
INVALID	21	O	Active low output when all RIN are unpowered
RIN1	4	I	RS232 line data input (from remote RS232 system)
RIN2	5	I	
RIN3	6	I	
RIN4	7	I	
RIN5	8	I	
ROUT1	19	O	Logic data output (to UART)
ROUT2	18	O	
ROUT2B	20	O	Always Active noninverting output for RIN2 (normally used for ring indicator)
ROUT3	17	O	Logic data output (to UART)
ROUT4	16	O	
ROUT5	15	O	
V+	27	O	Positive charge pump output for storage capacitor only
V–	3	O	Negative charge pump output for storage capacitor only
V _{CC}	26	—	Supply Voltage, Connect to 3-V to 5.5-V power supply

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted) ⁽¹⁾

		MIN	MAX	UNIT	
V _{CC}	Supply voltage ⁽²⁾	-0.3	6	V	
V ₊	Positive output supply voltage ⁽²⁾	-0.3	7	V	
V ₋	Negative output supply voltage ⁽²⁾	0.3	-7	V	
V ₊ - V ₋	Supply voltage difference ⁽²⁾		13	V	
V _I	Input voltage	Driver, $\overline{\text{FORCEOFF}}$, FORCEON	-0.3	6	V
		Receiver	-25	25	
V _O	Output voltage	Driver	-13.2	13.2	V
		Receiver, $\overline{\text{INVALID}}$	-0.3	V _{CC} + 0.3	
T _J	Operating virtual junction temperature		150	°C	
T _{stg}	Storage temperature	-65	150	°C	

- (1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) All voltages are with respect to network GND.

6.2 ESD Ratings

		VALUE	UNIT
V _(ESD)	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 RIN, DOUT, and GND pins ⁽¹⁾	±15000
		Human body model (HBM), per ANSI/ESDA/JEDEC JS-001 All other pins ⁽¹⁾	±3000
		Charged device model (CDM), per JEDEC specification JESD22-C101, all pins ⁽²⁾	±1000

- (1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
- (2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

(see [Figure 8](#))⁽¹⁾

		MIN	NOM	MAX	UNIT	
V _{CC}	Supply voltage	V _{CC} = 3.3 V	3	3.3	3.6	V
		V _{CC} = 5 V	4.5	5	5.5	
V _{IH}	Driver and control high-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	V _{CC} = 3.3 V	2	5.5	V
			V _{CC} = 5 V	2.4	5.5	
V _{IL}	Driver and control low-level input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	0	0.8	V	
V _I	Driver and control input voltage	DIN, $\overline{\text{FORCEOFF}}$, FORCEON	0	5.5	V	
V _I	Receiver input voltage		-25	25	V	
T _A	Operating free-air temperature	TRS3243C	0	70	°C	
		TRS3243I	-40	85		

- (1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

6.4 Thermal Information

THERMAL METRIC ⁽¹⁾	TRS3243		UNIT	
	DB (SSOP)	PW (TSSOP)		
	16 PINS	16 PINS		
R _{θJA}	Junction-to-ambient thermal resistance	62	62	°C/W

- (1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report ([SPRA953](#)).

6.5 Electrical Characteristics—Power and Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see Figure 8)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
I _{CC}	Supply current Automatic power down disabled	No load, $\overline{\text{FORCEOFF}}$ and FORCEON at V _{CC} . T _A = 25°C		0.3	1	mA
	Supply current Powered off	No load, $\overline{\text{FORCEOFF}}$ at GND. T _A = 25°C		1	10	μA
	Supply current Automatic power down enabled	No load, $\overline{\text{FORCEOFF}}$ at V _{CC} , FORCEON at GND, All RIN are open or grounded, All DIN are grounded. T _A = 25°C		1	10	
I _I	Input leakage current of $\overline{\text{FORCEOFF}}$, FORCEON	V _I = V _{CC} or V _I at GND		±0.01	±1	μA
V _{IT+}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V _{CC}			2.7	V
V _{IT-}	Receiver input threshold for INVALID high-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V _{CC}	-2.7			V
V _T	Receiver input threshold for INVALID low-level output voltage	FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V _{CC}	-0.3		0.3	V
V _{OH}	$\overline{\text{INVALID}}$ high-level output voltage	I _{OH} = -1 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V _{CC}	V _{CC} - 0.6			V
V _{OL}	$\overline{\text{INVALID}}$ low-level output voltage	I _{OL} = 1.6 mA, FORCEON = GND, $\overline{\text{FORCEOFF}}$ = V _{CC}			0.4	V

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.6 Electrical Characteristics—Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see Figure 8)

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	All DOUT at R _L = 3 kΩ to GND	5	5.4		V
V _{OL}	Low-level output voltage	All DOUT at R _L = 3 kΩ to GND	-5	-5.4		V
V _O	Output voltage (mouse driveability)	DIN1 = DIN2 = GND, DIN3 = V _{CC} , 3 kΩ to GND at DOUT3, DOUT1 = DOUT2 = 2.5 mA		±5		V
I _{IH}	High-level input current	V _I = V _{CC}		±0.01	±1	μA
I _{IL}	Low-level input current	V _I at GND		±0.01	±1	μA
V _{hys}	Input hysteresis				±1	V
I _{OS}	Short-circuit output current ⁽³⁾	V _{CC} = 3.6 V, V _O = 0 V		±35	±60	mA
		V _{CC} = 5.5 V, V _O = 0 V				
r _o	Output resistance	V _{CC} = 0 V, V ₊ = 0 V, and V ₋ = 0 V, V _O = ±2 V	300	10M		Ω
I _{off}	Output leakage current	$\overline{\text{FORCEOFF}}$ = GND,	V _O = ±12 V, V _{CC} = 3 to 3.6 V		±25	μA
			V _O = ±10 V, V _{CC} = 4.5 to 5.5 V		±25	

(1) Test conditions are C1–C4 = 0.1 μF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 μF, C2–C4 = 0.33 μF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Short-circuit durations must be controlled to prevent exceeding the device absolute power dissipation ratings, and not more than one output should be shorted at a time.

6.7 Electrical Characteristics—Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see [Figure 8](#))

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
V _{OH}	High-level output voltage	I _{OH} = -1 mA	V _{CC} - 0.6	V _{CC} - 0.1		V
V _{OL}	Low-level output voltage	I _{OH} = 1.6 mA			0.4	V
V _{IT+}	Positive-going input threshold voltage	V _{CC} = 3.3 V		1.6	2.4	V
		V _{CC} = 5 V		1.9	2.4	
V _{IT-}	Negative-going input threshold voltage	V _{CC} = 3.3 V	0.6	1.1		V
		V _{CC} = 5 V	0.8	1.4		
V _{hys}	Input hysteresis (V _{IT+} - V _{IT-})			0.5		V
I _{off}	Output leakage current (except ROUT2B)	FORCEOFF = 0 V		±0.05	±10	µA
r _i	Input resistance	V _i = ±3 V or ±25 V	3	5	7	kΩ

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.8 Switching Characteristics—Power and Status

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted) (see [Figure 7](#))

PARAMETER		TEST CONDITIONS	TYP ⁽¹⁾	UNIT
t _{valid}	Propagation delay time, low- to high-level output	V _{CC} = 5 V	1	µs
t _{invalid}	Propagation delay time, high- to low-level output	V _{CC} = 5 V	30	µs
t _{en}	Supply enable time	V _{CC} = 5 V	100	µs

(1) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

6.9 Switching Characteristics—Driver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾ (see [Figure 8](#))

TRS3243C, TRS3243I

PARAMETER		TEST CONDITIONS	MIN	TYP ⁽²⁾	MAX	UNIT
	Maximum data rate	R _L = 3 kΩ One DOUT switching, C _L = 1000 pF See Figure 3	150	250		kbps
t _{sk(p)}	Pulse skew ⁽³⁾	R _L = 3 kΩ to 7 kΩ C _L = 150 pF to 2500 pF See Figure 5		100		ns
SR(tr)	Slew rate, transition region (see Figure 3)	V _{CC} = 3.3 V, R _L = 3 kΩ to 7 kΩ	C _L = 150 pF to 1000 pF	6	30	V/µs
			C _L = 150 pF to 2500 pF	4	30	

(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

6.10 Switching Characteristics—Receiver

over recommended ranges of supply voltage and operating free-air temperature (unless otherwise noted)⁽¹⁾

PARAMETER		TEST CONDITIONS	TYP ⁽²⁾	UNIT
t _{PLH}	Propagation delay time, low- to high-level output	C _L = 150 pF, See Figure 5	150	ns
t _{PHL}	Propagation delay time, high- to low-level output		150	ns
t _{en}	Output enable time	C _L = 150 pF, R _L = 3 kΩ, See Figure 6	200	ns
t _{dis}	Output disable time		200	ns
t _{sk(p)}	Pulse skew ⁽³⁾		See Figure 5	50

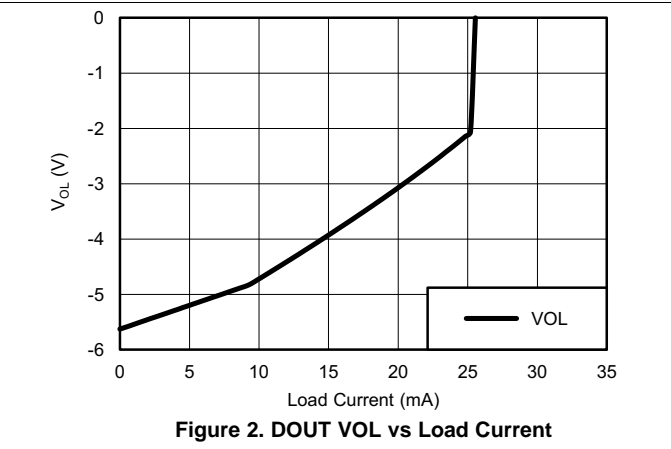
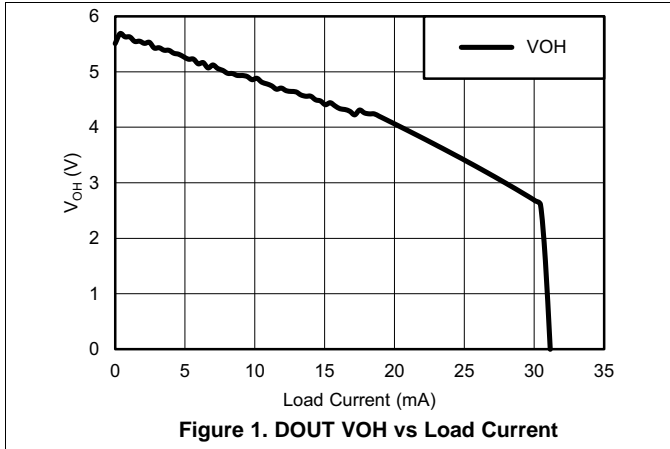
(1) Test conditions are C1–C4 = 0.1 µF at V_{CC} = 3.3 V ± 0.3 V; C1 = 0.047 µF, C2–C4 = 0.33 µF at V_{CC} = 5 V ± 0.5 V.

(2) All typical values are at V_{CC} = 3.3 V or V_{CC} = 5 V, and T_A = 25°C.

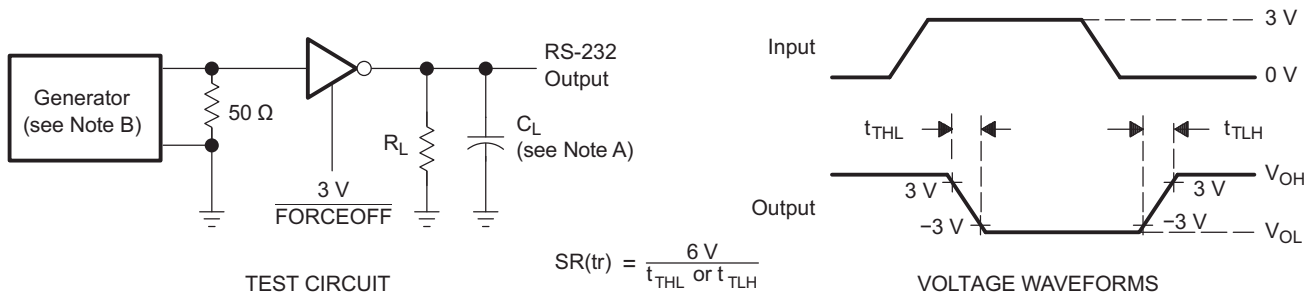
(3) Pulse skew is defined as |t_{PLH} - t_{PHL}| of each channel of the same device.

6.11 Typical Characteristics

$V_{CC} = 3.3\text{ V}$

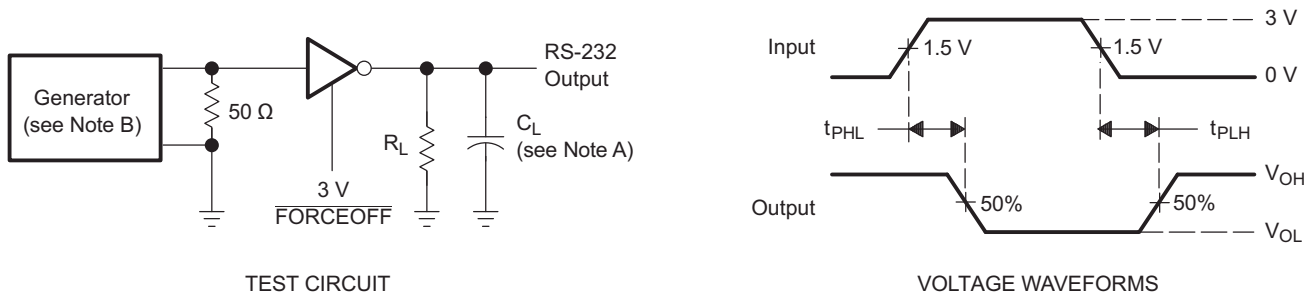


7 Parameter Measurement Information



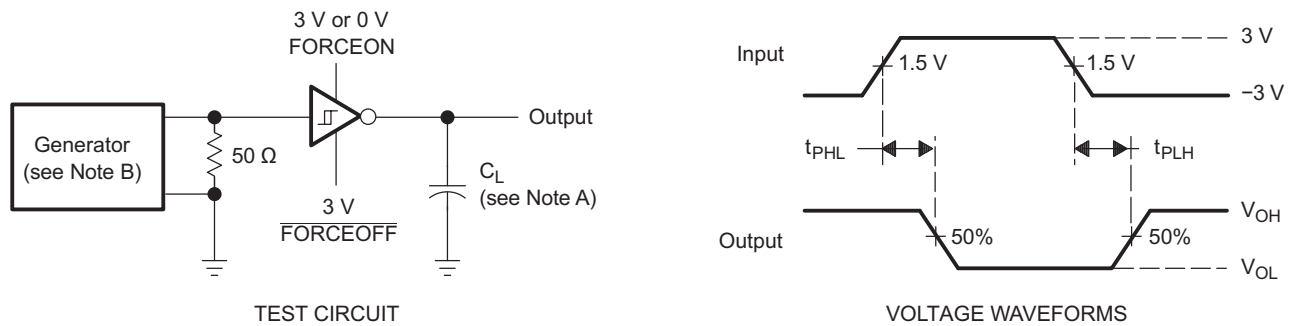
- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbps, (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 3. Driver Slew Rate



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 250 kbps, (MAX3243C/I) and 1 Mbit/s (MAX3243FC/I), $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

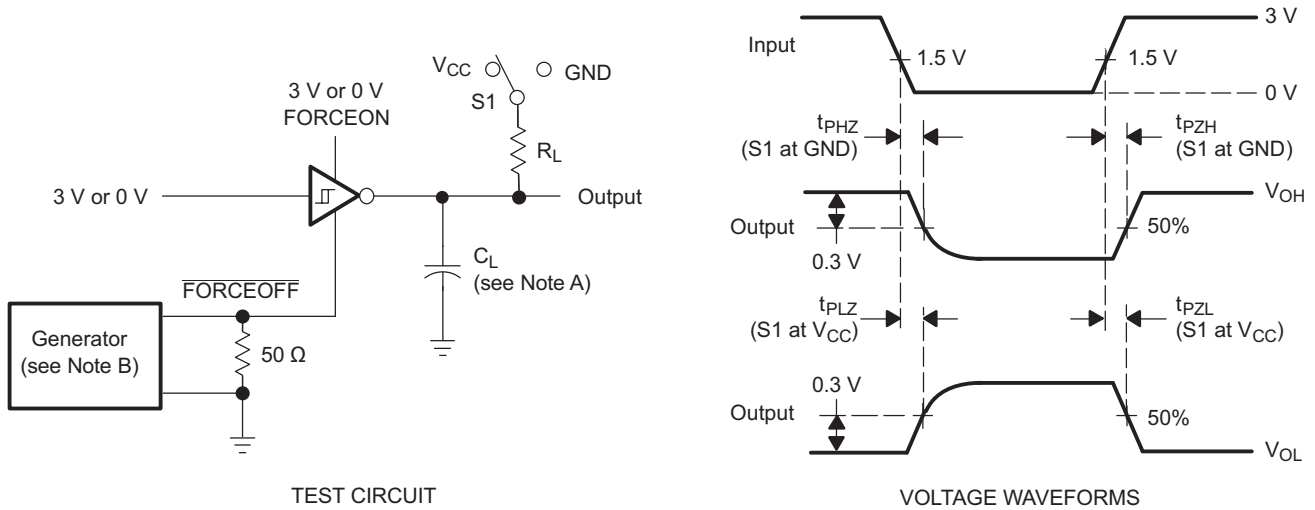
Figure 4. Driver Pulse Skew



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.

Figure 5. Receiver Propagation Delay Times

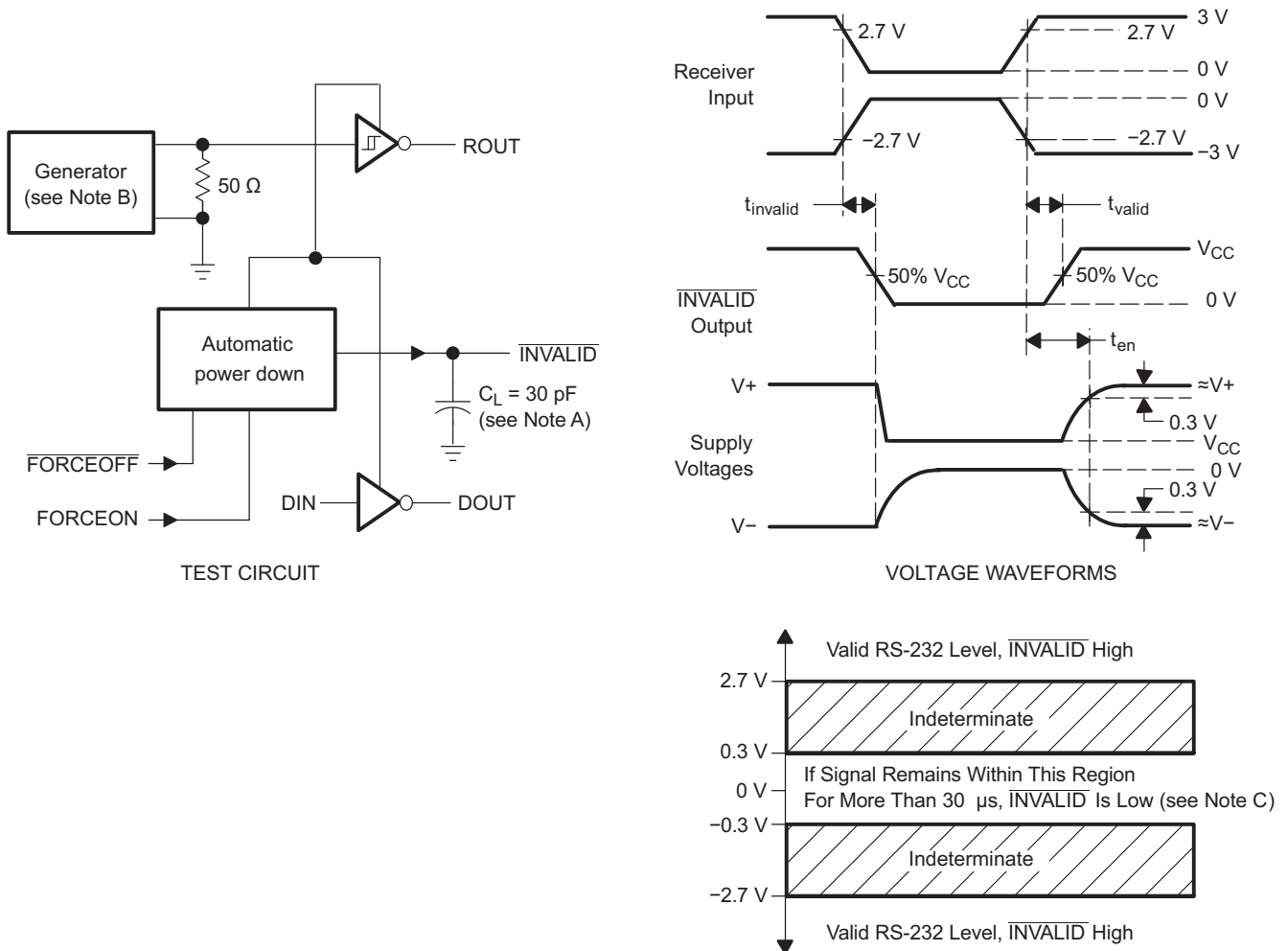
Parameter Measurement Information (continued)



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- C. t_{PLZ} and t_{PHZ} are the same as t_{dis} .
- D. t_{PZL} and t_{PZH} are the same as t_{en} .

Figure 6. Receiver Enable and Disable Times

Parameter Measurement Information (continued)



- A. C_L includes probe and jig capacitance.
- B. The pulse generator has the following characteristics: PRR = 5 kbps, $Z_O = 50 \Omega$, 50% duty cycle, $t_r \leq 10 \text{ ns}$, $t_f \leq 10 \text{ ns}$.
- C. Automatic power down disables drivers and reduces supply current to 1 μA .

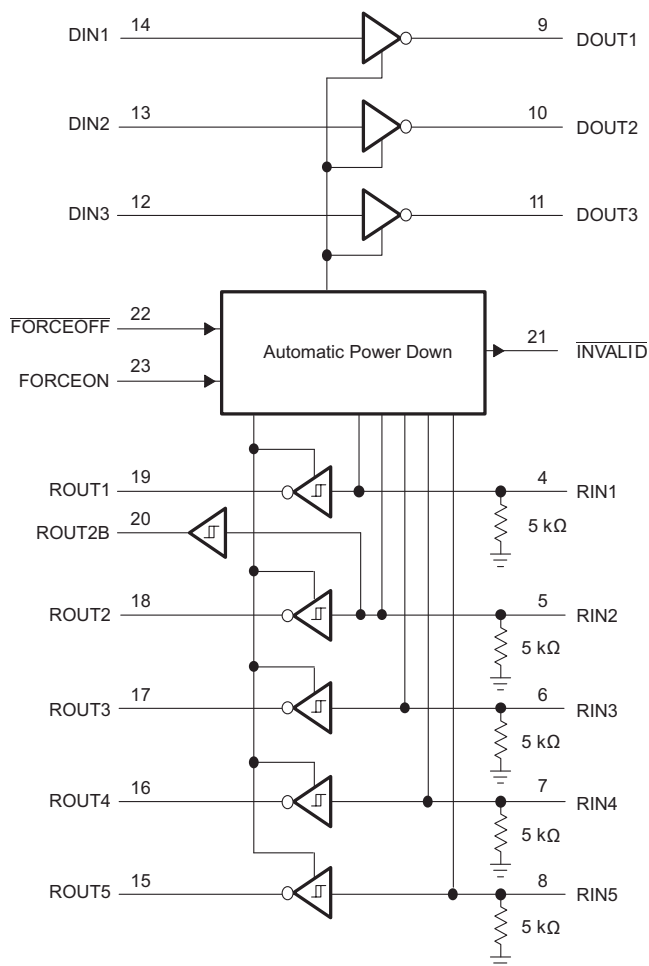
Figure 7. $\overline{\text{INVALID}}$ Propagation Delay Times and Supply Enabling Time

8 Detailed Description

8.1 Overview

The TRS3243 device consists of three line drivers, five line receivers, and a dual charge-pump circuit with ± 15 -kV ESD (HBM) protection pin-to-pin (serial-port connection pins, including GND). The TRS3243 device meets the requirements of TIA/EIA-232-F and provides the electrical interface between an asynchronous communication controller and the serial-port connector. This combination of drivers and receivers matches what is needed for the typical serial port used in an IBM PC, AT, or compatible device. The charge pump and four small external capacitors allow operation from one 3-V to 5.5-V supply. In addition, the device includes an always-active noninverting output (ROUT2B), which allows applications using the ring indicator to transmit data while the device is powered down. Flexible control options for power management are available when the serial port is inactive. The automatic power-down feature functions when FORCEON is low and FORCEOFF is high. During this mode of operation, if the device does not sense a valid RS-232 signal, the driver outputs are disabled. If FORCEOFF is set low, both drivers and receivers (except ROUT2B) are shut off, and the supply current is reduced to 1 μ A. Disconnecting the serial port or turning off the peripheral drivers causes the automatic power-down condition to occur. Automatic power down can be disabled when FORCEON and FORCEOFF are high and must be done when driving a serial mouse. With automatic power down enabled, the device is activated automatically when a valid signal is applied to any receiver input. The INVALID output is used to notify the user if an RS-232 signal is present at any receiver input. INVALID is high (valid data) if any receiver input voltage is greater than 2.7 V, is less than -2.7 V, or has been between -0.3 V and 0.3 V for less than 30 μ s. INVALID is low (invalid data) if all receiver input voltages are between -0.3 V and 0.3 V for more than 30 μ s.

8.2 Functional Block Diagram



8.3 Feature Description

8.3.1 Automatic Power Down

Automatic power down can be used to automatically save power when the receivers are unconnected or when they are connected to a powered down remote RS232 port. FORCEON being high overrides automatic power down and the drivers are active. $\overline{\text{FORCEOFF}}$ being low overrides FORCEON and powers down all outputs except for ROUT2B and $\overline{\text{INVALID}}$.

8.3.2 Charge Pump

The charge pump increases, inverts, and regulates voltage at V+ and V– pins. The charge pump requires four external capacitors.

8.3.3 RS232 Driver

Three drivers interface standard logic level to RS232 levels. All DIN inputs must be valid high or low.

8.3.4 RS232 Receiver

Five receivers interface RS232 levels to standard logic levels. An open input results in a high output on ROUT. Each RIN input includes an internal standard RS232 load.

8.3.5 ROUT2B Receiver

ROUT2B is an always-active, noninverting output of RIN2 input, which allows applications using the ring indicator to transmit data while the device is powered down.

8.3.6 Invalid Input Detection

The $\overline{\text{INVALID}}$ output goes active low when all RIN inputs are unpowered. The $\overline{\text{INVALID}}$ output goes inactive high when any RIN input is connected to an active RS232 voltage level.

8.4 Device Functional Modes

Table 1. Each Driver⁽¹⁾

INPUTS				OUTPUT	DRIVER STATUS
DIN	FORCEON	$\overline{\text{FORCEOFF}}$	VALID RIN RS-232 LEVEL	DOUT	
X	X	L	X	Z	Powered off
L	H	H	X	H	Normal operation with automatic power down disabled
H	H	H	X	L	
L	L	H	YES	H	Normal operation with automatic power down enabled
H	L	H	YES	L	
X	L	H	NO	Z	Power off by automatic power down feature

(1) H = high level, L = low level, X = irrelevant, Z = high impedance, YES = any RIN valid, NO = all RIN invalid

Table 2. Each Receiver⁽¹⁾

INPUTS			OUTPUTS	RECEIVER STATUS
RIN	FORCEON	$\overline{\text{FORCEOFF}}$	ROUT	
X	X	L	Z	Powered off
L	X	H	H	Normal operation
H	X	H	L	
Open	X	H	H	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), Open = input disconnected or connected driver off

Table 3. $\overline{\text{INVALID}}$ and ROUT2B Outputs⁽¹⁾

INPUTS				OUTPUTS		OUTPUT STATUS
VALID RIN RS-232 LEVEL	RIN2	FORCEON	$\overline{\text{FORCEOFF}}$	$\overline{\text{INVALID}}$	ROUT2B	
YES	L	X	X	H	L	Always Active
YES	H	X	X	H	H	
YES	OPEN	X	X	H	L	Always Active
NO	OPEN	X	X	L	L	

(1) H = high level, L = low level, X = irrelevant, Z = high impedance (off), OPEN = input disconnected or connected driver off, YES = any RIN valid, NO = all RIN invalid

9 Application and Implementation

NOTE

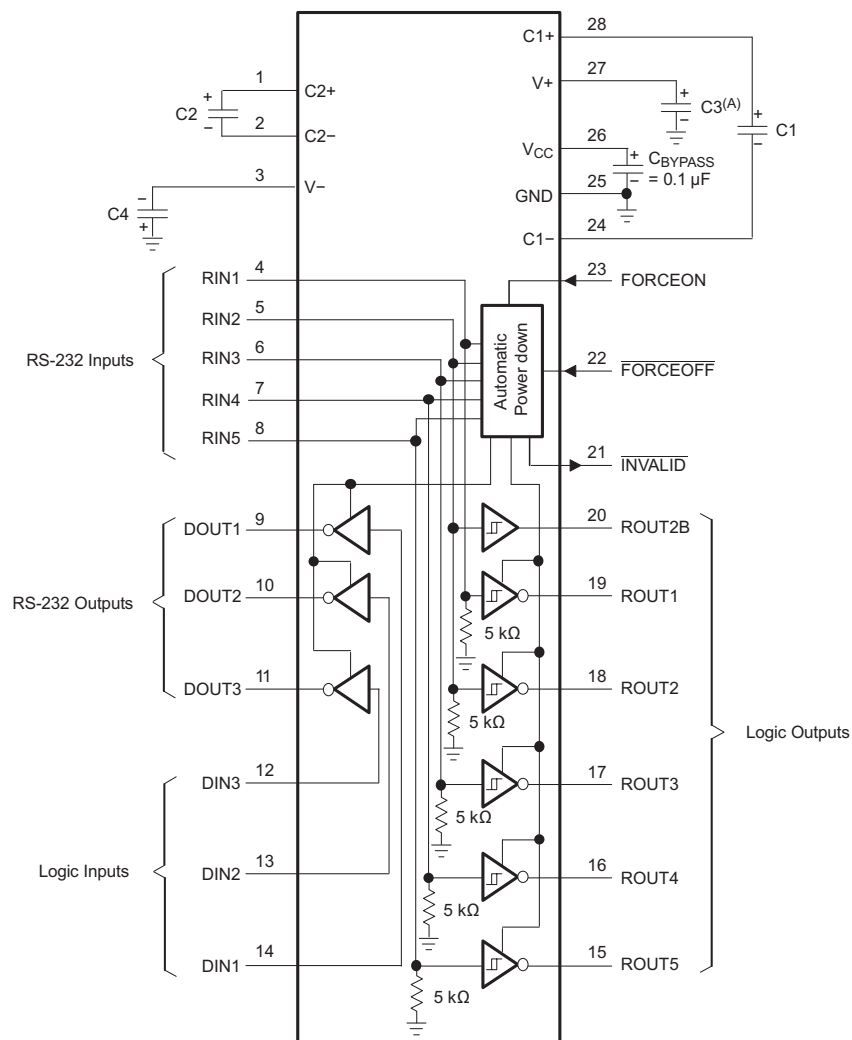
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

9.1 Application Information

The TRS3221 device is designed to convert single-ended signals into RS232-compatible signals, and vice-versa.

This device can be used in any application where an RS232 line driver or receiver is required. One benefit of this device is its ESD protection, which helps protect other components on the board when the RS232 lines are tied to a physical connector. The device also features an automatic power-down circuit.

9.2 Typical Application



- C3 can be connected to V_{CC} or GND.
- Resistor values shown are nominal.
- Nonpolarized ceramic capacitors are acceptable. If polarized tantalum or electrolytic capacitors are used, they must be connected as shown.

Figure 8. Typical Operating Circuit and Capacitor Values

Typical Application (continued)

9.2.1 Design Requirements

- V_{CC} minimum is 3 V and maximum is 5.5 V
- Maximum recommended bit rate is 250 kbps

Table 4. V_{CC} versus Capacitor Values

V_{CC}	C1	C2, C3, C4
3.3 V \pm 0.3 V	0.1 μ F	0.1 μ F
5 V \pm 0.5 V	0.047 μ F	0.33 μ F
3 V to 5.5 V	0.1 μ F	0.47 μ F

9.2.2 Detailed Design Procedure

It is recommended to add capacitors as shown in [Figure 8](#).

All DIN, $\overline{\text{FORCEOFF}}$ and FORCEON inputs must be connected to valid low or high logic levels.

Select capacitor values based on V_{CC} level for best performance.

9.2.3 Application Curve

$V_{CC} = 3.3$ V

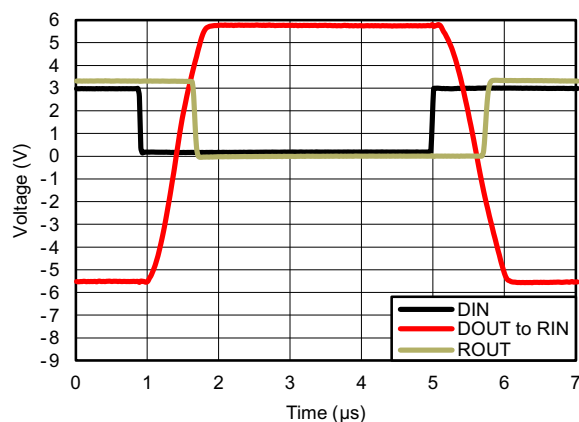


Figure 9. Driver to Receiver Loopback Timing Waveform

10 Power Supply Recommendations

V_{CC} must be between 3 V and 5.5 V. Charge pump capacitors must be chosen using [Table 4](#).

11 Layout

11.1 Layout Guidelines

Keep the external capacitor traces short. This is more important on C1 and C2 nodes that have the fastest rise and fall times.

[Figure 10](#) shows only critical layout sections. Input and output traces will vary in shape and size depending on the customer application. FORCEON and FORCEOFF must be pulled up to VCC or GND through a pullup resistor, depending on which configuration is desired upon powerup.

11.2 Layout Example

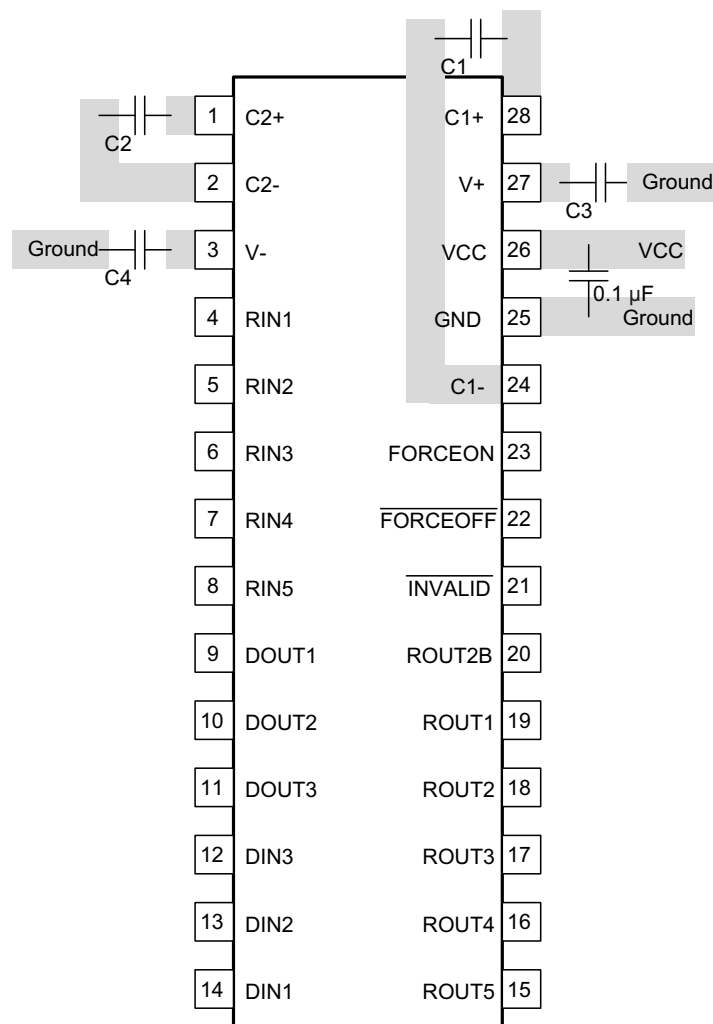


Figure 10. Layout Diagram

12 Device and Documentation Support

12.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's [Terms of Use](#).

TI E2E™ Online Community *TI's Engineer-to-Engineer (E2E) Community*. Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support *TI's Design Support* Quickly find helpful E2E forums along with design support tools and contact information for technical support.

12.2 Trademarks

E2E is a trademark of Texas Instruments.

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All other trademarks are the property of their respective owners.

12.3 Electrostatic Discharge Caution



These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

12.4 Glossary

[SLYZ022](#) — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

13 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
TRS3243CDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	TRS3243C	Samples
TRS3243CPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43C	Samples
TRS3243CPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	0 to 70	RS43C	Samples
TRS3243IDB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples
TRS3243IDBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	TRS3243I	Samples
TRS3243IPW	ACTIVE	TSSOP	PW	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43I	Samples
TRS3243IPWR	ACTIVE	TSSOP	PW	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-40 to 85	RS43I	Samples

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

⁽⁵⁾ Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

⁽⁶⁾ Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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TAPE AND REEL INFORMATION

QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
TRS3243CDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243CPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1
TRS3243IDBR	SSOP	DB	28	2000	330.0	16.4	8.2	10.5	2.5	12.0	16.0	Q1
TRS3243IPWR	TSSOP	PW	28	2000	330.0	16.4	6.9	10.2	1.8	12.0	16.0	Q1

TAPE AND REEL BOX DIMENSIONS


*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
TRS3243CDBR	SSOP	DB	28	2000	367.0	367.0	38.0
TRS3243CPWR	TSSOP	PW	28	2000	367.0	367.0	38.0
TRS3243IDBR	SSOP	DB	28	2000	367.0	367.0	38.0
TRS3243IPWR	TSSOP	PW	28	2000	367.0	367.0	38.0

MECHANICAL DATA

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



4040064-7/G 02/11

- NOTES:
- A. All linear dimensions are in millimeters. Dimensioning and tolerancing per ASME Y14.5M-1994.
 - B. This drawing is subject to change without notice.
 - C. Body length does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0,15 each side.
 - D. Body width does not include interlead flash. Interlead flash shall not exceed 0,25 each side.
 - E. Falls within JEDEC MO-153

PW (R-PDSO-G28)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
 - This drawing is subject to change without notice.
 - Publication IPC-7351 is recommended for alternate design.
 - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC-7525 for other stencil recommendations.
 - Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.

DB0028A



PACKAGE OUTLINE

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



4214853/B 03/2018

NOTES:

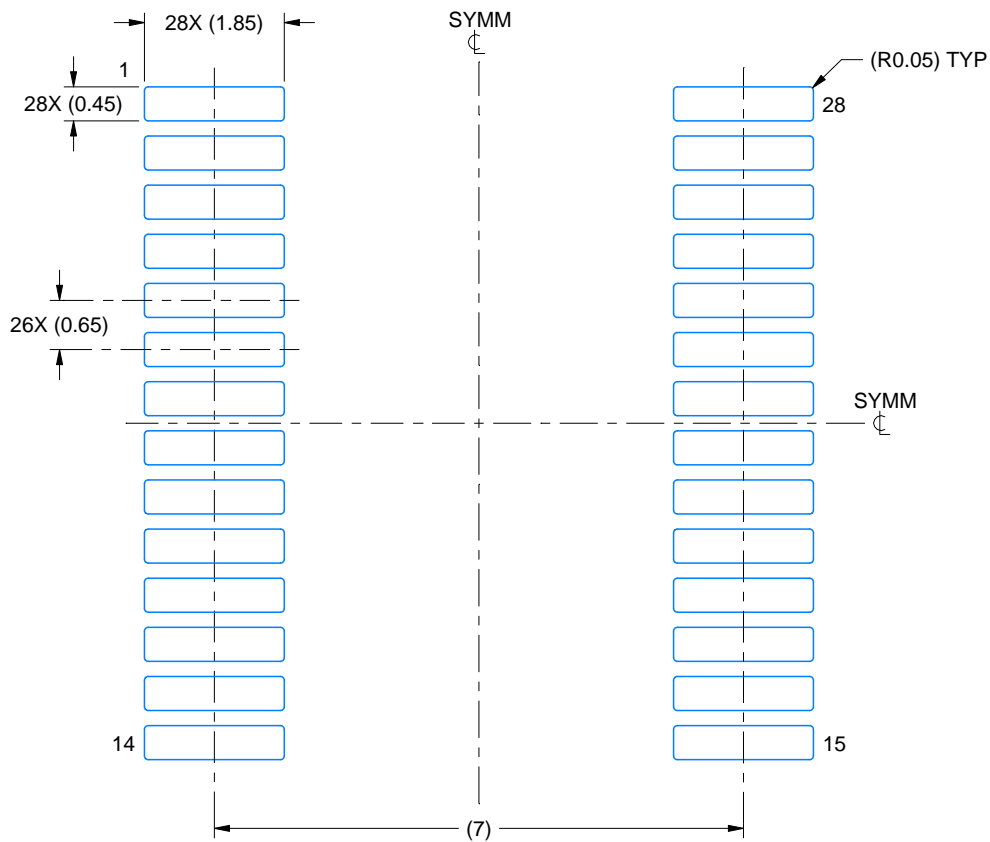
- All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
- This drawing is subject to change without notice.
- This dimension does not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.
- This dimension does not include interlead flash. Interlead flash shall not exceed 0.25 mm per side.
- Reference JEDEC registration MO-150.

EXAMPLE BOARD LAYOUT

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE: 10X



4214853/B 03/2018

NOTES: (continued)

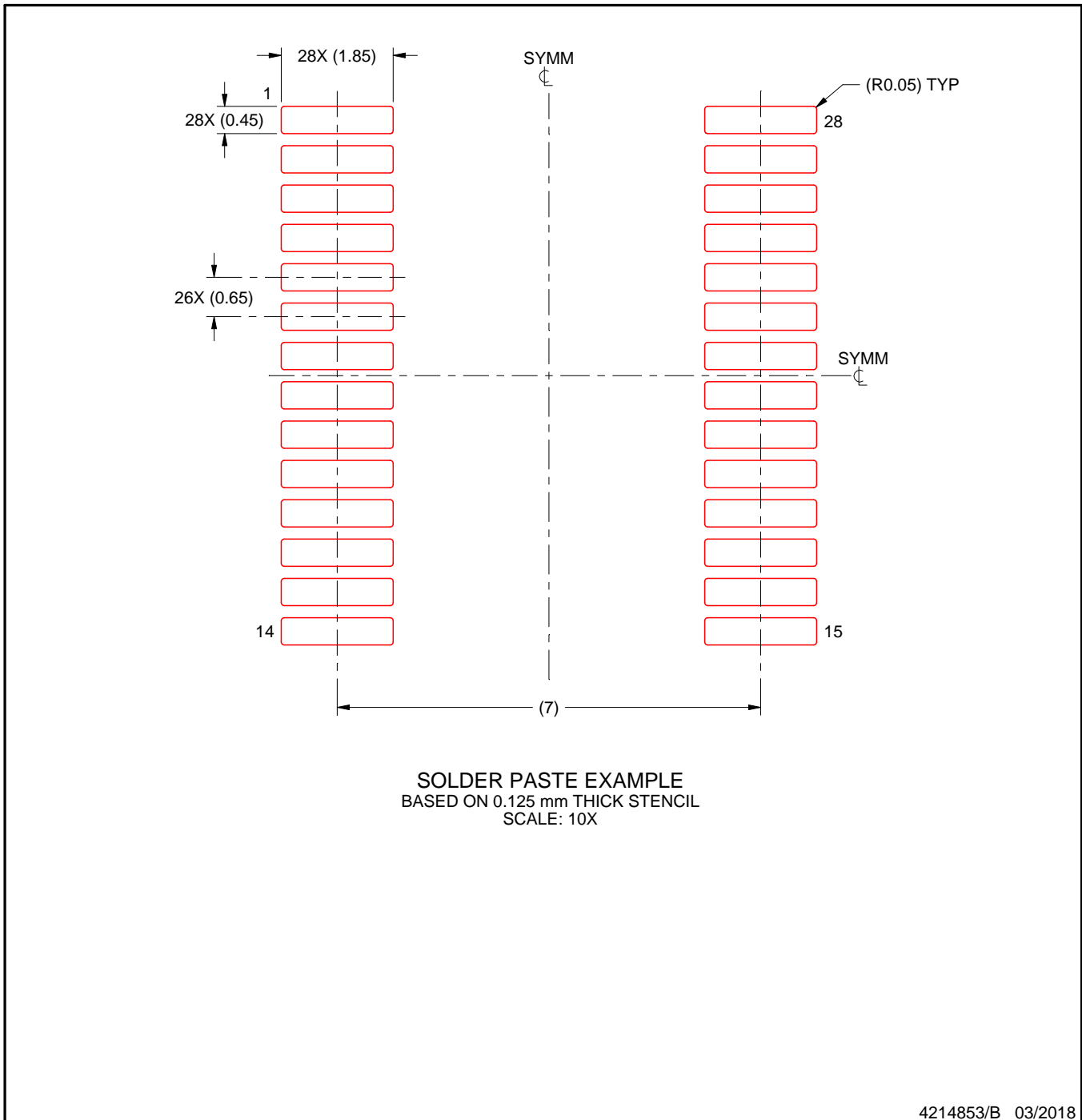
- 6. Publication IPC-7351 may have alternate designs.
- 7. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

EXAMPLE STENCIL DESIGN

DB0028A

SSOP - 2 mm max height

SMALL OUTLINE PACKAGE



NOTES: (continued)

8. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
9. Board assembly site may have different recommendations for stencil design.

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