



# THE DATASHEET OF STD45N10F7



N-channel 100 V, 0.0145  $\Omega$  typ., 45 A, STripFET™ F7 Power MOSFETs in DPAK, I<sup>2</sup>PAK and TO-220 packages

Datasheet - production data

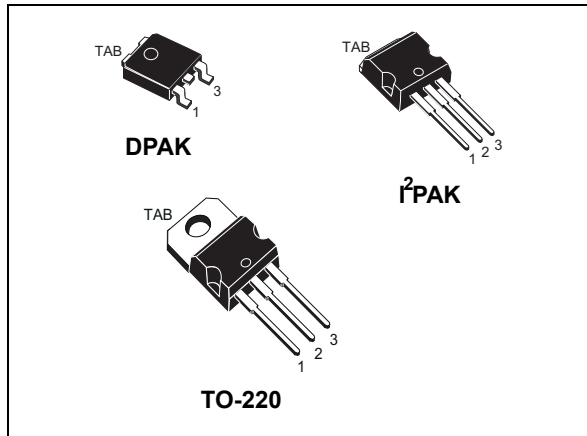
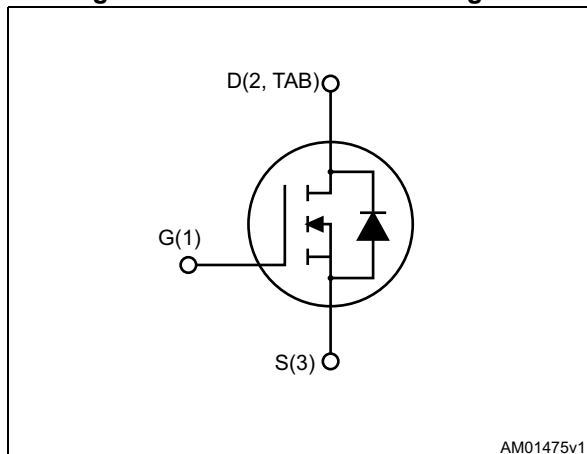


Figure 1. Internal schematic diagram



## Features

Order code	V <sub>DS</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>	P <sub>TOT</sub>
STD45N10F7	100 V	0.018 $\Omega$	45 A	60 W
STI45N10F7				
STP45N10F7				

- Among the lowest R<sub>DS(on)</sub> on the market
- Excellent figure of merit (FoM)
- Low C<sub>rSS</sub>/C<sub>iSS</sub> ratio for EMI immunity
- High avalanche ruggedness

## Applications

- Switching applications

## Description

These N-channel Power MOSFETs utilize STripFET™ F7 technology with an enhanced trench gate structure that results in very low on-state resistance, while also reducing internal capacitance and gate charge for faster and more efficient switching.

Table 1. Device summary

Order code	Marking	Package	Packing
STD45N10F7	45N10F7	DPAK	Tape and reel
STI45N10F7		I <sup>2</sup> PAK	Tube
STP45N10F7		TO-220	

# Contents

- 1      Electrical ratings ..... 3**
- 2      Electrical characteristics ..... 4**
  - 2.1    Electrical characteristics (curves) ..... 6
- 3      Test circuits ..... 8**
- 4      Package information ..... 9**
  - 4.1    DPAK (TO-252) package information ..... 9
  - 4.2    I<sup>2</sup>PAK (TO-262) package information ..... 12
  - 4.3    TO-220 type A package information ..... 14
- 5      Packing mechanical data ..... 16**
- 6      Revision history ..... 19**

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{DS}$	Drain-source voltage	100	V
$V_{GS}$	Gate-source voltage	±20	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	45	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	32	A
$I_{DM}^{(1)}$	Drain current (pulsed)	180	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	60	W
$E_{AS}^{(2)}$	Single pulse avalanche energy	190	mJ
$T_J$	Operating junction temperature	-55 to 175	°C
$T_{stg}$	Storage temperature		°C

1. Pulse width limited by safe operating area.
2. Starting  $T_J = 25\text{ °C}$ ,  $I_d = 10\text{ A}$ ,  $V_{dd} = 50\text{ V}$

**Table 3. Thermal resistance**

Symbol	Parameter	Value		Unit
		DPAK	TO-220 I <sup>2</sup> PAK	
$R_{thj-case}$	Thermal resistance junction-case	2.5	2.5	°C/W
$R_{thj-amb}$	Thermal resistance junction-ambient		62.5	°C/W
$R_{thj-pcb}^{(1)}$	Thermal resistance junction-pcb	31.2		°C/W

1. When mounted on FR-4 board of 1inch<sup>2</sup>, 2oz Cu,  $t < 10\text{ sec}$ .

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	100		-	V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 100\text{ V}$			10	$\mu\text{A}$
		$V_{DS} = 100\text{ V}; T_C = 125\text{ °C}$			100	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 20\text{ V}$			$\pm 100$	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2.5		4.5	V
$R_{DS(on)}$	Static drain-source on-resistance	$V_{GS} = 10\text{ V}, I_D = 22.5\text{ A}$		0.0145	0.018	$\Omega$

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz}, V_{GS} = 0$	-	1640	-	pF
$C_{oss}$	Output capacitance		-	360	-	pF
$C_{riss}$	Reverse transfer capacitance		-	25	-	pF
$Q_g$	Total gate charge	$V_{DD} = 50\text{ V}, I_D = 45\text{ A}$	-	25	-	nC
$Q_{gs}$	Gate-source charge	$V_{GS} = 10\text{ V}$	-	5.1	-	nC
$Q_{gd}$	Gate-drain charge	<a href="#">Figure 14</a>	-	12.2	-	nC

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 50\text{ V}, I_D = 22.5\text{ A}, R_G = 4.7\text{ }\Omega, V_{GS} = 10\text{ V}$ <a href="#">Figure 13</a>	-	15	-	ns
$t_r$	Rise time		-	17	-	ns
$t_{d(off)}$	Turn-off delay time		-	24	-	ns
$t_f$	Fall time		-	8	-	ns

Table 7. Source-drain diode

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		45	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)		-		180	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 45 \text{ A}$ , $V_{GS} = 0$	-		1.1	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 45 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$ , $V_{DD} = 80 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$	-	53		ns
$Q_{rr}$	Reverse recovery charge		-	67		nC
$I_{RRM}$	Reverse recovery current		-	2.5		A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration=300  $\mu\text{s}$ , duty cycle 1.5%.

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

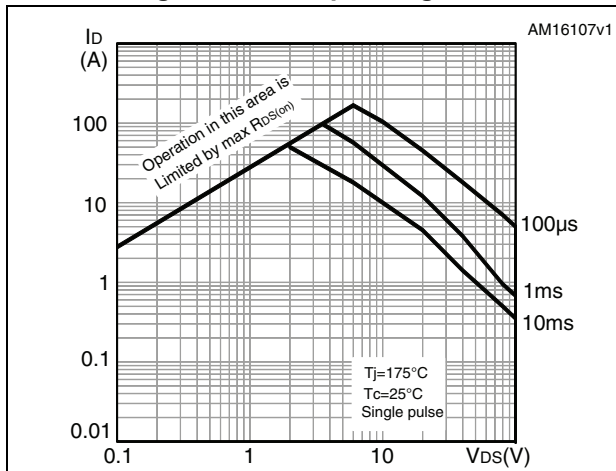


Figure 3. Thermal impedance

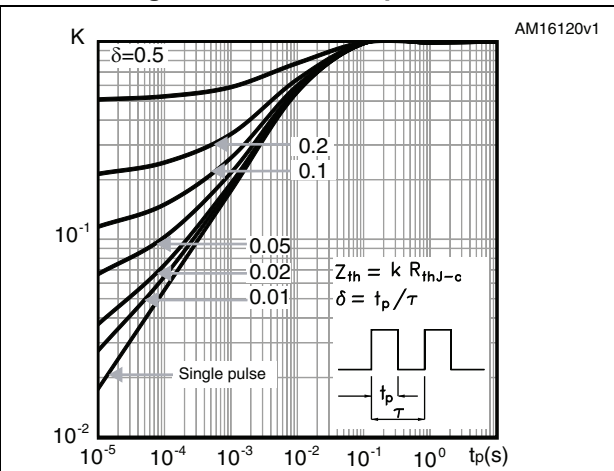


Figure 4. Output characteristics

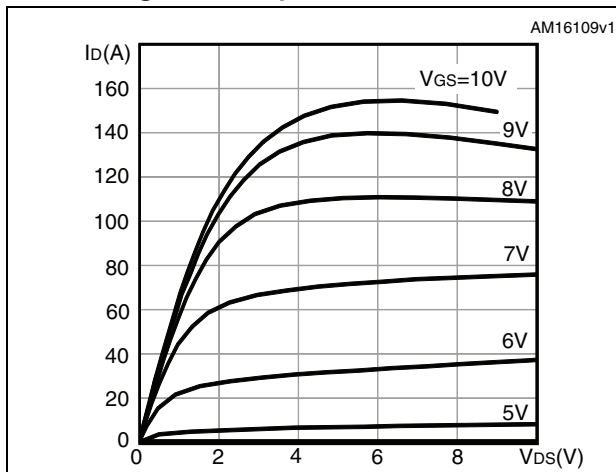


Figure 5. Transfer characteristics

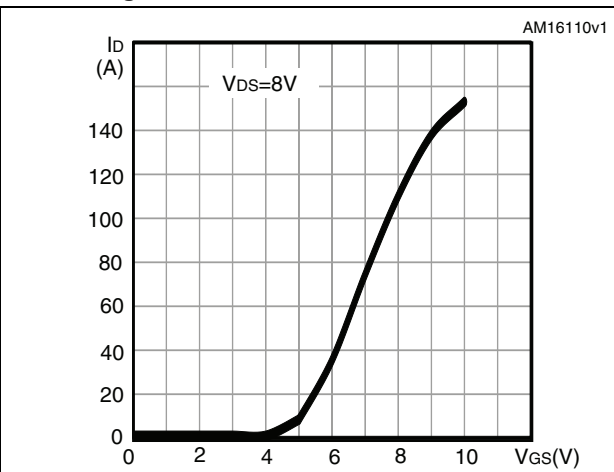


Figure 6. Gate charge vs gate-source voltage

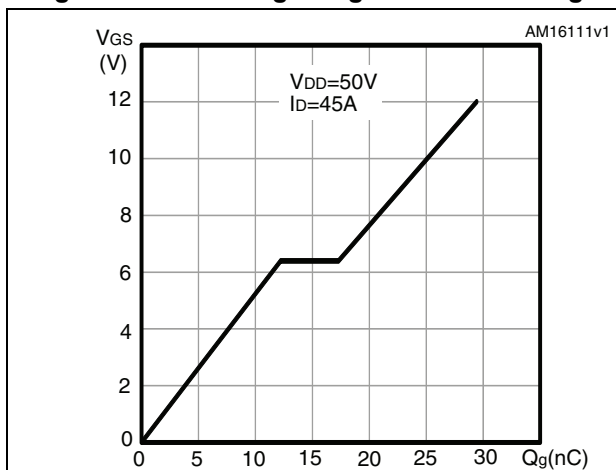


Figure 7. Static drain-source on-resistance

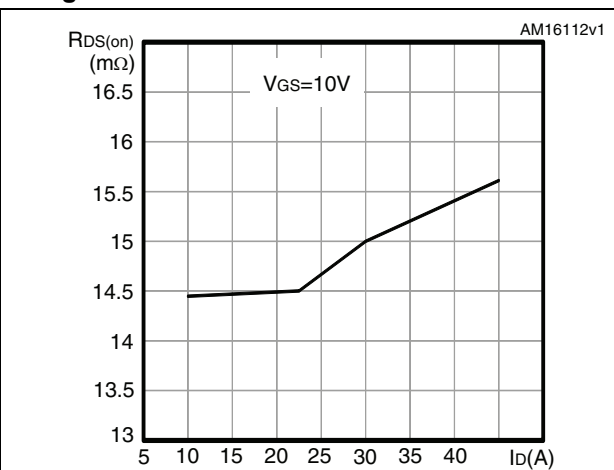


Figure 8. Capacitance variations

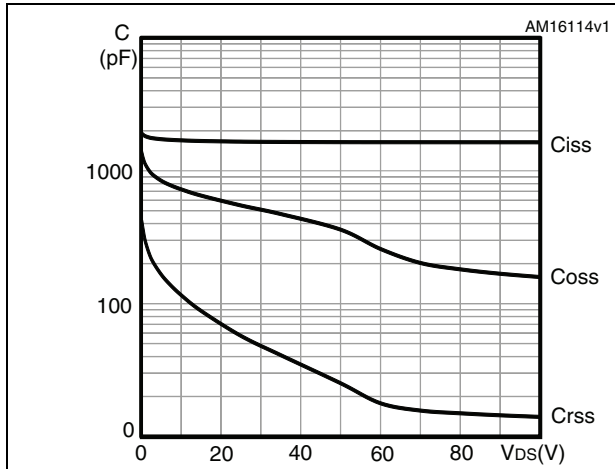


Figure 9. Normalized gate threshold voltage vs temperature

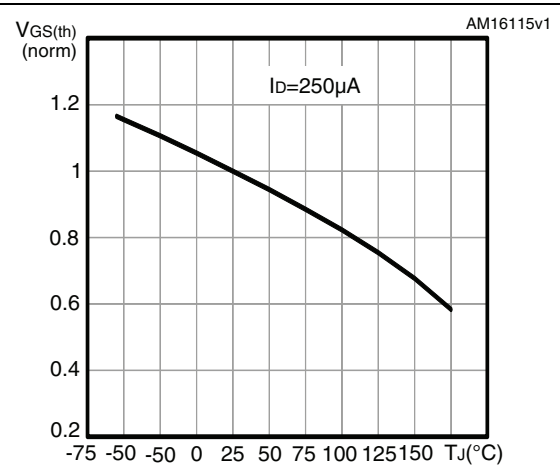


Figure 10. Normalized on-resistance vs temperature

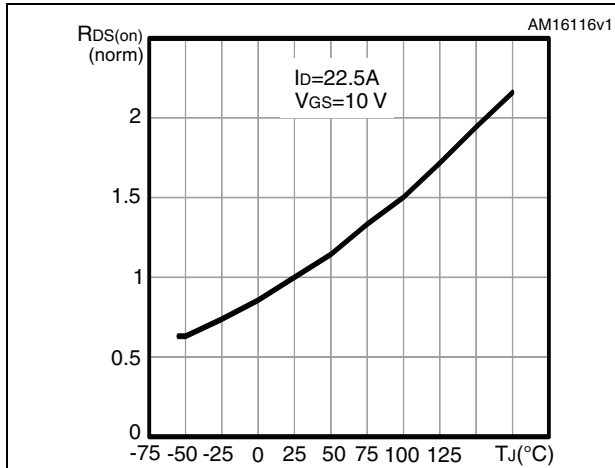


Figure 11. Source-drain diode forward characteristics

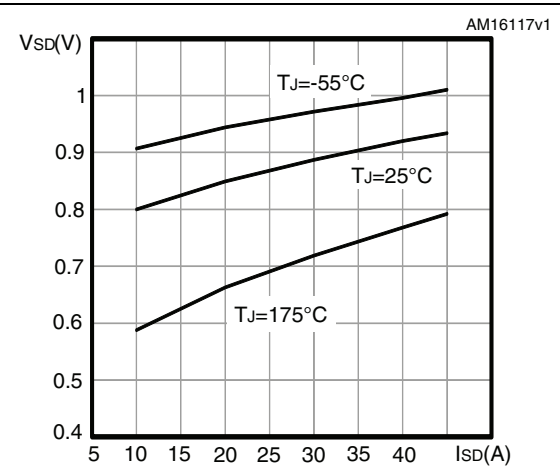
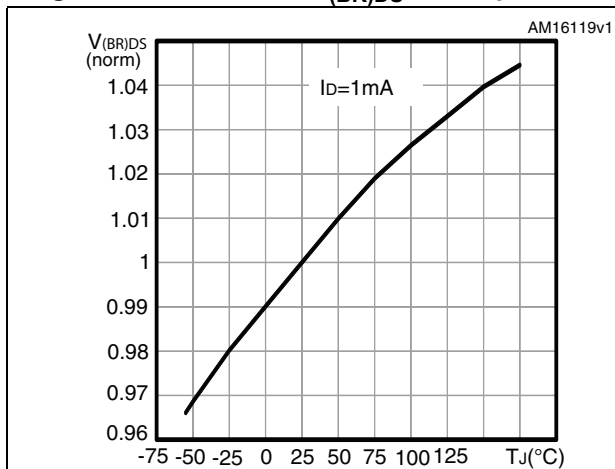


Figure 12. Normalized V(BR)DS vs temperature



### 3 Test circuits

Figure 13. Switching times test circuit for resistive load

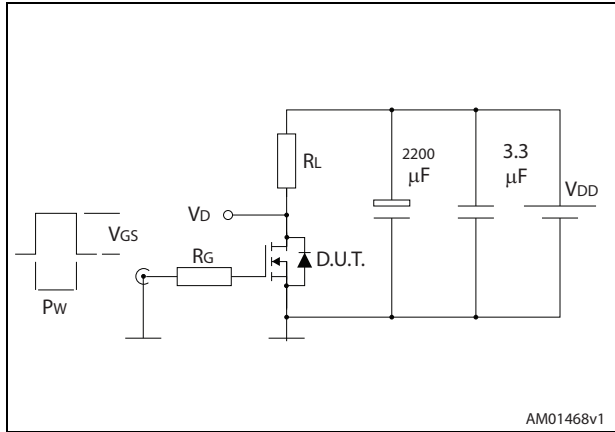


Figure 14. Gate charge test circuit

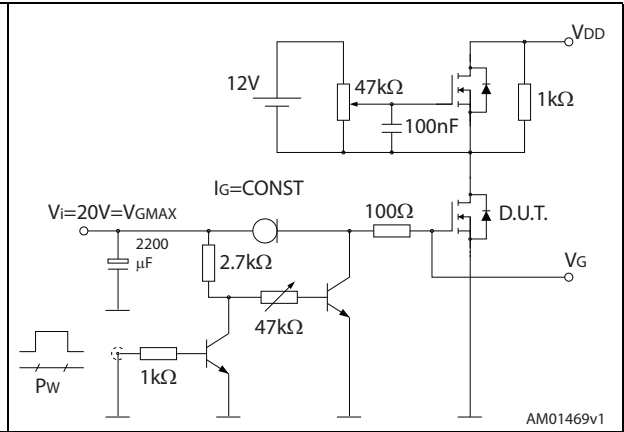


Figure 15. Test circuit for inductive load switching and diode recovery times

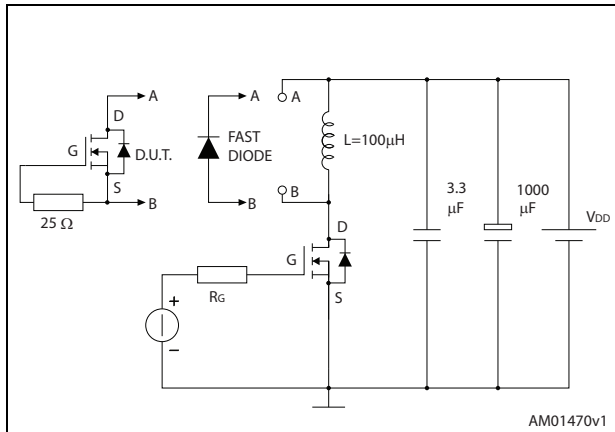


Figure 16. Unclamped inductive load test circuit

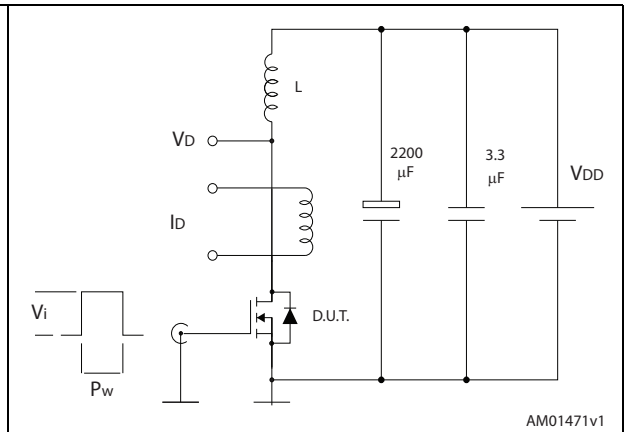


Figure 17. Unclamped inductive waveform

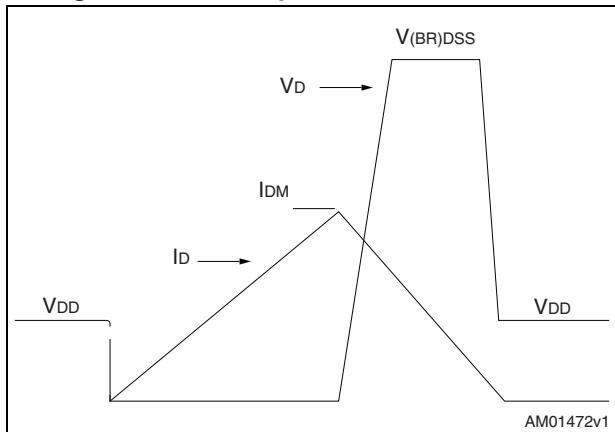
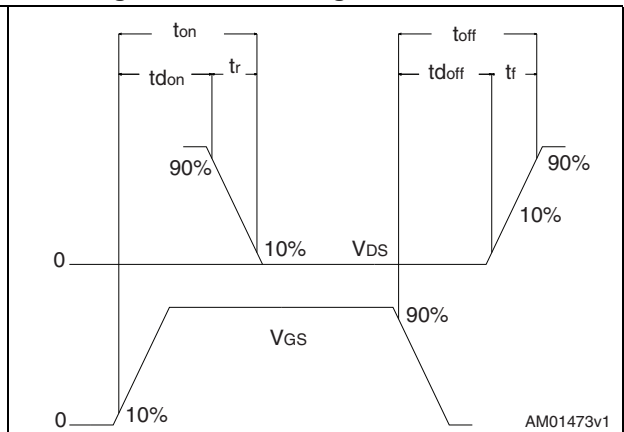


Figure 18. Switching time waveform



## 4 Package information

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

### 4.1 DPAK (TO-252) package information

Figure 19. DPAK (TO-252) type A package outline

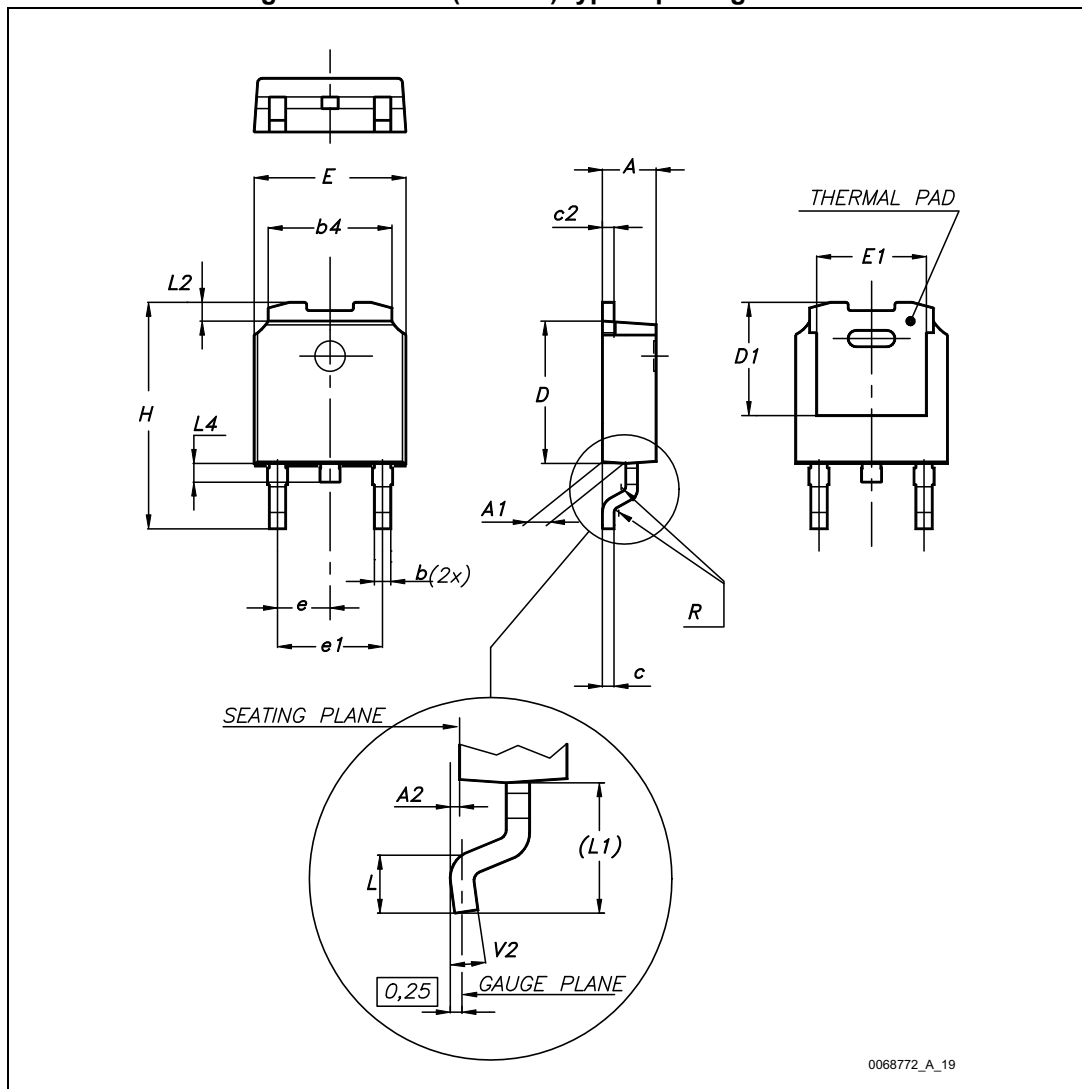
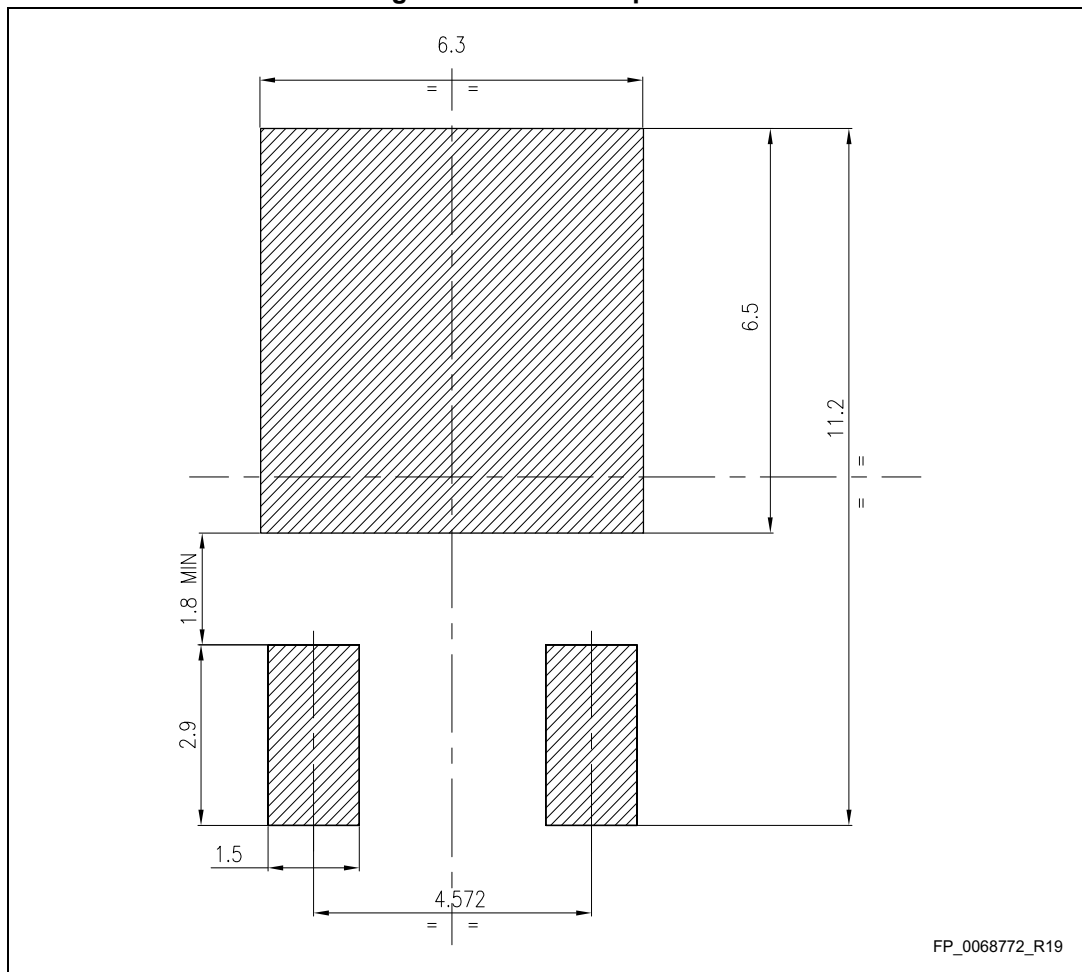


Table 8. DPAK (TO-252) type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.16	2.28	2.40
e1	4.40		4.60
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

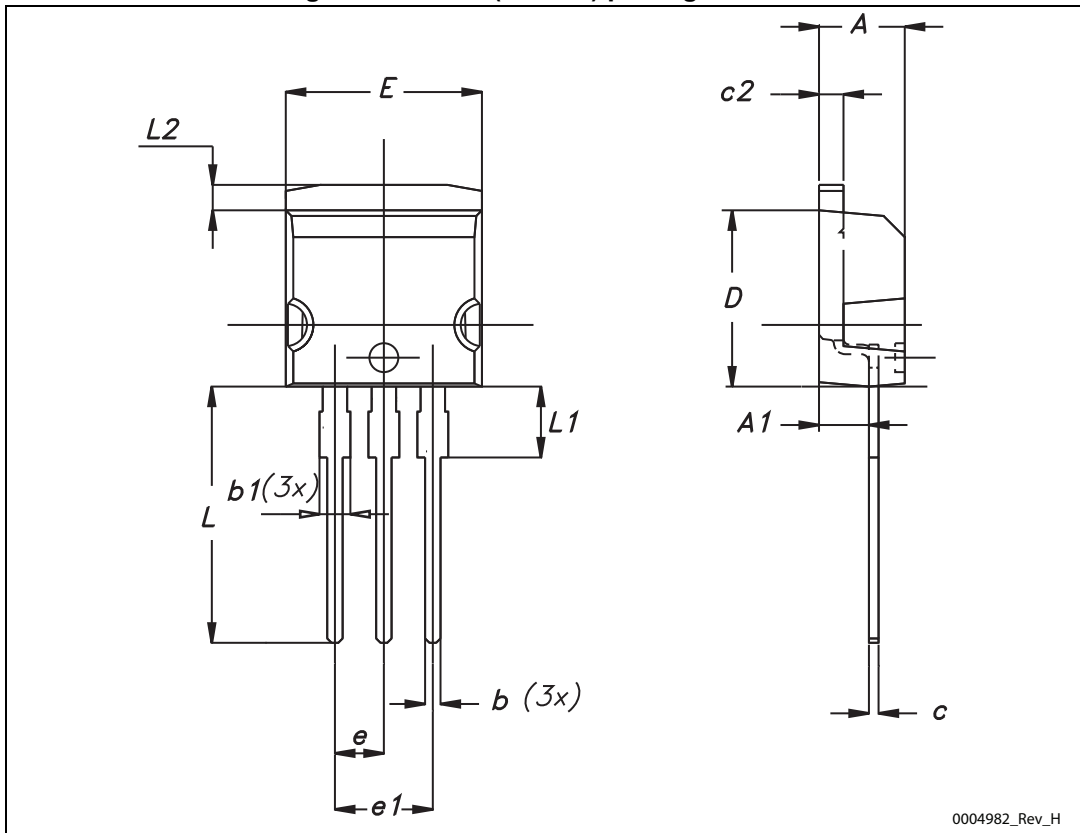
Figure 20. DPAK footprint (a)



a. All dimensions are in millimeters

### 4.2 I<sup>2</sup>PAK (TO-262) package information

Figure 21. I<sup>2</sup>PAK (TO-262) package outline



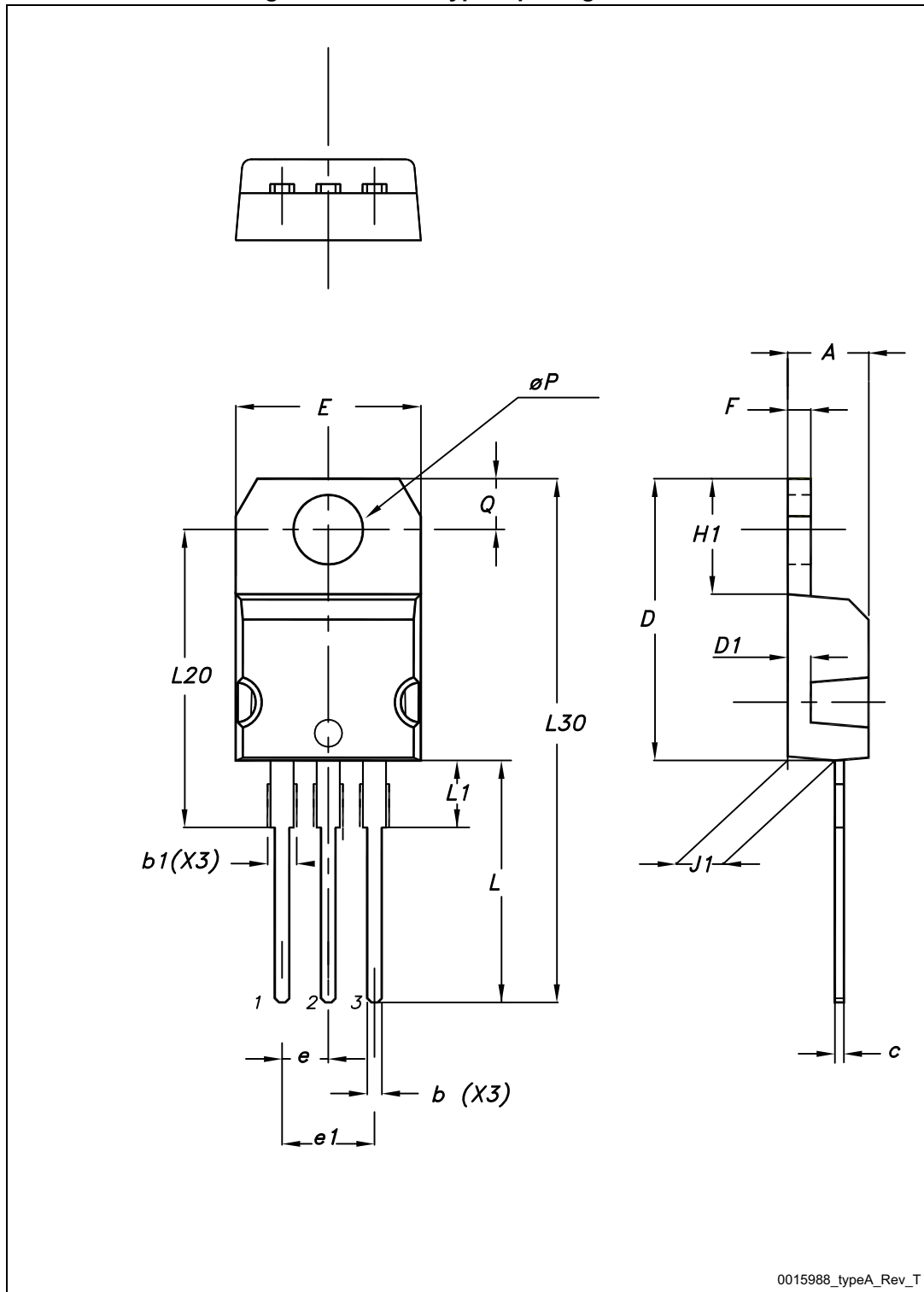
0004982\_Rev\_H

Table 9. I<sup>2</sup>PAK (TO-262) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
A1	2.40		2.72
b	0.61		0.88
b1	1.14		1.70
c	0.49		0.70
c2	1.23		1.32
D	8.95		9.35
e	2.40		2.70
e1	4.95		5.15
E	10		10.40
L	13		14
L1	3.50		3.93
L2	1.27		1.40

### 4.3 TO-220 type A package information

Figure 22. TO-220 type A package outline



0015988\_typeA\_Rev\_T

Table 10. TO-220 type A mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	4.40		4.60
b	0.61		0.88
b1	1.14		1.70
c	0.48		0.70
D	15.25		15.75
D1		1.27	
E	10		10.40
e	2.40		2.70
e1	4.95		5.15
F	1.23		1.32
H1	6.20		6.60
J1	2.40		2.72
L	13		14
L1	3.50		3.93
L20		16.40	
L30		28.90	
ØP	3.75		3.85
Q	2.65		2.95

# 5 Packing mechanical data

Figure 23. Tape

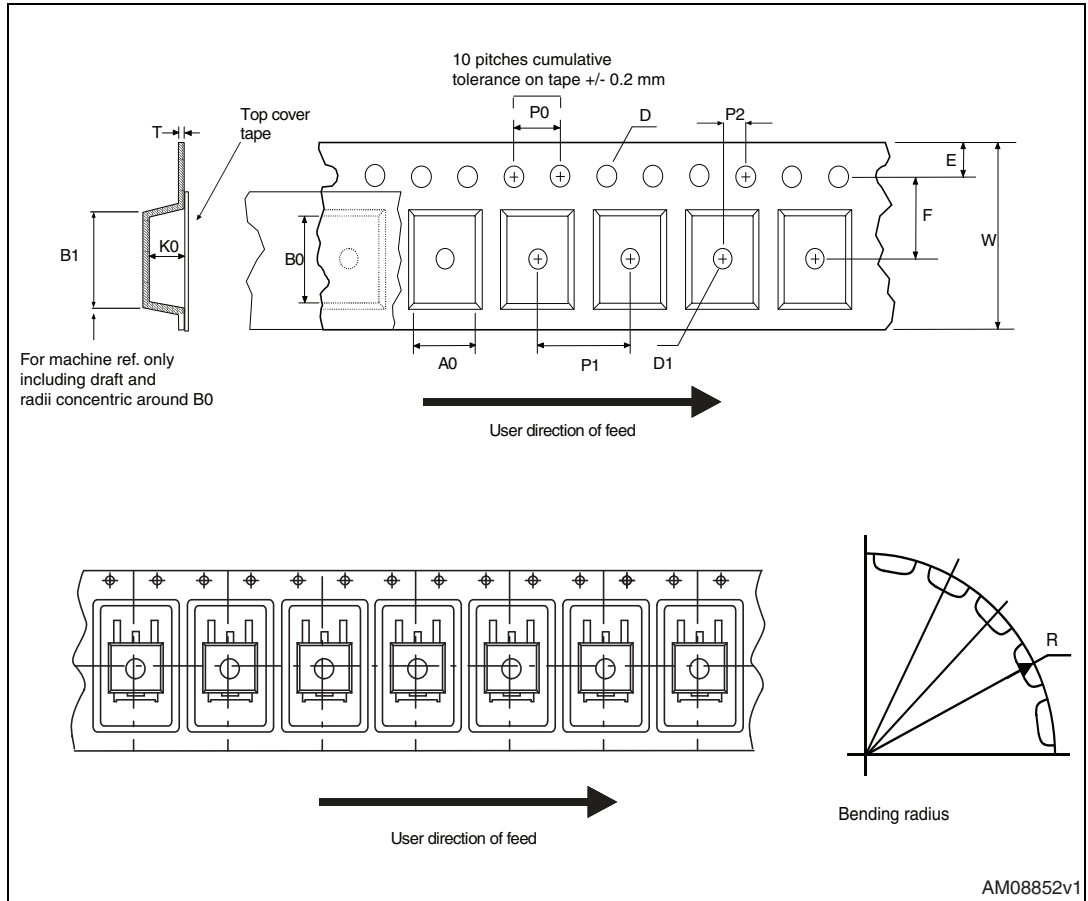


Figure 24. Reel

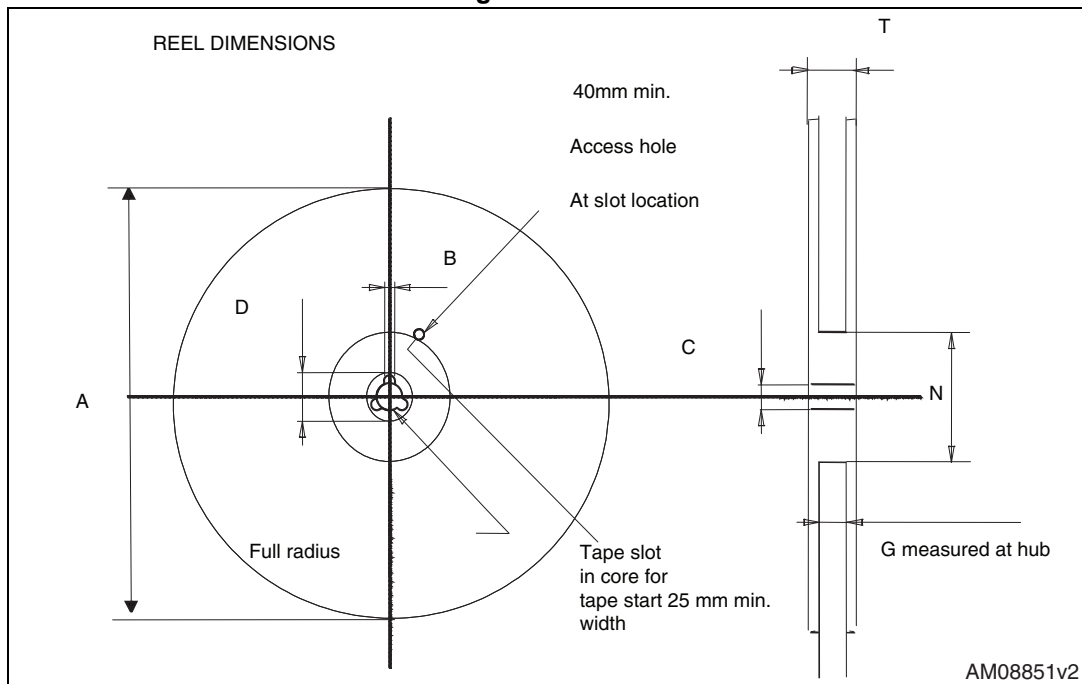


Table 11. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

## 6 Revision history

Table 12. Document revision history

Date	Revision	Changes
10-Oct-2013	1	First release.
08-Sep-2015	2	Updated title, features and description in cover page Updated <a href="#">Table 2.: Absolute maximum ratings</a> Updated <a href="#">4.1: DPAK (TO-252) package information</a> Minor text changes.

**IMPORTANT NOTICE – PLEASE READ CAREFULLY**

STMicroelectronics NV and its subsidiaries ("ST") reserve the right to make changes, corrections, enhancements, modifications, and improvements to ST products and/or to this document at any time without notice. Purchasers should obtain the latest relevant information on ST products before placing orders. ST products are sold pursuant to ST's terms and conditions of sale in place at the time of order acknowledgement.

Purchasers are solely responsible for the choice, selection, and use of ST products and ST assumes no liability for application assistance or the design of Purchasers' products.

No license, express or implied, to any intellectual property right is granted by ST herein.

Resale of ST products with provisions different from the information set forth herein shall void any warranty granted by ST for such product.

ST and the ST logo are trademarks of ST. All other product or service names are the property of their respective owners.

Information in this document supersedes and replaces information previously supplied in any prior versions of this document.

© 2015 STMicroelectronics – All rights reserved

## Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- ⊖ [View STD45N10F7](#) on WIN SOURCE
- ⊖ [STMicroelectronics](#) Information

## Optimize Your Supply Chain with WIN SOURCE Solutions

- ✓ Global Sourcing Solution
- ✓ Obsolete Management
- ✓ Cost Control Management
- ✓ Shortage Management
- ✓ Alternative Solution
- ✓ Excess Inventory Management