THE DATASHEET OF

PT7A7533WEX

Features

- Precision supply-voltage monitor
  - 4.63V (PT7A7511, 7521, 7531)
  - 4.38V (PT7A7512, 7522, 7532)
  - 3.08V (PT7A7513, 7523, 7533)
  - 2.93V (PT7A7514, 7524, 7534)
  - 2.63V (PT7A7515, 7525, 7535)
- 200ms reset pulse width
- Debounced TTL/CMOS-compatible manual-reset input
- Independent watchdog timer 1.6sec time-out (not available for PT7A7531 - 7535)
- Reset output signal:
  - Active-low only (PT7A7511 - 7515)
  - Active-high only (PT7A7521 - 7525)
  - Active-high and active-low (PT7A7531 - 7535)
- Voltage monitor for power-fail or low battery warning
- Guaranteed $\overline{\text{RESET}}$/RESET valid at V_{CC}=1.2V

Description

The PT7A751X/752X/753X family micro-processor (µP) supervisory circuits are targeted to improve reliability and accuracy of power-supply circuitry in µP's systems. These devices reduce the complexity and number of components required to monitor power-supply and battery functions.

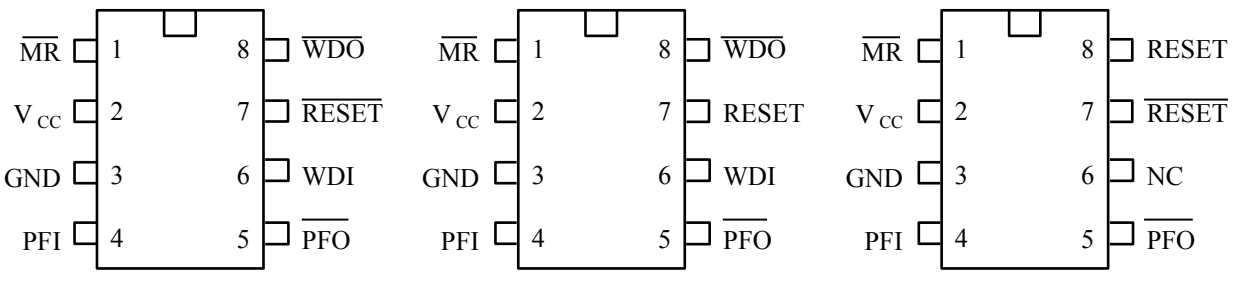
The main functions are:

1. Asserting reset output during power-up, power-down and brownout conditions for µP system.
2. Detecting power failure or low-battery conditions with a 1.25V threshold detector.
3. Watchdog functions (not for PT7A753x)

Applications

- Power-supply circuitry in µP systems

Pin Configuration



Top View

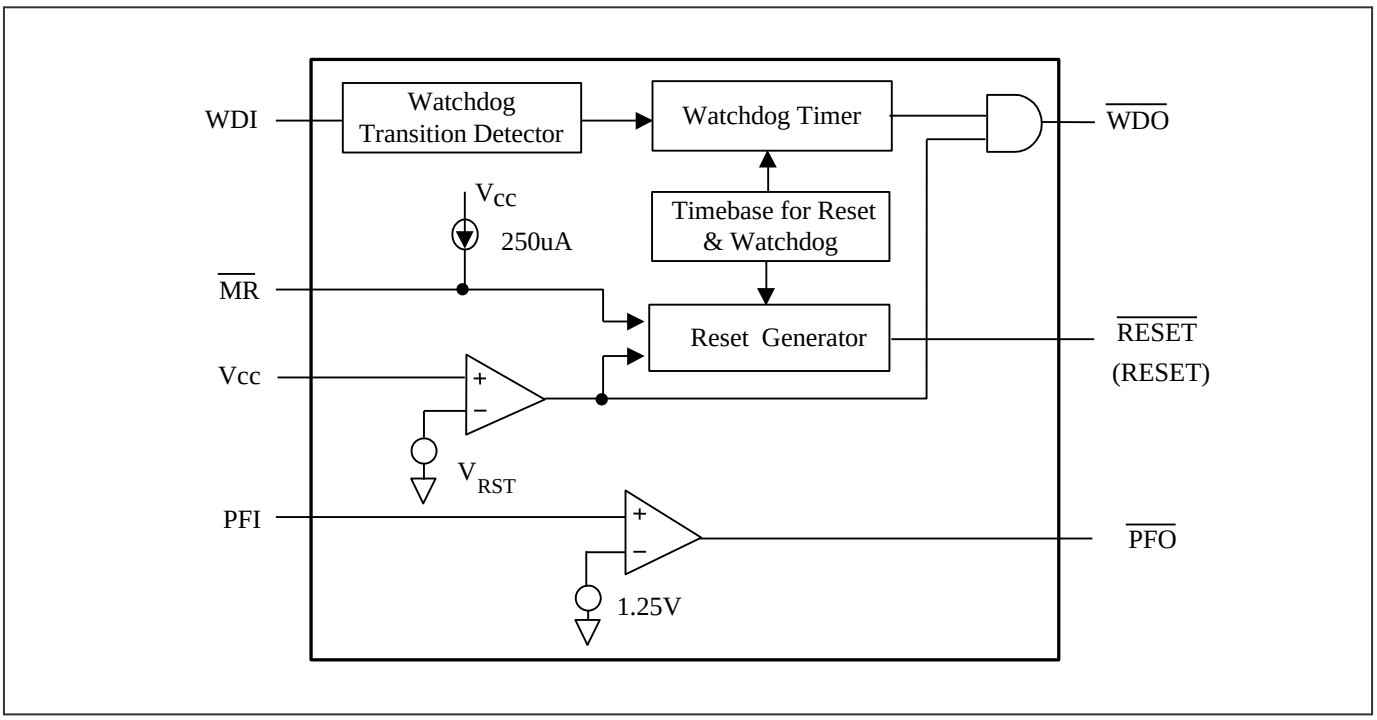
PT7A7511W-7515W **PT7A7521W-7525W** **PT7A7531W-7535W**

Pin Description

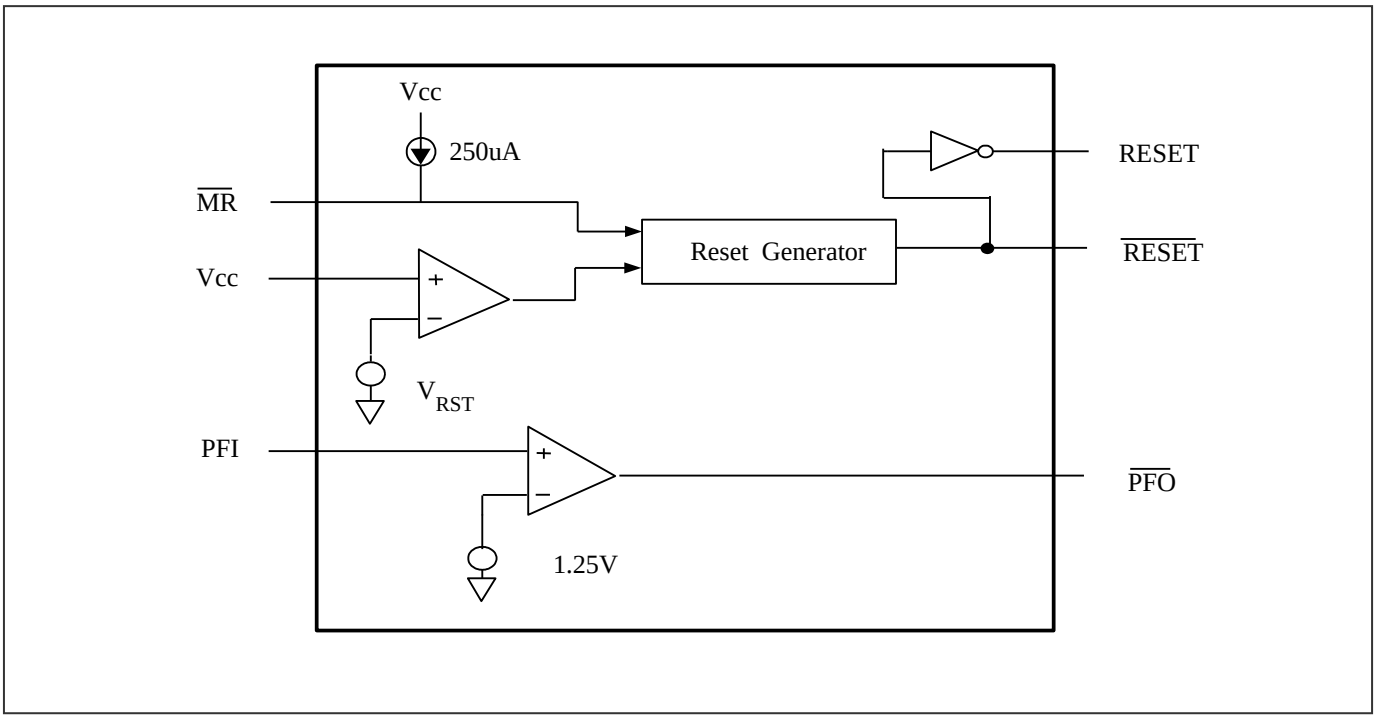
Pin	Type	Description
$\overline{MR}$	I	**Manual-Reset:** triggers a reset pulse when pulled below 0.8V, active low. It has an internal 250 µA pull-up current and be driven from a TTL or CMOS logic line as well as shorted to ground with a switch.
V_{CC}	Power	**Supply Voltage.**
GND	Ground	**Ground Reference** for all signals.
PFI	I	**Power-Fail Voltage Monitor Input.** When PFI is less than 1.25V, PFO goes low. Connect PFI to GND or Vcc when not used.
$\overline{PFO}$	O	**Power-Fail Output:** it gets low and sinks current when PFI is less than 1.25V; otherwise $\overline{PFO}$ stays high.
WDI	I	**Watchdog Input:** If WDI remains high or low for 1.6sec, the internal watchdog timer runs out and $\overline{WDO}$ goes low. Floating WDI or connecting WDI to a high-impedance three-state buffer disables the watchdog feature. The internal watchdog timer clears whenever reset is asserted. WDI is three-stated, or WDI sees a rising or falling edge.
$\overline{RESET}$	O	**Reset Output pulses:** low for 200ms when triggered, and stays low whenever Vcc is below the reset threshold. It remains low for 200ms after Vcc rises above the reset threshold or $\overline{MR}$ goes from low to high. A watchdog timeout will not trigger $\overline{RESET}$ unless $\overline{WDO}$ is connected to $\overline{MR}$.
$\overline{WDO}$	O	**Watchdog Output:** pulls low when the internal watchdog timer finishes its 1.6sec count and does not go high again until the watchdog is cleared. $\overline{WDO}$ also goes low during low-line conditions. Whenever Vcc is below the reset threshold, WDO stays low; however, unlike $\overline{RESET}$, $\overline{WDO}$ does not have minimum pulse width. As soon as Vcc rises above the reset threshold, $\overline{WDO}$ goes high with no delay.
RESET	O	**The inverse of $\overline{RESET}$,** active high. Whenever $\overline{RESET}$ is high, RESET is low.

Block Diagram

Block Diagram of PT7A7511-7515/7521-7525



Block Diagram of PT7A7531-35



Maximum Ratings

Storage Temperature ..... -65°C to +150°C
Ambient Temperature with Power Applied..... -40°C to +85°C
Supply Voltage to Ground Potential (Vcc to GND) .....-0.3V to +7.0V
DC Input Voltage (All inputs except Vcc and GND).....-0.3V to V_{CC}+0.3V
DC Output Current (All outputs) 20mA
Power Dissipation ..... 500mW (Depend on package)

Note:
Stresses greater than those listed under MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
V_{CC}	Supply Voltage for 75x1,75x2	-	4.5	5.0	5.5	V
	Supply Voltage for 75x3,75x4	-	3.0	3.3	5.5	V
	Supply Voltage for 75x5		2.7	3.0	5.5	
V_{IH1}	$\overline{MR}$ Input High Voltage	V_{CC} > 4.0V	2.0	2.4	V_{CC}	V
		$V_{CC} \leq$ 4.0V	0.7V_{CC}	-	V_{CC}	V
V_{IH2}	WDI Input High Voltage	-	0.7V_{CC}	-	V_{CC}	V
V_{IL1}	$\overline{MR}$ Input Low Voltage	V_{CC} > 4.0V	-	-	0.8	V
		$V_{CC} \leq$ 4.0V	-	-	0.2V_{CC}	V
V_{IL2}	WDI Input Low Voltage	-	-	-	0.3V_{CC}	V
T_A	Operating Temperature	-	-40	-	85	℃

DC Electrical Characteristics

(V_{CC} = V_{RN} + 5% to 5.5V, T_A= -40~85℃, unless otherwise noted.)(Note 1)

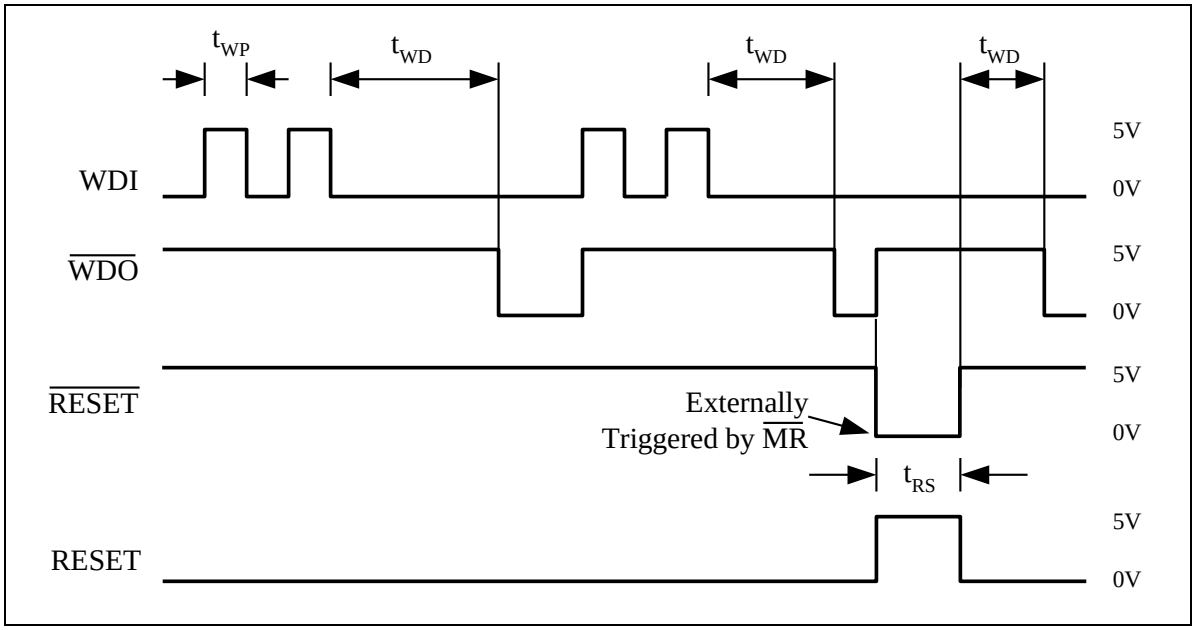
Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
I_{CC}	Supply Current	75x1/x2 Vcc = 5V, 75x3/x4 Vcc = 3.3V, 75x5 Vcc = 3.0V, Left WDI un-connected (No output load)	-	30	200	µA
V_{IH}	Input High Voltage	Pin: $\overline{MR}$, WDI	0.7V_{CC}	-	V_{CC}	V
V_{IL}	Input Low Voltage	Pin: $\overline{MR}$, WDI	-	-	0.3V_{CC}	V
V_{RST}	Reset Threshold Voltage (**Note 2**)	T_A= 25℃	V_{RN} - 1.5%	V_{RN}	V_{RN} + 1.5%	V
		75x1	4.560	4.630	4.699	
		75x2	4.314	4.380	4.446	
		75x3	3.034	3.080	3.126	
		75x4	2.886	2.930	2.974	
		75x5	2.590	2.630	2.669	
V_{RTH+}	Reset Threshold Voltage (**Note 2**)	V_{CC} Varies between V_{RN} - 5%	-	70	-	mV
V_{OH}	Output High Voltage	Vcc ≥ 4.5V Isource=800µA	Vcc-1.5	-	V_{CC}	V
		Vcc ≥ 2.7V Isource=500µA	0.8×Vcc	-	V_{CC}	
		Vcc ≥ 1.8V Isource=150µA	0.8×Vcc	-	V_{CC}	
V_{OL}	Output Low Voltage	Vcc ≥ 4.5V Isink=3.2mA	-	-	0.4	V
		Vcc ≥ 2.7V Isink=1.2mA	-	-	0.3	
		Vcc ≥ 1.2V Isink=100µA	-	-	0.3	
V_{PFT}	PFI Input Threshold	V_{PFI} varies from 1.0V to 1.5V	1.23	1.25	1.27	V
		V_{PFI} varies from 0V to 1.0V	1.20	1.25	1.30	
I_{PFI}	PFI Input Current	PFI connected to Vcc	-	-	2.00	µA
		PFI connected to GND	-2.00	-	-	
I_{WDI}	Average WDI Input Current (**Note 3**)	WDI connected to V_{CC}	-	30	100	µA
		WDI connected to GND	-100	-30	-	
I_{MR}	$\overline{MR}$ input Current	$\overline{MR}$=0, Vcc = 5V	-600	-250	-100	µA

Note: 1. Parameters of room temperature guaranteed by production test and parameters of full-temperature guaranteed by design.
2. Valid for both $\overline{RESET}$ and RESET. V_{RST} is the Reset threshold voltage when V_{CC} from high to low level, V_{RN} is nominal reset threshold voltage.
3. WDI is internally serviced within the watchdog period if WDI is left unconnected.

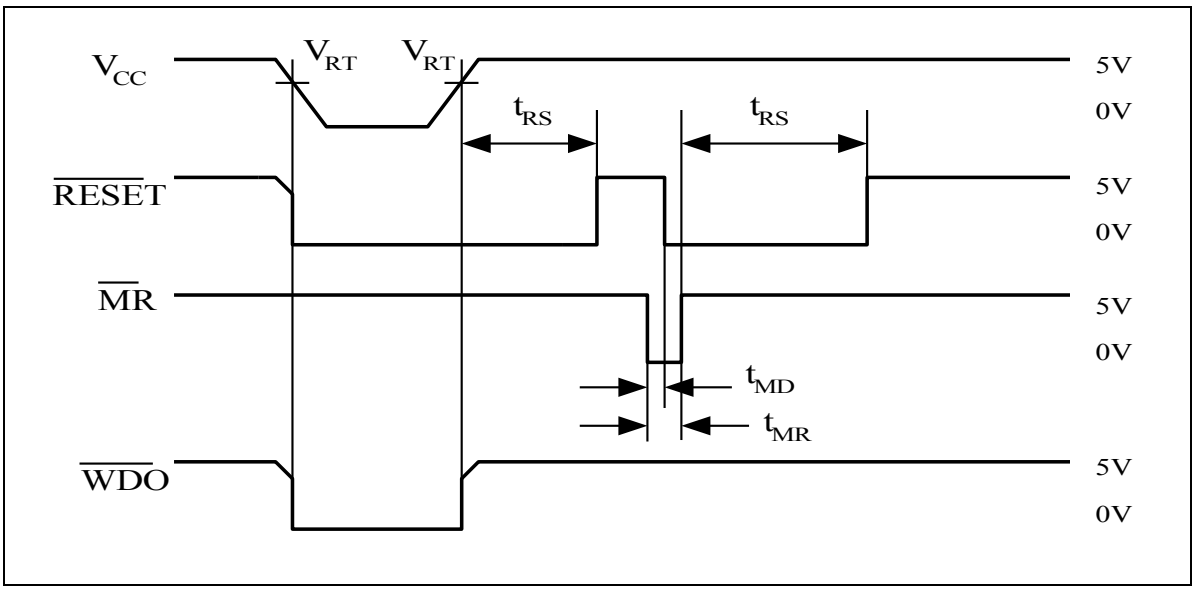
AC Electrical Characteristics

Symbol	Description	Test Conditions	Min.	Typ.	Max.	Unit
t_{RS}	Reset Pulse Width	$\overline{MR}$ from low to High.	160	200	280	ms
t_{WD}	Watchdog Timeout Period	WDI, $\overline{MR}$ tied to V_{CC}, V_{CC} >V_{RN}+5%.	1.2	1.6	2.25	s
t_{MR}	$\overline{MR}$ Pulse Width	-	200	-	-	ns
t_{MD}	$\overline{MR}$ to RESET Delay	V_{CC} =5V	-	-	250	ns
t_{WP}	WDI Pulse Width	-	150	-	-	ns

Watchdog Timing Diagram



Watchdog Timing Diagram



Functional Description

The PT75xx family can assert reset output during power-up, power-down and brownout conditions for µP system, detect power failure or low-battery conditions with a 1.25V threshold detector and have watchdog functions. Refer to Function Table of PT7A75xx Family for their individual features. The typical application see Figure 4.

Reset Output

The supervisory circuits can assert reset for a microprocessor during power-up, power-down and brownout to prevent code execution errors.

On power-up, once Vcc reaches about 1.2V, $\overline{\text{RESET}}$ is a guaranteed logic low of 0.4V or less. As Vcc rises, $\overline{\text{RESET}}$ stays low. When Vcc rises above the reset threshold, an internal timer releases $\overline{\text{RESET}}$ after about 200ms. $\overline{\text{RESET}}$ pulses low whenever Vcc drops below the reset threshold, i.e. brownout condition. If brownout occurs in the middle of a previously initiated reset pulse, the pulse continues for at least another 140ms. On power-down, once Vcc falls below the reset threshold, $\overline{\text{RESET}}$ stays low and is guaranteed to be 0.4V or less until Vcc drops below 1.0V.

The PT7A752x and PT7A753x active-high RESET output is simply the inverse of the $\overline{\text{RESET}}$ output, and is guaranteed to be valid with Vcc down to 1.2V. Some µPs, such as Intel's 80C51, require an active-high reset pulse.

Watchdog Timer

The watchdog circuit monitors the µP activity. If the µP does not toggle the watchdog input (WDI) within 1.6sec and WDI is not in high impedance, $\overline{\text{WDO}}$ goes low. As long as $\overline{\text{RESET}}$ is asserted or the WDI input is in high impedance, the watchdog timer will stay cleared and will not count. As soon as reset is released and WDI is driven high or low, the timer will start counting. Pulses as short as 50ns can be detected.

Typically, $\overline{\text{WDO}}$ will be connected to the non-maskable interrupt input (NMI) of a µP. When V_{CC} drops below the reset threshold, $\overline{\text{WDO}}$ will go low whether or not the watchdog timer has timed out yet. Normally this would trigger an NMI interrupt, but $\overline{\text{RESET}}$ goes low simultaneously, and thus overrides the NMI interrupt. If WDI is left unconnected, $\overline{\text{WDO}}$ can be used as a low-line output. Since floating WDI disables the internal timer, $\overline{\text{WDO}}$ goes low only when VCC falls below the reset threshold, thus functioning as a low-line output. Do not apply voltage level over V_{CC}.

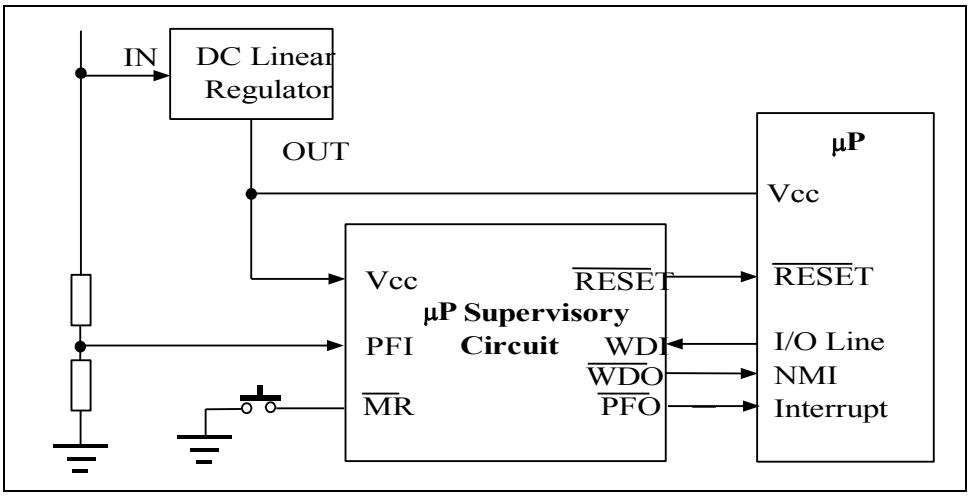
Manual Reset

The manual-reset input ($\overline{\text{MR}}$) allows reset to be triggered by a push button switch. The switch is effectively debounced by the 140ms minimum reset pulse width. $\overline{\text{MR}}$ is TTL/CMOS logic compatible, so it can be driven by any logic reset output. Do not apply voltage level over $V_{CC.}$

Power-Fail Comparator

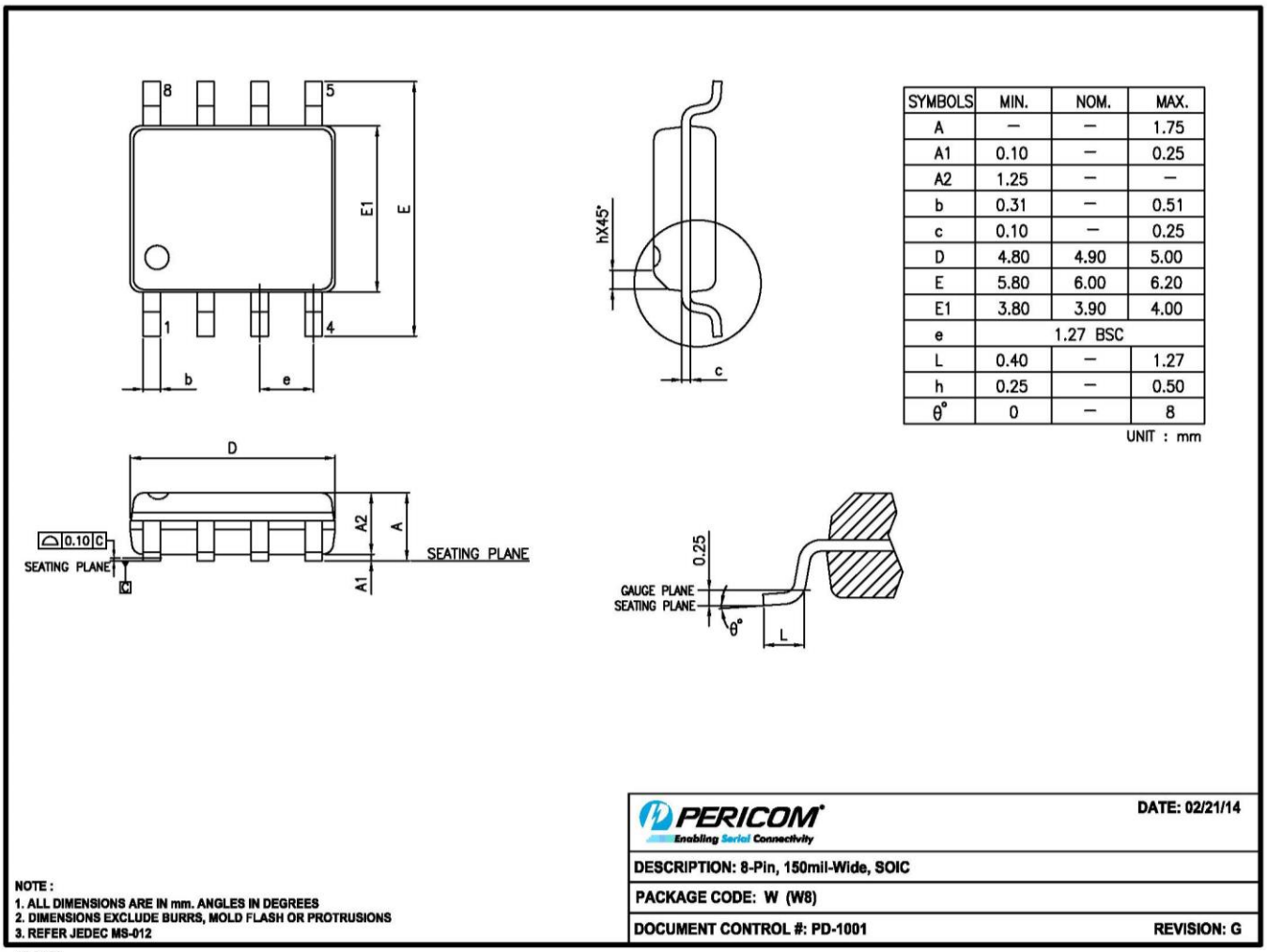
The power-fail comparator will send out a Low signal once detects a voltage lowered than 1.25V. It can be used for various purposes because its output and non-inverting input are not internally connected. The inverting input is internally connected to a 1.25V reference.

Typical Application Circuit



Mechanical Information

W (SOIC-8L)



SYMBOLS	MIN.	NOM.	MAX.
A	–	–	1.75
A1	0.10	–	0.25
A2	1.25	–	–
b	0.31	–	0.51
c	0.10	–	0.25
D	4.80	4.90	5.00
E	5.80	6.00	6.20
E1	3.80	3.90	4.00
e	1.27 BSC		
L	0.40	–	1.27
h	0.25	–	0.50
θ°	0	–	8

UNIT : mm

NOTE :
1. ALL DIMENSIONS ARE IN mm. ANGLES IN DEGREES
2. DIMENSIONS EXCLUDE BURRS, MOLD FLASH OR PROTRUSIONS
3. REFER JEDEC MS-012

PERICOM Enabling Serial Connectivity — DATE: 02/21/14

DESCRIPTION: 8-Pin, 150mil-Wide, SOIC

PACKAGE CODE: W (W8)

DOCUMENT CONTROL #: PD-1001 — REVISION: G

15-0103

For latest package info.
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Ordering Information

Part Number	Package Code	Package Description
PT7A751xWE	W	8-Pin, 150mil-Wide (SOIC)
PT7A752xWE	W	8-Pin, 150mil-Wide (SOIC)
PT7A753xWE	W	8-Pin, 150mil-Wide (SOIC)

Note:
- "x" refers to voltage range, see below ***Function Comparison Table***.
- E=Lead-free or Lead-free and Green
- Adding X suffix=Tape/Reel

Function Comparison Table

Part No.	Reset Threshold	Reset Active Low or High	Nom. Reset Time (ms), t_{RS}	Nom. Watch dog Time (sec), t_{WD}	Power Fail Comp.	Manual Reset Input
PT7A7511	4.63V	LOW	200	1.6	1.25V detector	Yes
PT7A7521	4.63V	HIGH	200	1.6	1.25V detector	Yes
PT7A7531	4.63V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7512	4.38V	LOW	200	1.6	1.25V detector	Yes
PT7A7522	4.38V	HIGH	200	1.6	1.25V detector	Yes
PT7A7532	4.38V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7513	3.08V	LOW	200	1.6	1.25V detector	Yes
PT7A7523	3.08V	HIGH	200	1.6	1.25V detector	Yes
PT7A7533	3.08V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7514	2.93V	LOW	200	1.6	1.25V detector	Yes
PT7A7524	2.93V	HIGH	200	1.6	1.25V detector	Yes
PT7A7534	2.93V	LOW, HIGH	200	unavailable	1.25V detector	Yes
PT7A7515	2.63V	LOW	200	1.6	1.25V detector	Yes
PT7A7525	2.63V	HIGH	200	1.6	1.25V detector	Yes
PT7A7535	2.63V	LOW, HIGH	200	unavailable	1.25V detector	Yes

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