THE DATASHEET OF

CSD15571Q2

20-V N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD15571Q2

FEATURES

- **Ultralow Q_g and Q_{gd}**
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- **SON 2-mm × 2-mm Plastic Package**

APPLICATIONS

- **Optimized for Load Switch Applications**
- **Storage, Tablets, and Handheld Devices**
- **Optimized for Control FET Applications**
- **Point of Load Synchronous Buck Converters**

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion and load management applications. The SON 2x2 offers excellent thermal performance for the size of the package.

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	20		V
Q_g	Gate Charge Total (4.5V)	2.5		nC
Q_{gd}	Gate Charge Gate to Drain	0.66		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V	16	mΩ
		V_{GS} = 10V	12	mΩ
$V_{GS(th)}$	Threshold Voltage	1.45		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD15571Q2	SON 2-mm × 2-mm Plastic Package	7-Inch Reel	3000	Tape and Reel

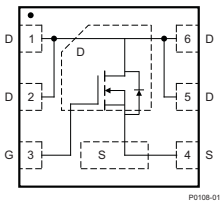
ABSOLUTE MAXIMUM RATINGS

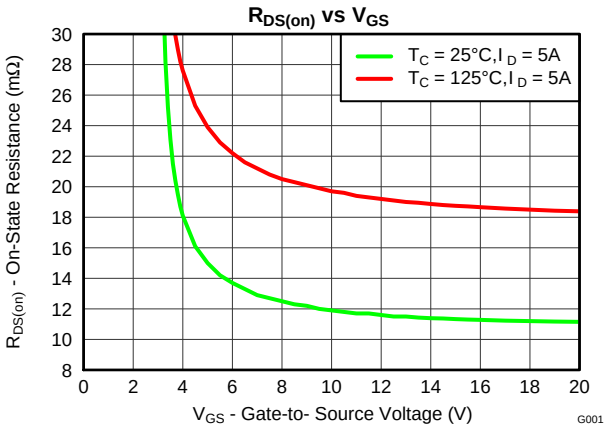
T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	20	V
V_{GS}	Gate to Source Voltage	±20	V
I_D	Continuous Drain Current (Package Limit)	22	A
	Continuous Drain Current(1)	10	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	52	A
P_D	Power Dissipation(1)	2.5	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 19A, L = 0.1mH, R_G = 25Ω	18	mJ

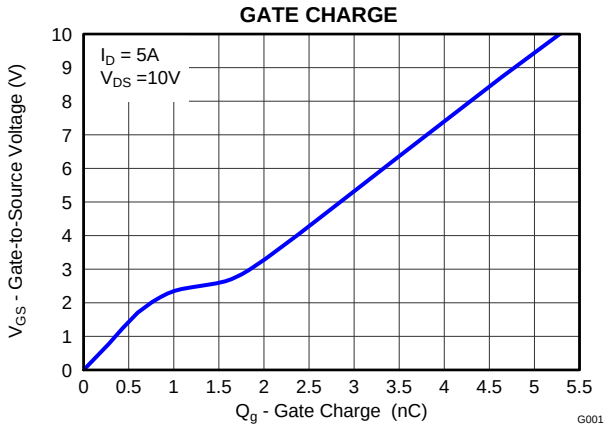
(1) $R_{\theta JA}$ = 50 on 1in² Cu (2 oz.) on .060" thick FR4 PCB.

(2) Pulse duration 10µs, duty cycle ≤2%

Top View







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NexFET is a trademark of Texas Instruments.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

T_A = 25°C, unless otherwise specified

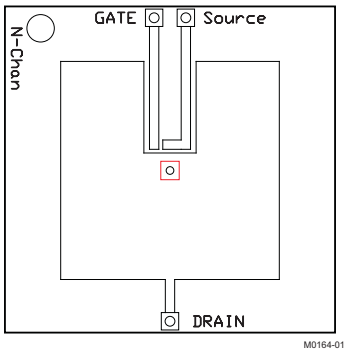
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250µA	20			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	µA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = 20V			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_{DS} = 250µA	1.10	1.45	1.90	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_{DS} = 5A		16.0	19.2	mΩ
		V_{GS} = 10V, I_{DS} = 5A		12.0	15.0	mΩ
g_{fs}	Transconductance	V_{DS} = 16V, I_{DS} = 5A		25		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 10V, f = 1MHz		320	419	pF
C_{OSS}	Output Capacitance			184	239	pF
C_{RSS}	Reverse Transfer Capacitance			32	42	pF
R_g	Series Gate Resistance			3.8	7.6	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 10V, I_{DS} = 5A		2.5	3.3	nC
Q_g	Gate Charge Total (10V)			5.1	6.7	nC
Q_{gd}	Gate Charge – Gate to Drain			0.66		nC
Q_{gs}	Gate Charge Gate to Source			0.93		nC
$Q_{g(th)}$	Gate Charge at Vth			0.52		nC
Q_{OSS}	Output Charge	V_{DS} = 10V, V_{GS} = 0V		4.1		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 10V, V_{GS} = 4.5V, I_{DS} = 5A, R_G = 2Ω		4.7		ns
t_r	Rise Time			17.2		ns
$t_{d(off)}$	Turn Off Delay Time			9.9		ns
t_f	Fall Time			4.1		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_{DS} = 5A, V_{GS} = 0V		0.82	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 10V, I_F = 5A, di/dt = 300A/µs		10.7		nC
t_{rr}	Reverse Recovery Time			19		ns

THERMAL CHARACTERISTICS

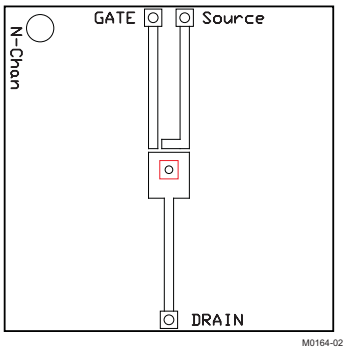
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			4.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1)(2)			65	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu pad on a 1.5-inch × 1.5-inch (3.81-cm × 3.81-cm), 0.06-inch (1.52-mm) thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 material with 1-inch^2 (6.45-cm^2), 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 65 when mounted on 1 inch^2 (6.45 cm^2) of 2-oz. (0.071-mm thick) Cu.



Max $R_{\theta JA}$ = 235 when mounted on minimum pad area of 2-oz. (0.071-mm thick) Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

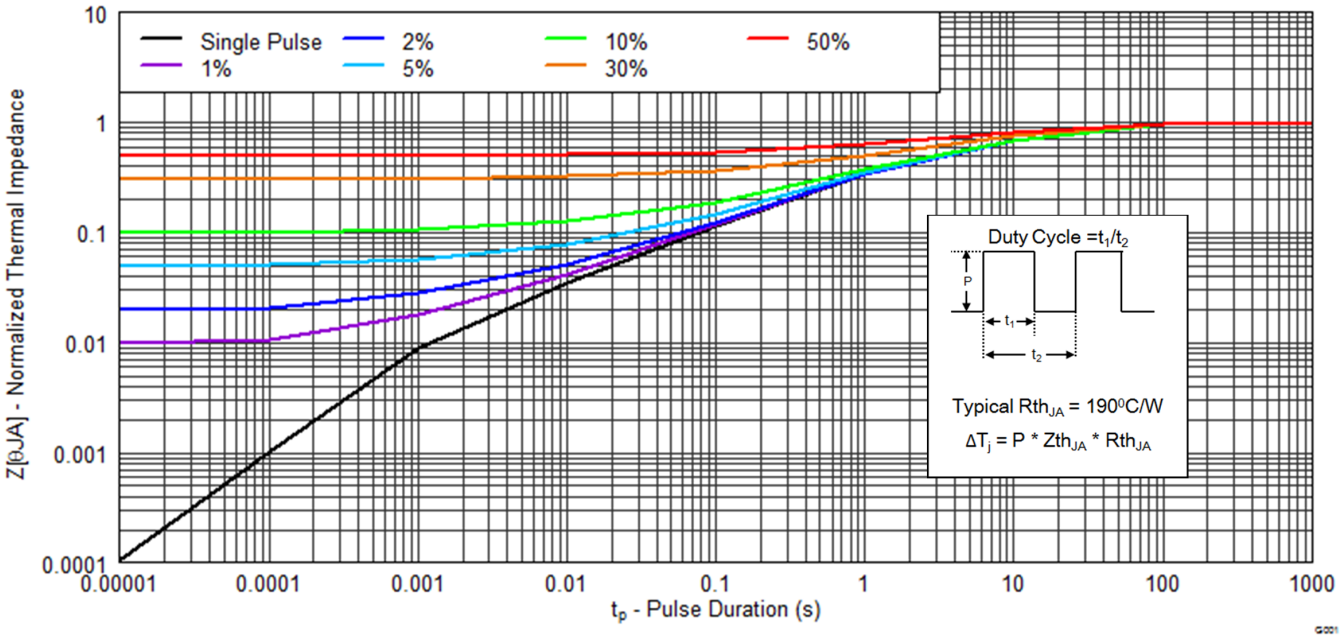


Figure 1. Transient Thermal Impedance

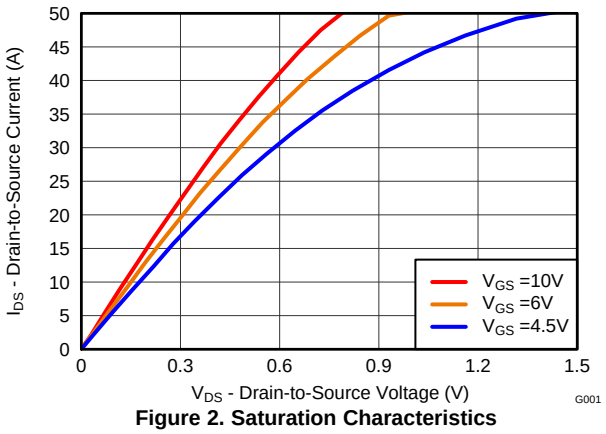


Figure 2. Saturation Characteristics

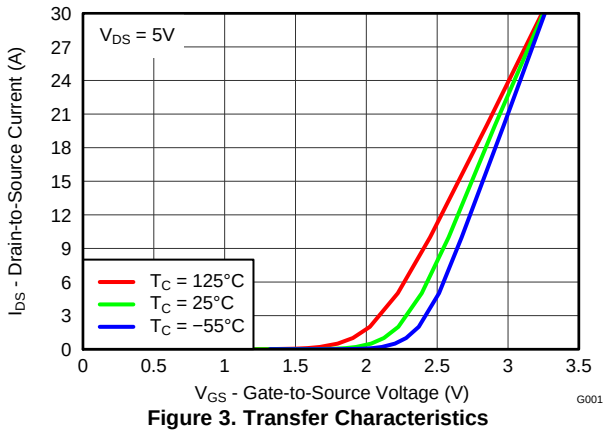


Figure 3. Transfer Characteristics

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

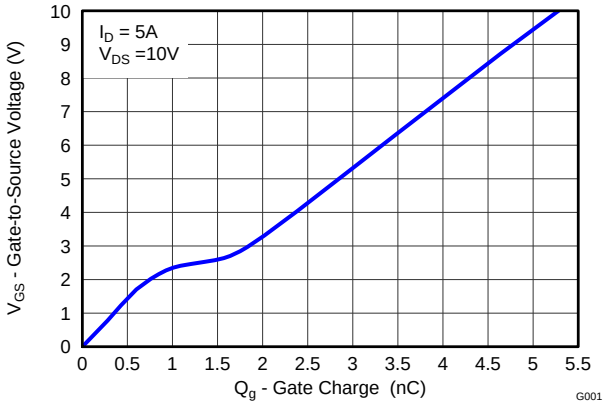


Figure 4. Gate Charge

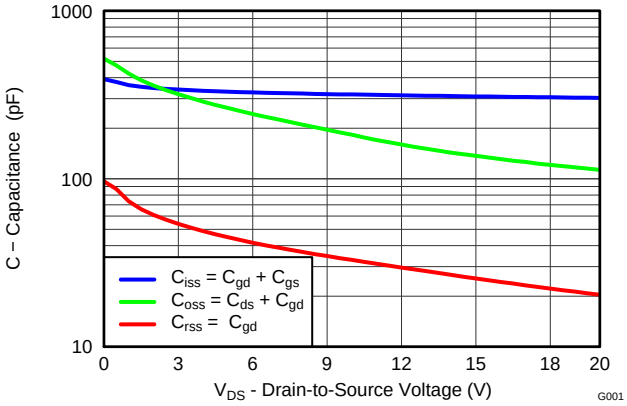


Figure 5. Capacitance

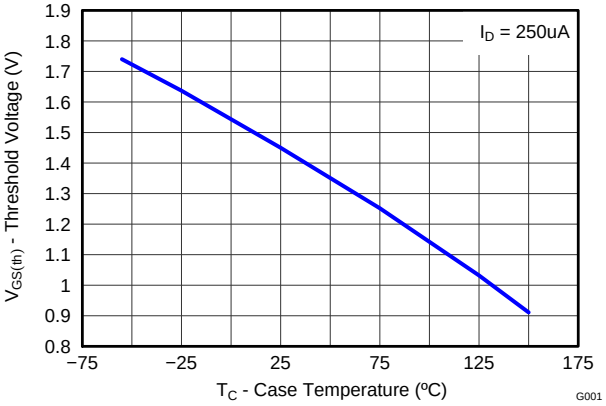


Figure 6. Threshold Voltage vs. Temperature

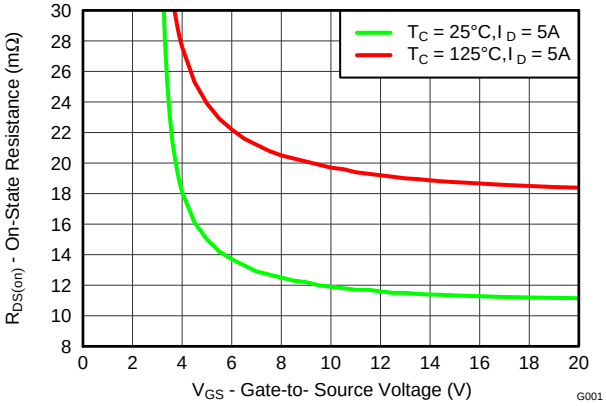


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

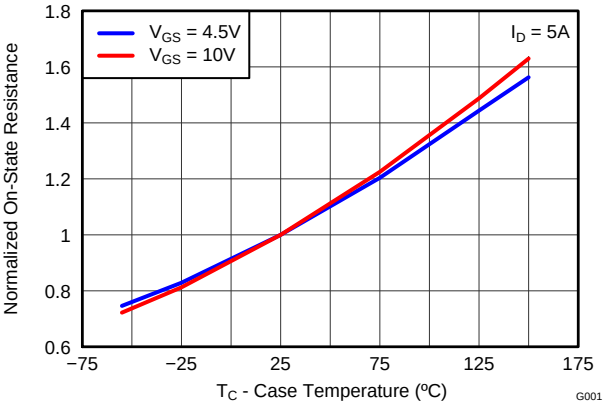


Figure 8. Normalized On-State Resistance vs. Temperature

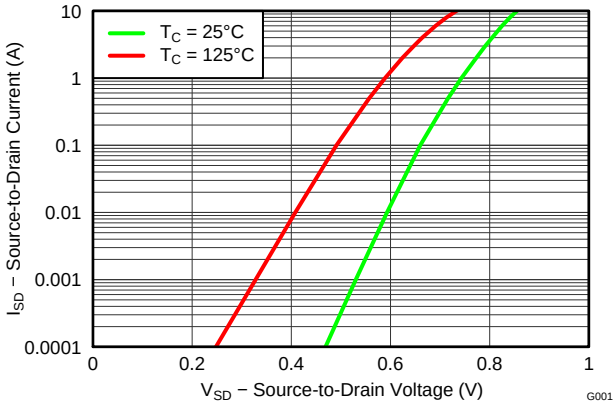


Figure 9. Typical Diode Forward Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

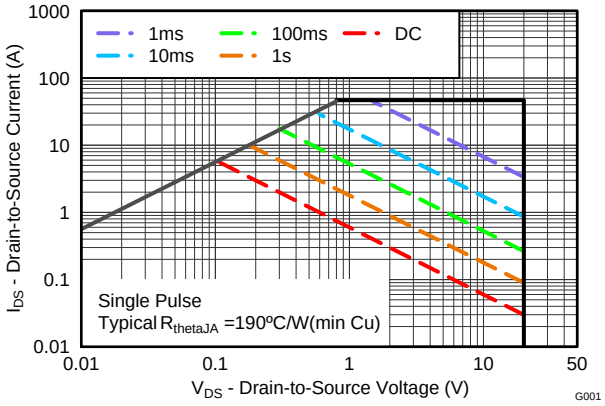


Figure 10. Maximum Safe Operating Area

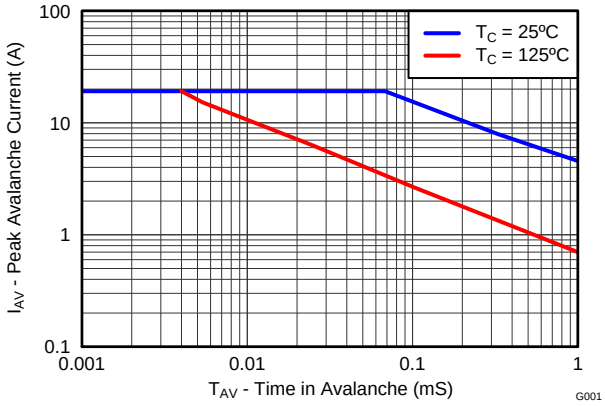


Figure 11. Single Pulse Unclamped Inductive Switching

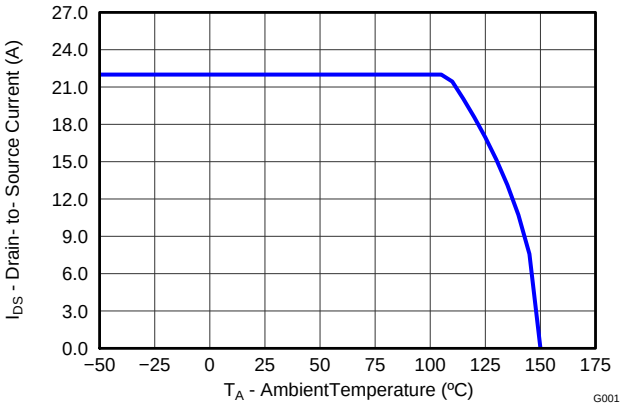
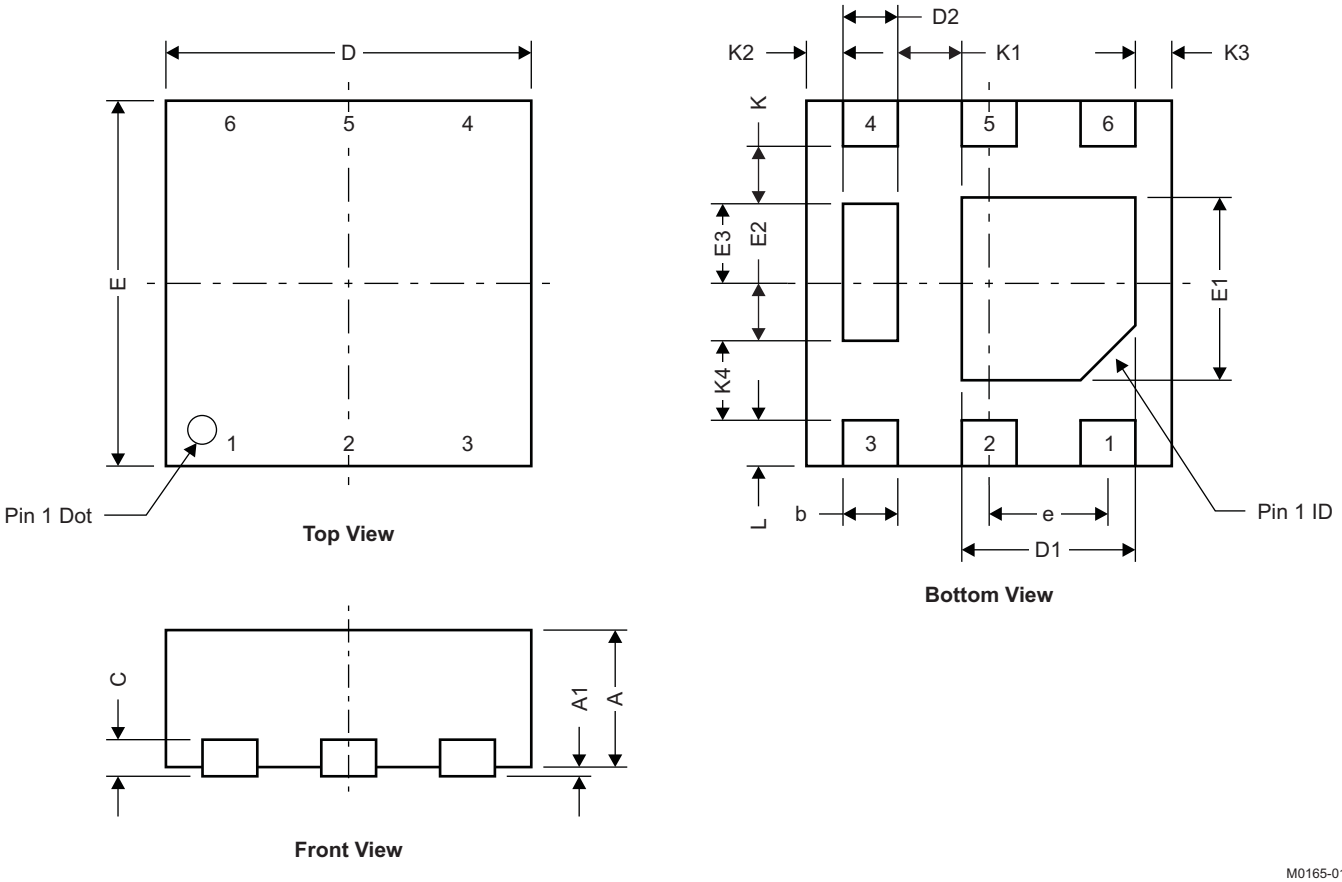


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

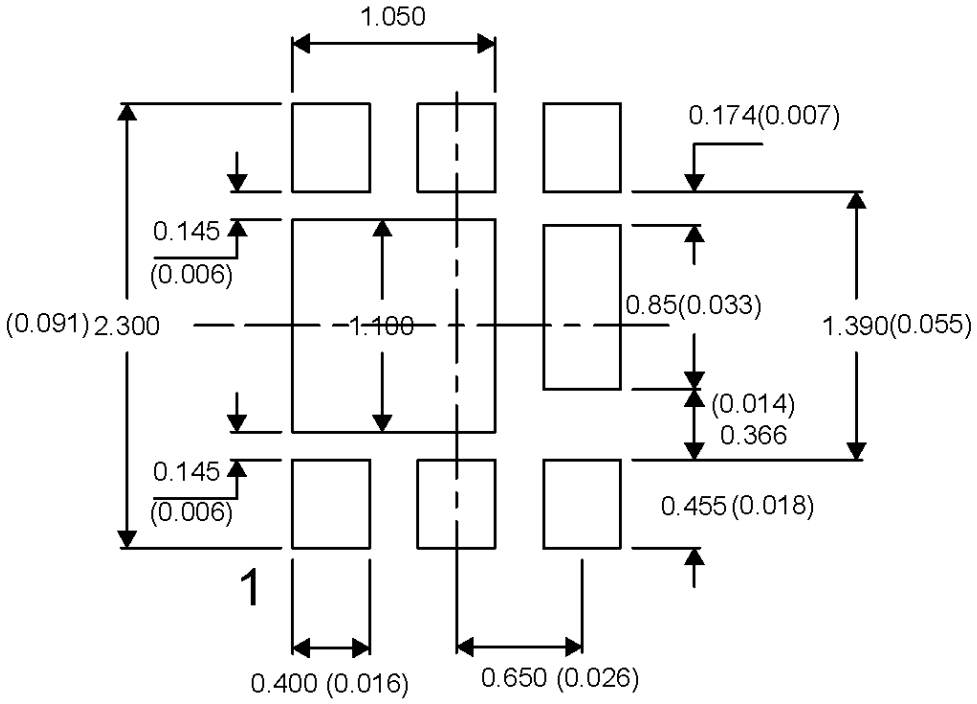
Q2 Package Dimensions



M0165-01

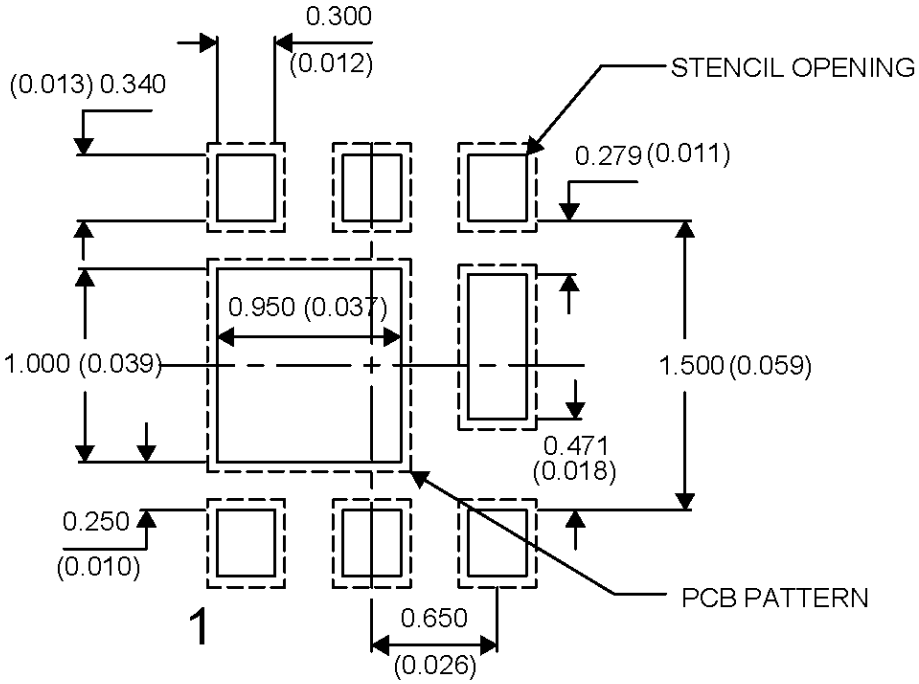
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.700	0.750	0.800	0.028	0.030	0.032
A1	0.000		0.050	0.000		0.002
b	0.250	0.300	0.350	0.010	0.012	0.014
C	0.203 TYP			0.008 TYP		
D	2.000 TYP			0.080 TYP		
D1	0.900	0.950	1.000	0.036	0.038	0.040
D2	0.300 TYP			0.012 TYP		
E	2.000 TYP			0.080 TYP		
E1	0.900	1.000	1.100	0.036	0.040	0.044
E2	0.280 TYP			0.0112 TYP		
E3	0.470 TYP			0.0188 TYP		
e	0.650 BSC			0.026 TYP		
K	0.280 TYP			0.0112 TYP		
K1	0.350 TYP			0.014 TYP		
K2	0.200 TYP			0.008 TYP		
K3	0.200 TYP			0.008 TYP		
K4	0.470 TYP			0.0188 TYP		
L	0.200	0.25	0.300	0.008	0.010	0.012

Recommended PCB Pattern



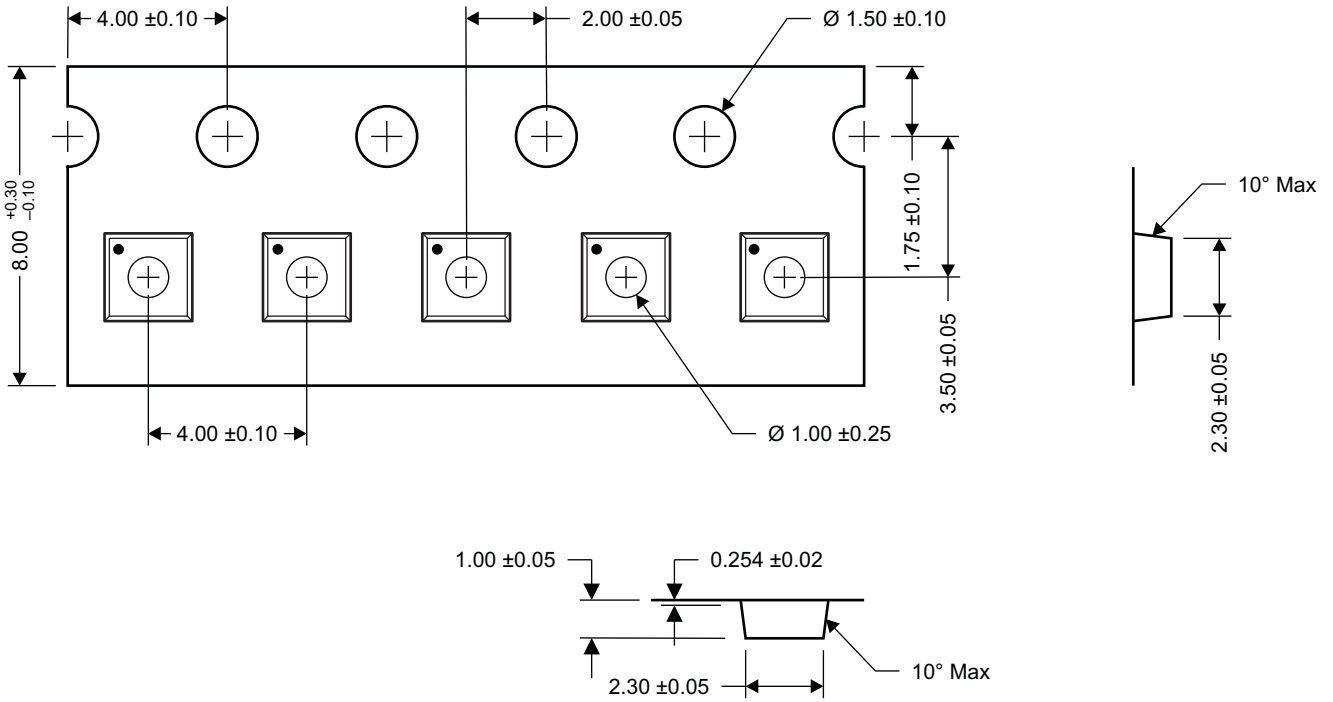
For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Recommended Stencil Pattern



Note: All dimensions are in mm, unless otherwise specified.

Q2 Tape and Reel Information



Notes: 1. Measured from centerline of sprocket hole to centerline of pocket
2. Cumulative tolerance of 10 sprocket holes is ±0.20
3. Other material available
4. Typical SR of form tape Max 10^9 OHM/SQ
5. All dimensions are in mm, unless otherwise specified.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
CSD15571Q2	ACTIVE	WSON	DQK	6	3000	Green (RoHS & no Sb/Br)	CU NIPDAU | CU SN	Level-1-260C-UNLIM	-55 to 150	1551	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".
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Green: TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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