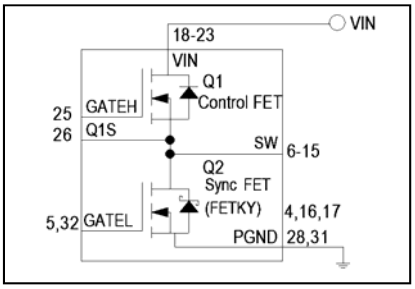
THE DATASHEET OF

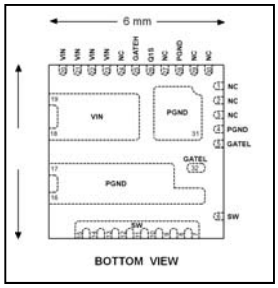
IRFHE4250DTRPBF

FASTIRFET™
IRFHE4250DPbF

HEXFET® Power MOSFET

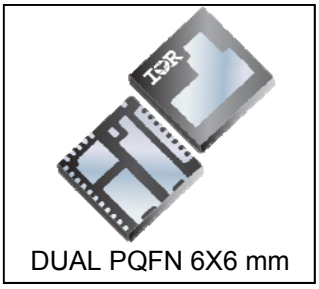
	Q1	Q2	
V_{DSS}	25	25	V
$R_{DS(on)}$ max (@V_{GS} = 4.5V)	4.10	1.35	mΩ
Qg (typical)	13	35	nC
I_D (@T_C = 25°C)	60⑦	60⑦	A





Applications

- Control and Synchronous MOSFETs for synchronous buck converters



DUAL PQFN 6X6 mm

Features		Benefits
Control and synchronous MOSFETs in one package		Increased power density
Low thermal resistance path to the PCB		Increased power density
Low thermal resistance path to the top		Increased power density
Low charge control MOSFET (13nC typical)	results in	Lower switching losses
Low R_{DSON} synchronous MOSFET (<1.35mΩ)	⇒	Lower conduction losses
Intrinsic schottky diode with low forward voltage on Q2		Lower switching losses
RoHS compliant, halogen-free		Environmentally friendlier
MSL2, industrial qualification		Increased reliability

Base part number	Package Type	Standard Pack		Orderable Part Number
		Form	Quantity	
IRFHE4250DPbF	Dual PQFN 6mm x 6mm	Tape and Reel	4000	IRFHE4250DTRPbF

Absolute Maximum Ratings

	Parameter	Q1 Max.	Q2 Max.	Units
V_{GS}	Gate-to-Source Voltage	± 16		V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	86⑥⑦	303⑥⑦	A
I_D @ T_C = 70°C	Continuous Drain Current, V_{GS} @ 10V	69⑥⑦	243⑥⑦	
I_D @ T_C = 25°C	Continuous Drain Current (Source Bonding Technology Limited)	60⑦	60⑦	
I_{DM}	Pulsed Drain Current	180	525⑧	
P_D @T_C = 25°C	Power Dissipation	156	156	W
P_D @T_C = 70°C	Power Dissipation	100	100	
	Linear Derating Factor	1.3	1.3	W/°C
T_J T_{STG}	Operating Junction and Storage Temperature Range	-55 to + 150		°C

Thermal Resistance

	Parameter	Q1 Max.	Q2 Max.	Units
$R_{\theta JC}$ (Bottom)	Junction-to-Case ④	3.7	0.91	°C/W
$R_{\theta JC}$ (Top)	Junction-to-Case ④	0.91	2.1	
$R_{\theta JA}$	Junction-to-Ambient ⑤	24	24	
$R_{\theta JA}$ (<10s)	Junction-to-Ambient ⑤	17	17	

Notes ① through ⑧ are on page 12

Static @ T_J = 25°C (unless otherwise specified)

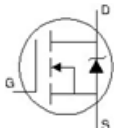
	Parameter		Min.	Typ.	Max.	Units	Conditions
BV_{DSS}	Drain-to-Source Breakdown Voltage	Q1	25	—	—	V	V_{GS} = 0V, I_D = 250µA
		Q2	25	—	—		V_{GS} = 0V, I_D = 1.0mA
$\Delta BV_{DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	Q1	—	23	—	mV/°C	Reference to 25°C, I_D = 1.0mA
		Q2	—	21	—		Reference to 25°C, I_D = 10mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	Q1	—	2.20	2.75	mΩ	V_{GS} = 10V, I_D = 27A ③
		Q2	—	0.70	0.90		V_{GS} = 10V, I_D = 27A ③
		Q1	—	3.20	4.10		V_{GS} = 4.5V, I_D = 27A ③
		Q2	—	1.00	1.35		V_{GS} = 4.5V, I_D = 27A ③
$V_{GS(th)}$	Gate Threshold Voltage	Q1	1.1	1.6	2.1	V	Q1: V_{DS} = V_{GS}, I_D = 35µA
		Q2	1.1	1.6	2.1		Q2: V_{DS} = V_{GS}, I_D = 100µA
$\Delta V_{GS(th)}/\Delta T_J$	Gate Threshold Voltage Coefficient	Q1	—	-5.8	—	mV/°C	Q1: V_{DS} = V_{GS}, I_D = 35µA
		Q2	—	-7.8	—		Q2: V_{DS} = V_{GS}, I_D = 1.0mA
I_{DSS}	Drain-to-Source Leakage Current	Q1	—	—	1.0	µA	V_{DS} = 20V, V_{GS} = 0V
		Q2	—	—	500		V_{DS} = 20V, V_{GS} = 0V
I_{GSS}	Gate-to-Source Forward Leakage	Q1/Q2	—	—	100	nA	V_{GS} = 16V
	Gate-to-Source Reverse Leakage	Q1/Q2	—	—	-100		V_{GS} = -16V
gfs	Forward Transconductance	Q1	73	—	—	S	V_{DS} = 10V, I_D = 14A
		Q2	121	—	—		V_{DS} = 10V, I_D = 23A
Q_g	Total Gate Charge	Q1	—	13	20		
		Q2	—	35	53		
Q_{gs1}	Pre-Vth Gate-to-Source Charge	Q1	—	3.6	—		Q1
		Q2	—	8.6	—		V_{DS} = 13V
Q_{gs2}	Post-Vth Gate-to-Source Charge	Q1	—	1.3	—		V_{GS} = 4.5V, I_D = 13A
		Q2	—	3.8	—	nC	
Q_{gd}	Gate-to-Drain Charge	Q1	—	5.2	—		Q2
		Q2	—	13	—		V_{DS} = 13V
Q_{godr}	Gate Charge Overdrive	Q1	—	2.9	—		V_{GS} = 4.5V, I_D = 23A
		Q2	—	9.6	—		
Q_{sw}	Switch Charge (Q_{gs2} + Q_{gd})	Q1	—	6.5	—		
		Q2	—	16.8	—		
Q_{oss}	Output Charge	Q1	—	14	—	nC	V_{DS} = 16V, V_{GS} = 0V
		Q2	—	41	—		
R_G	Gate Resistance	Q1	—	0.5	—	Ω	
		Q2	—	0.4	—		
$t_{d(on)}$	Turn-On Delay Time	Q1	—	11	—		Q1
		Q2	—	17	—		V_{DS} = 13V V_{GS} = 4.5V
t_r	Rise Time	Q1	—	33	—		I_D = 14A, Rg = 1.8Ω
		Q2	—	54	—	ns	
$t_{d(off)}$	Turn-Off Delay Time	Q1	—	14	—		Q2
		Q2	—	24	—		V_{DS} = 13V V_{GS} = 4.5V
t_f	Fall Time	Q1	—	12	—		I_D = 23A, Rg = 1.8Ω
		Q2	—	16	—		
C_{iss}	Input Capacitance	Q1	—	1735	—		
		Q2	—	4765	—		V_{GS} = 0V
C_{oss}	Output Capacitance	Q1	—	493	—	pF	V_{DS} = 13V
		Q2	—	1577	—		f = 1.0MHz
C_{rss}	Reverse Transfer Capacitance	Q1	—	137	—		
		Q2	—	370	—		

Avalanche Characteristics

	Parameter	Typ.	Q1 Max.	Q2 Max.	Units
E_{AS}	Single Pulse Avalanche Energy ②	—	71②	481②	mJ
I_{AR}	Avalanche Current ①	—	32	63	A

Diode Characteristics

	Parameter		Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current	Q1	—	—	60⑦	A	MOSFET symbol
	(Body Diode)	Q2	—	—	60⑦		showing the
I_{SM}	Pulsed Source Current	Q1	—	—	180	A	integral reverse
	(Body Diode)	Q2	—	—	525⑧		p-n junction diode.
V_{SD}	Diode Forward Voltage	Q1	—	0.77	0.88	V	T_J = 25°C, I_S = 14A, V_{GS} = 0V③
		Q2	—	0.60	0.75		T_J = 25°C, I_S = 27A, V_{GS} = 0V③
t_{rr}	Reverse Recovery Time	Q1	—	19	29	ns	Q1 T_J = 25°C, I_F = 30A
		Q2	—	34	51		V_{DD} = 13V, di/dt = 200A/µs ③
Q_{rr}	Reverse Recovery Charge	Q1	—	16	24	nC	Q2 T_J = 25°C, I_F = 30A
		Q2	—	54	81		V_{DD} = 13V, di/dt = 200A/µs ③



Q1 - Control FET

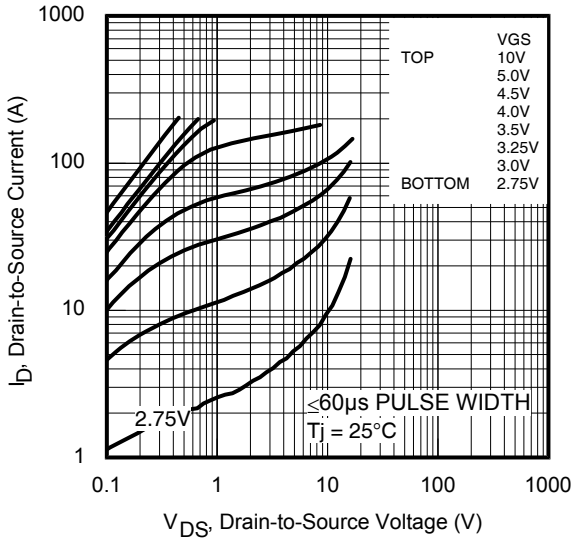


Fig 1. Typical Output Characteristics

Q2 - Synchronous FET

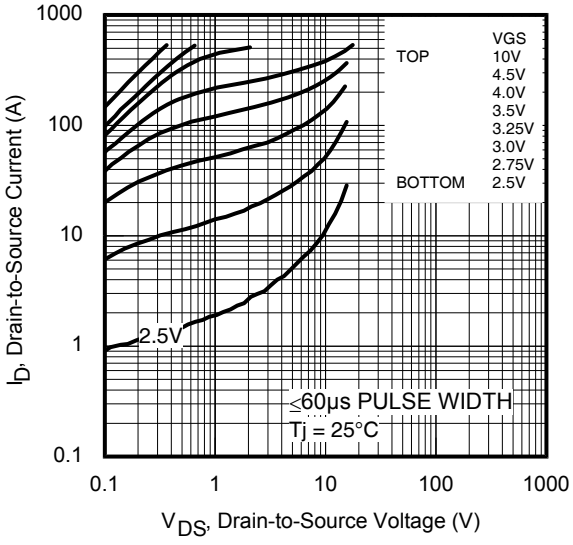


Fig 2. Typical Output Characteristics

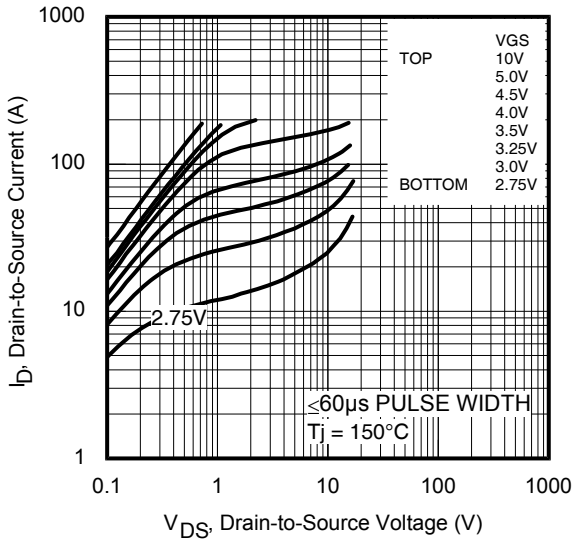


Fig 3. Typical Output Characteristics

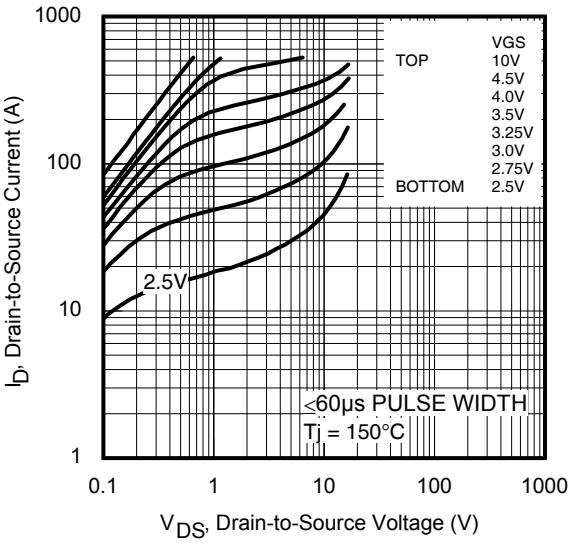


Fig 4. Typical Output Characteristics

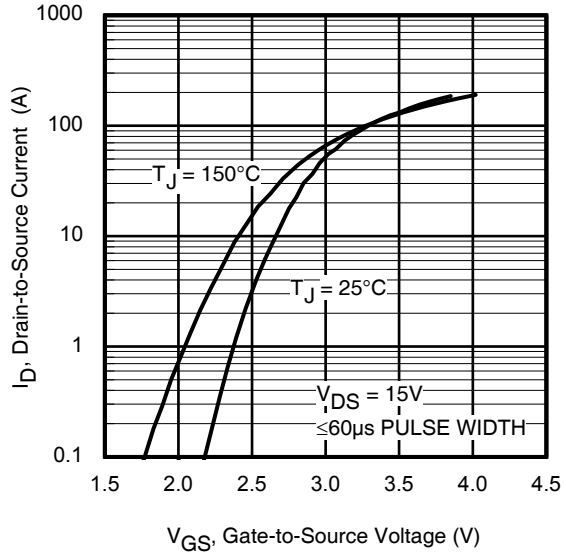


Fig 5. Typical Transfer Characteristics

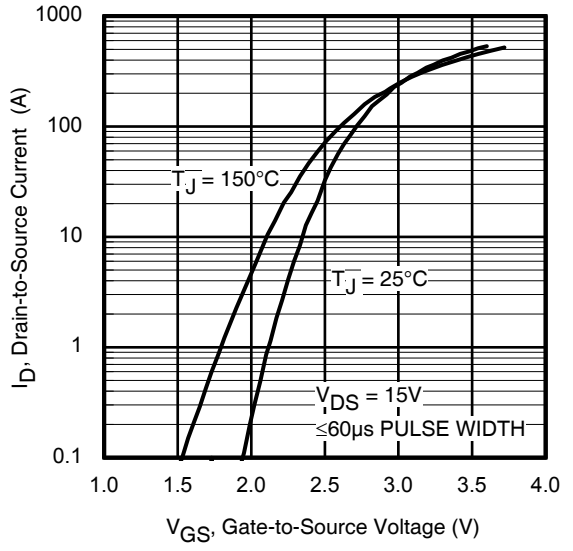


Fig 6. Typical Transfer Characteristics

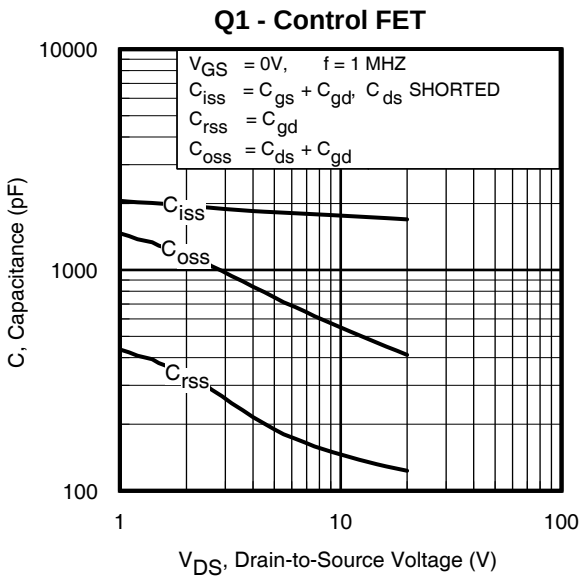


Fig 7. Typical Capacitance vs. Drain-to-Source Voltage

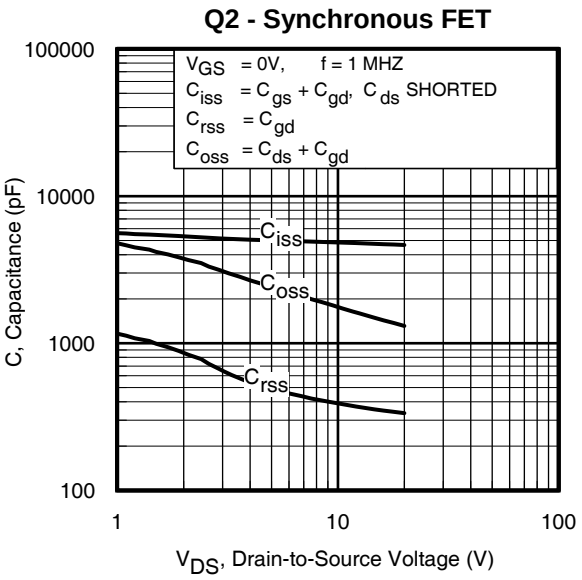


Fig 8. Typical Capacitance vs. Drain-to-Source Voltage

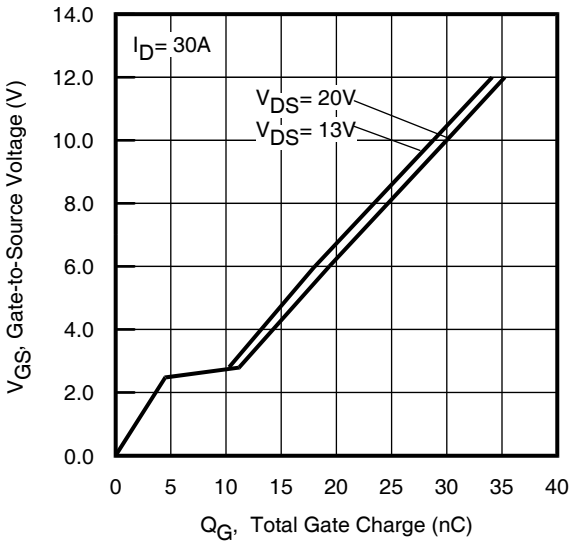


Fig 9. Typical Gate Charge vs. Gate-to-Source Voltage

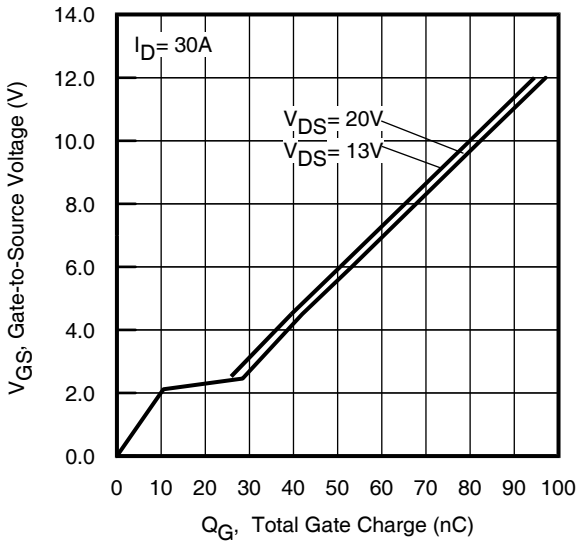


Fig 10. Typical Gate Charge vs. Gate-to-Source Voltage

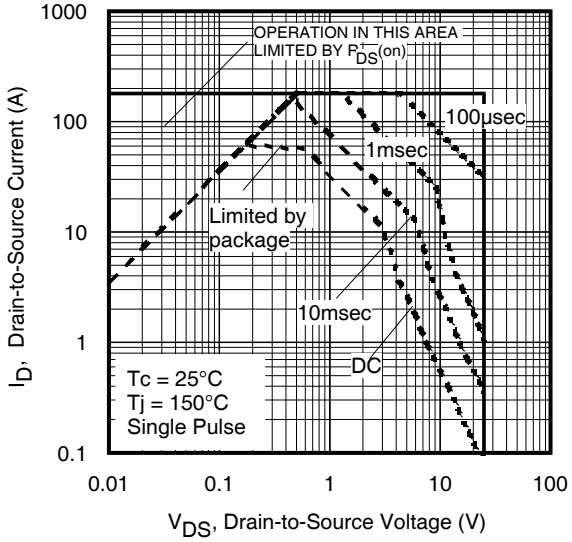


Fig 11. Maximum Safe Operating Area

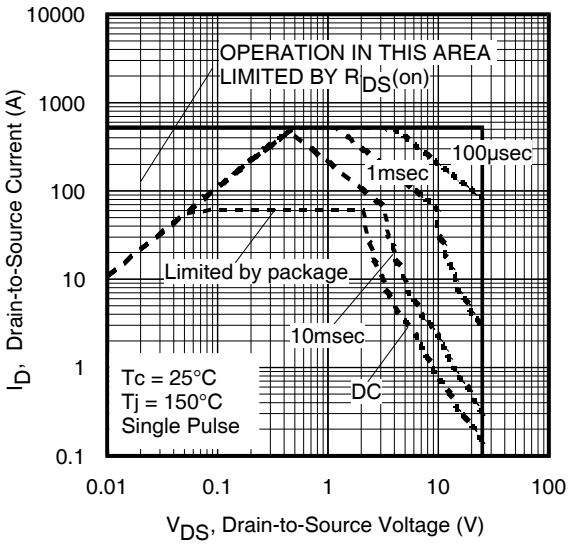


Fig 12. Maximum Safe Operating Area

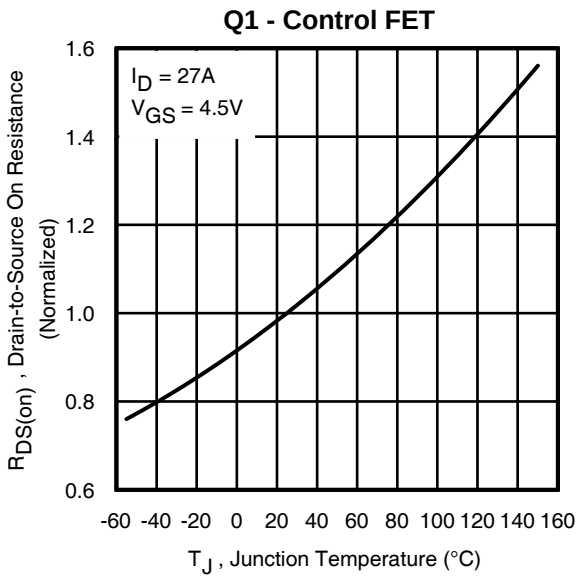


Fig 13. Normalized On-Resistance vs. Temperature

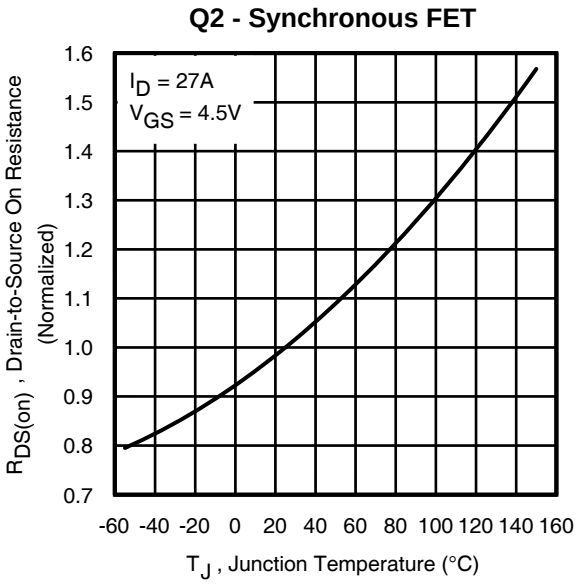


Fig 14. Normalized On-Resistance vs. Temperature

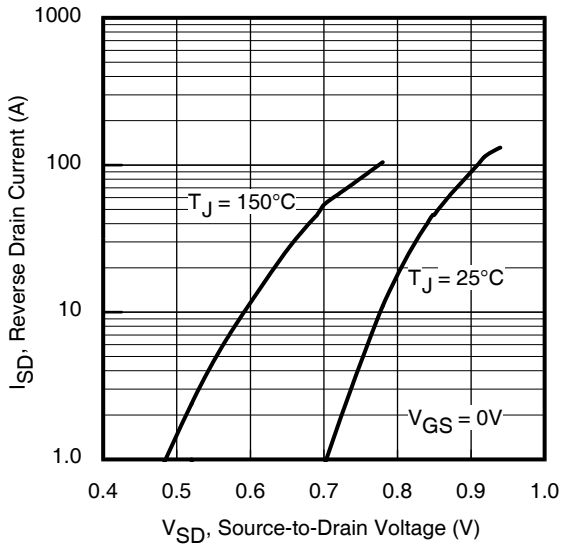


Fig 15. Typical Source-Drain Diode Forward Voltage

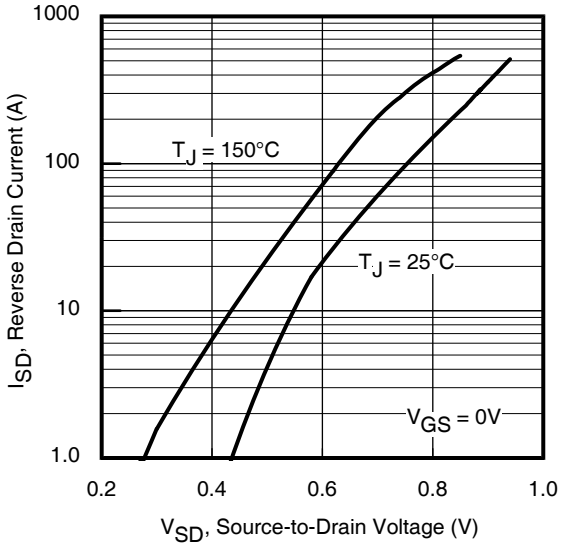


Fig 16. Typical Source-Drain Diode Forward Voltage

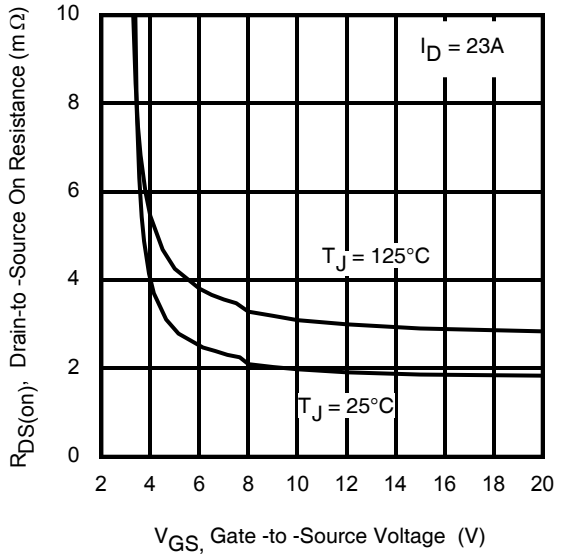


Fig 17. Typical On-Resistance vs. Gate Voltage

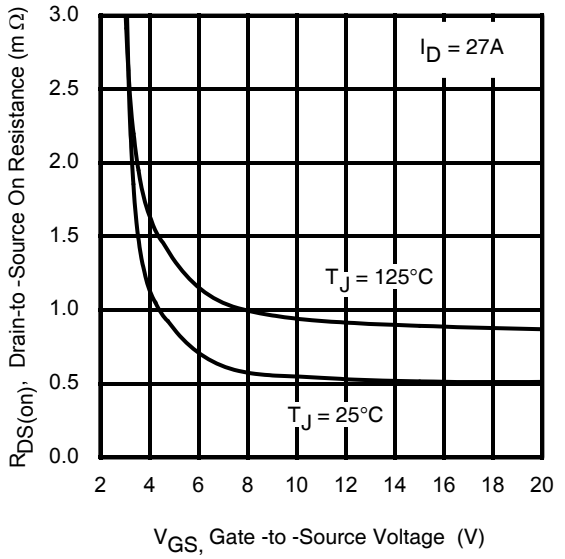


Fig 18. Typical On-Resistance vs. Gate Voltage

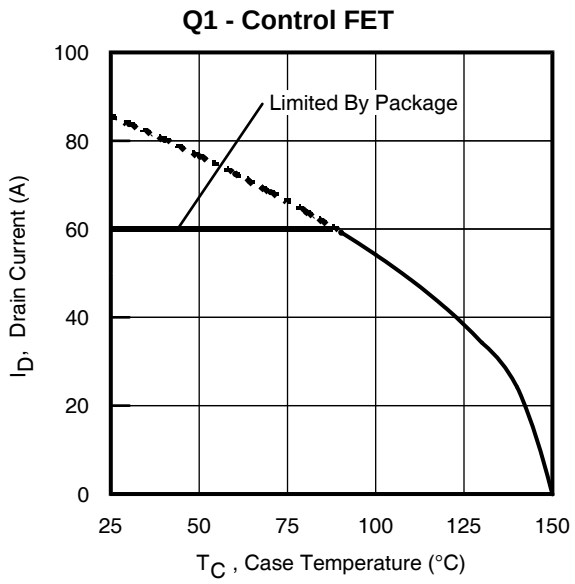


Fig 19. Maximum Drain Current vs. Case Temperature

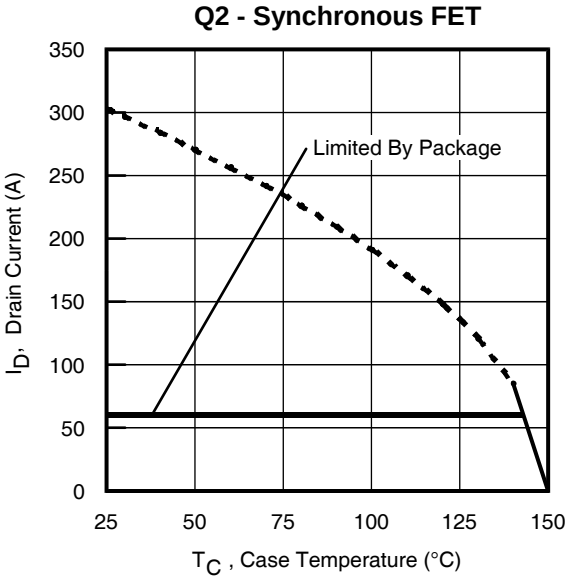


Fig 20. Maximum Drain Current vs. Case Temperature

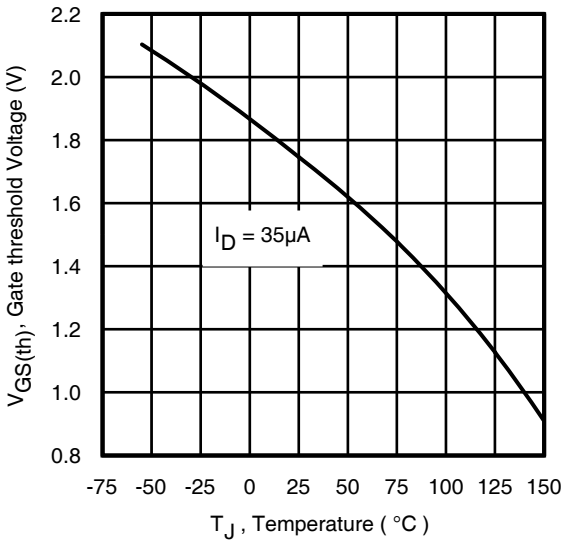


Fig 21. Threshold Voltage vs. Temperature

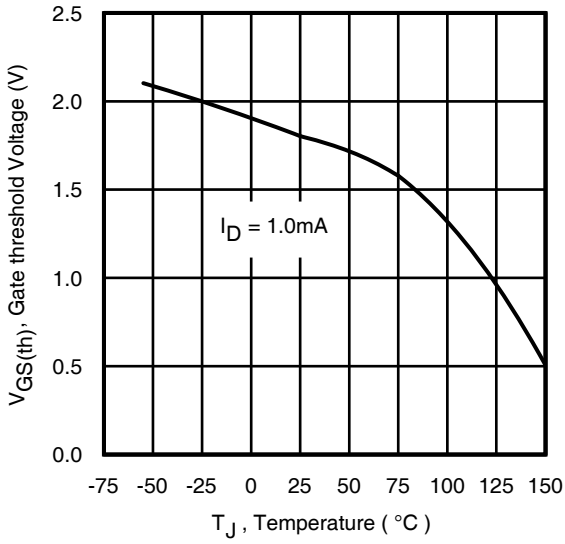


Fig 22. Threshold Voltage vs. Temperature

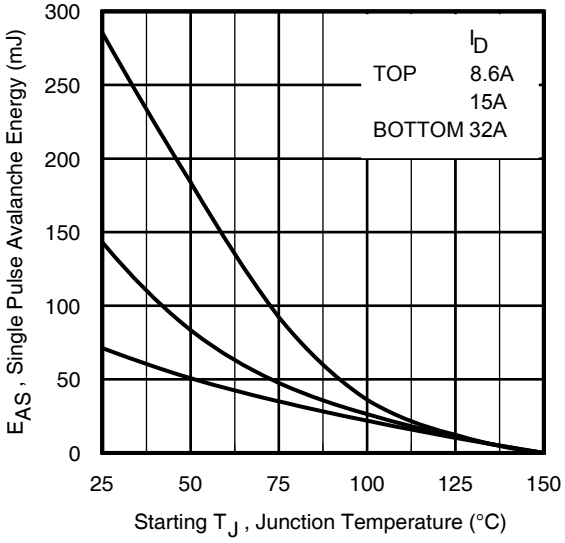


Fig 23. Maximum Avalanche Energy vs. Drain Current

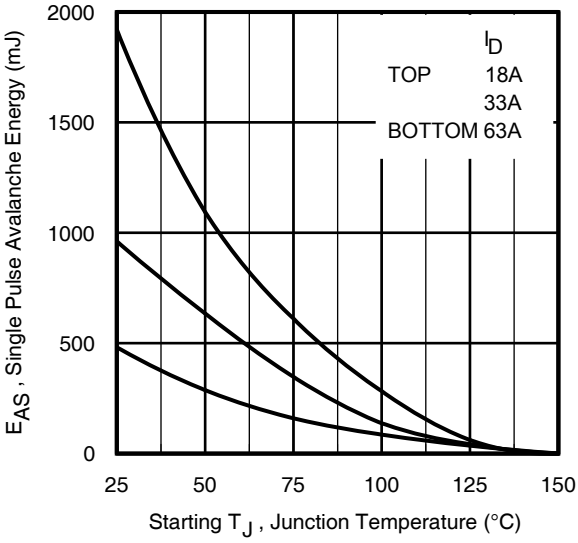


Fig 24. Maximum Avalanche Energy vs. Drain Current

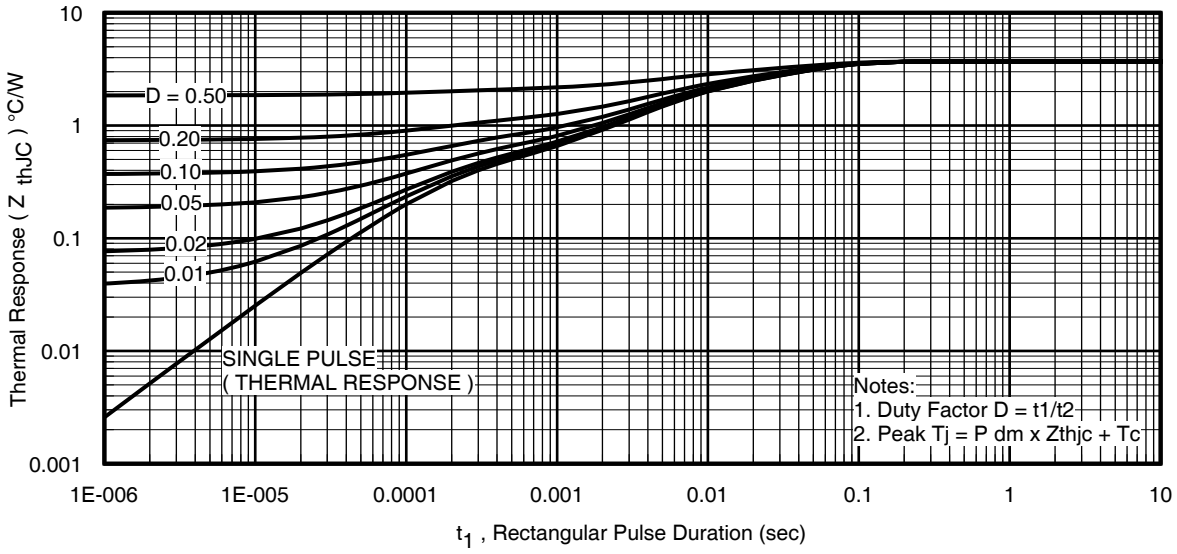


Fig 25. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q1)

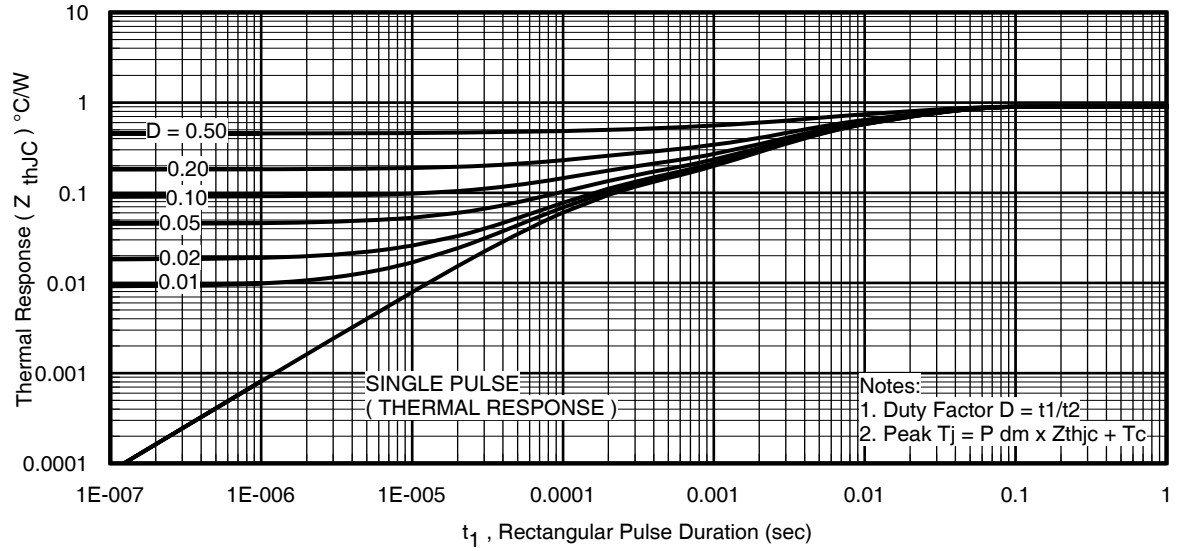


Fig 26. Maximum Effective Transient Thermal Impedance, Junction-to-Case (Q2)

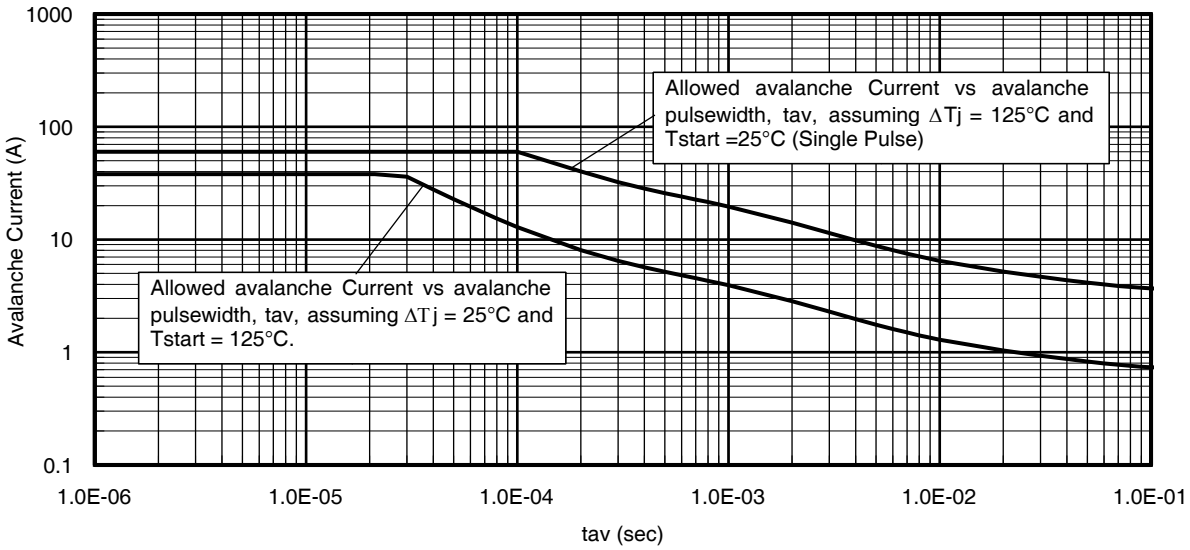


Fig 27. Single Avalanche Event: Pulse Current vs. Pulse Width (Q1)

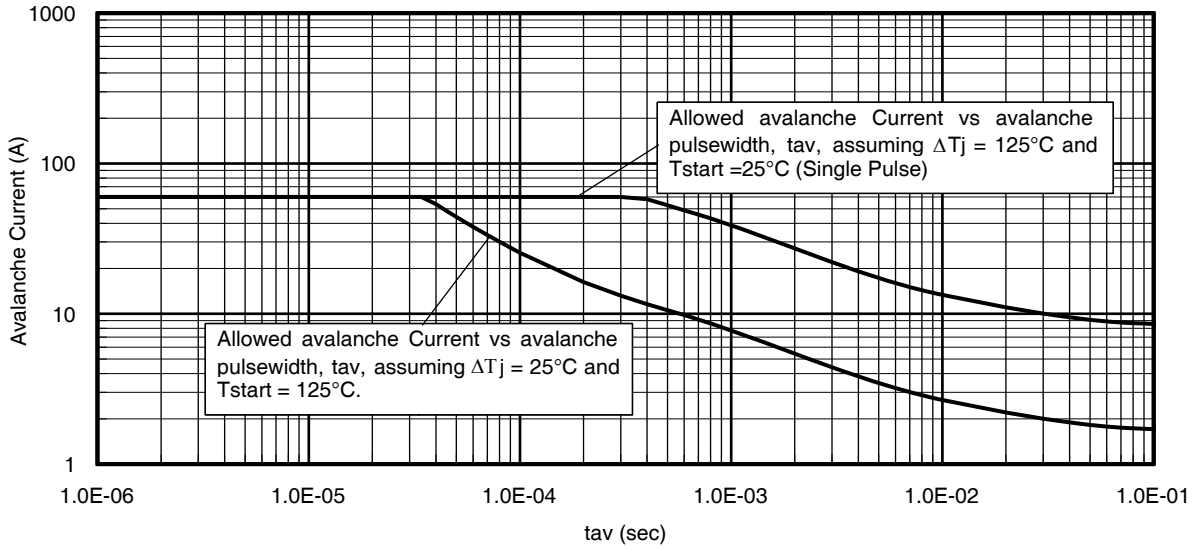


Fig 28. Single Avalanche Event: Pulse Current vs. Pulse Width (Q2)

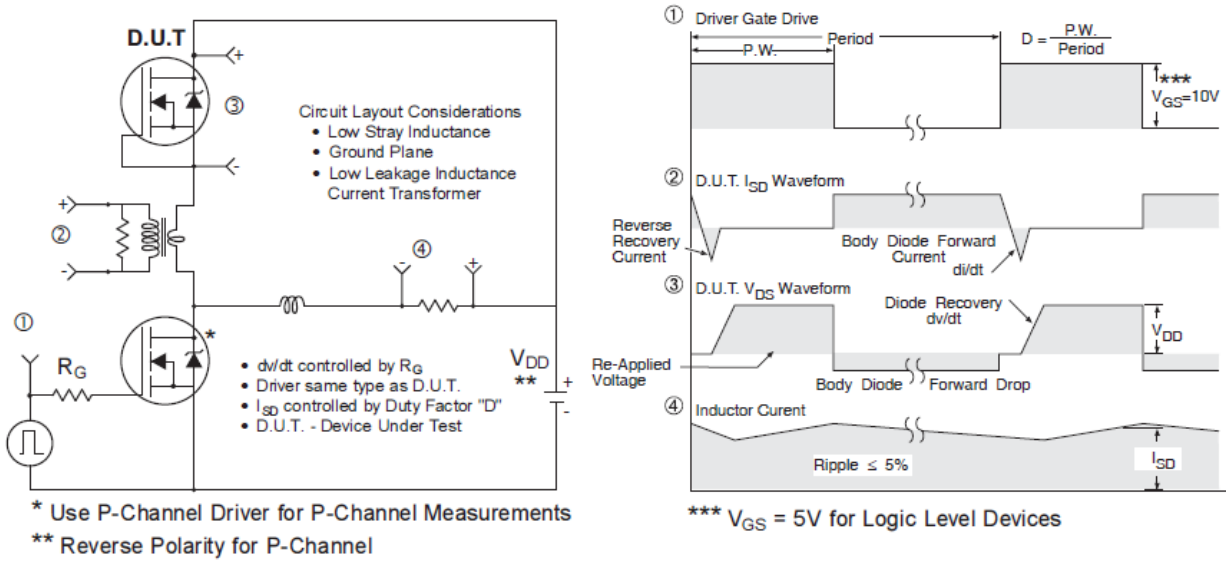


Fig 29. Peak Diode Recovery dv/dt Test Circuit for N-Channel HEXFET® Power MOSFETs

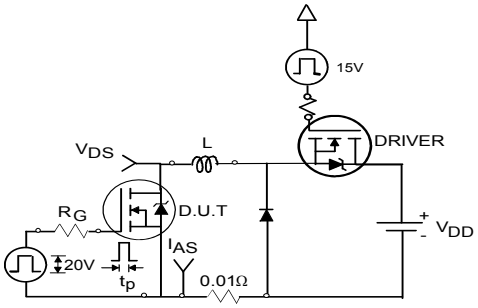


Fig 30a. Unclamped Inductive Test Circuit

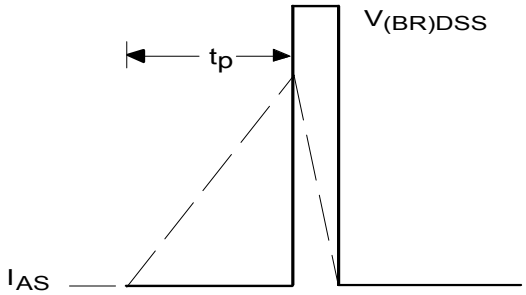


Fig 30b. Unclamped Inductive Waveforms

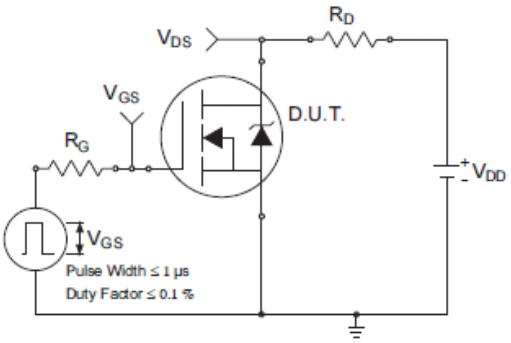


Fig 31a. Switching Time Test Circuit

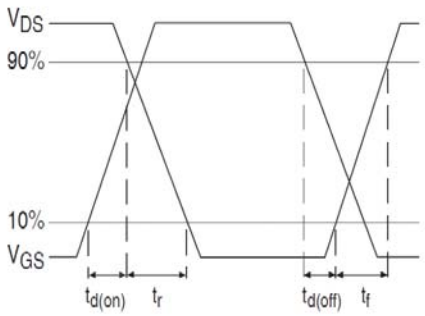


Fig 31b. Switching Time Waveforms

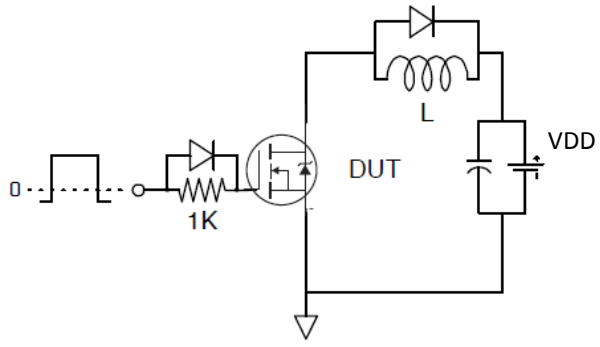


Fig 32a. Gate Charge Test Circuit

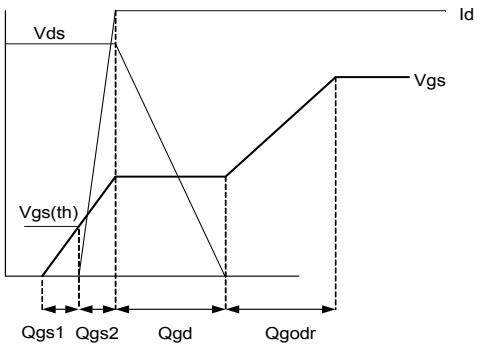
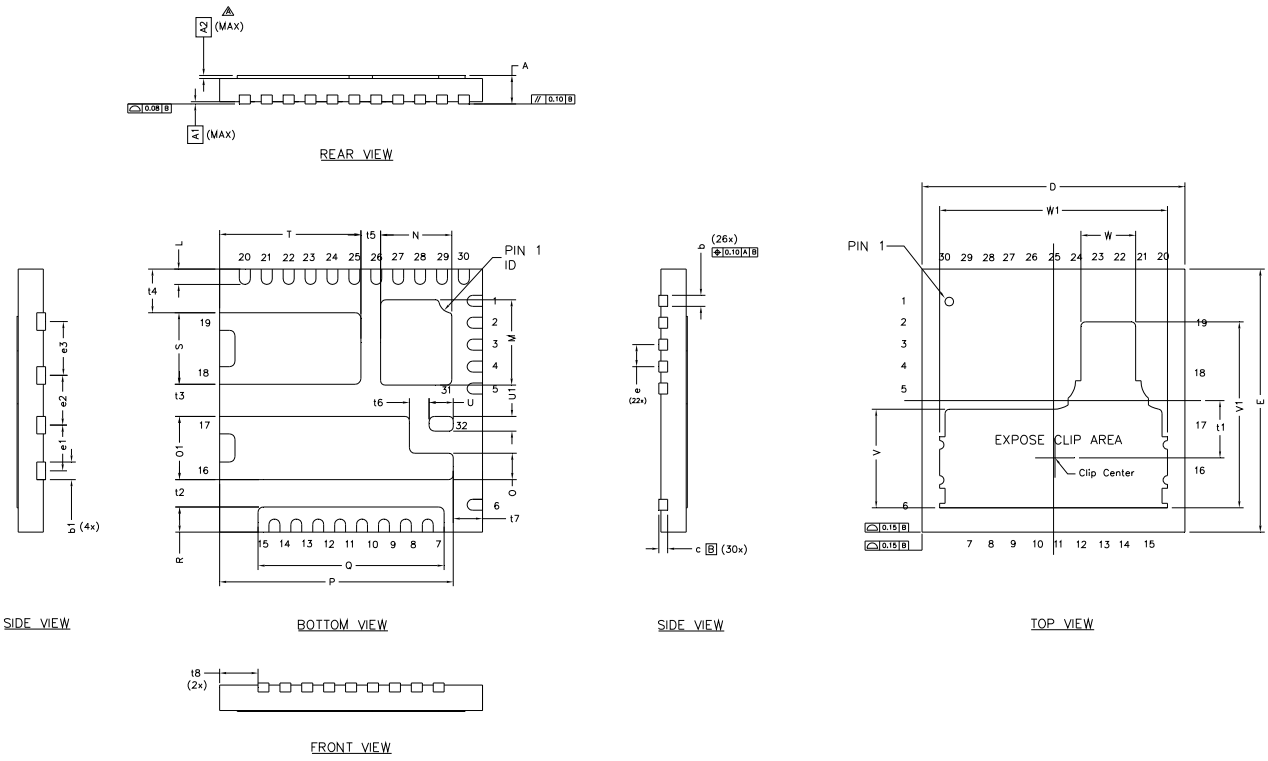


Fig 32b. Gate Charge Waveform

Dual PQFN 6x6 Outline Package Details



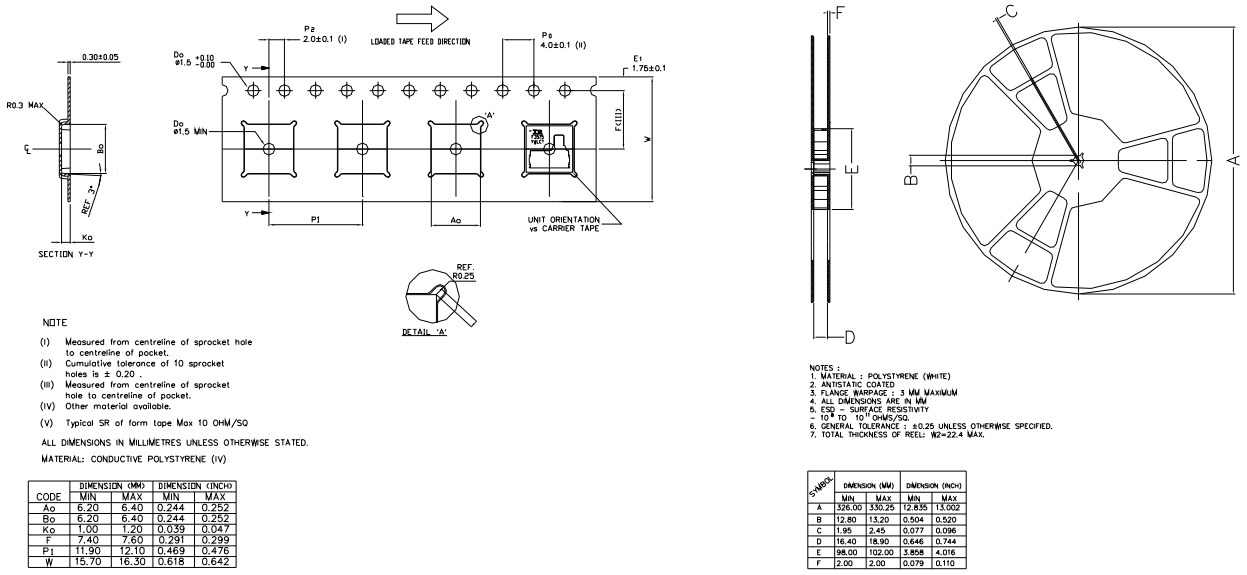
DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	0.55	0.75	.0217	.0295
A1	0.000	0.050	.0000	.0020
A2	0.000	0.070	.0000	.0028
b	0.20	0.30	.0079	.0118
b1	0.350	0.450	.0138	.0177
c	0.203 REF.		.0080 REF.	
D	6.000 BASIC		.2362 BASIC	
E	6.000 BASIC		.2362 BASIC	
e	0.500 BASIC		.0197 BASIC	
e1	1.041 BASIC		.0410 BASIC	
e2	1.134 BASIC		.0446 BASIC	
e3	1.230 BASIC		.0484 BASIC	
L	0.300	0.400	.0118	.0157
M	1.846	2.046	.0727	.0806
N	1.527	1.727	.0601	.0680
O	0.500	0.700	.0197	.0276
O1	1.341	1.541	.0528	.0607
P	5.231	5.431	.2059	.2138

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
Q	4.150	4.350	.1634	.1713
R	0.475	0.675	.0187	.0266
S	1.530	1.730	.0602	.0681
T	3.123	3.323	.1230	.1308
t1	1.207	1.407	.0475	.0554
t2	0.525	0.725	.0207	.0285
t3	0.634	0.834	.0250	.0328
t4	0.896	1.096	.0353	.0431
t5	0.350	0.550	.0138	.0217
t6	0.350	0.550	.0138	.0217
t7	0.569	0.769	.0224	.0303
t8	0.775	0.975	.0305	.0384
U	0.450	0.650	.0177	.0256
U1	0.237	0.437	.0093	.0172
V	2.147	2.347	.0845	.0924
V1	4.140	4.340	.1630	.1709
W	1.148	1.348	.0452	.0531
W1	5.100	5.300	.0200	.0208

For more information on board mounting, including footprint and stencil recommendation, please refer to application note AN-1136: http://www.irf.com/technical-info/appnotes/an-1136.pdf
For more information on package inspection techniques, please refer to application note AN-1154: http://www.irf.com/technical-info/appnotes/an-1154.pdf

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Dual PQFN 6x6 Outline Tape and Reel



CODE	DIMENSION (MM) MIN	MAX	DIMENSION (INCH) MIN	MAX
Ao	6.20	6.40	0.244	0.252
Bo	6.20	6.40	0.244	0.252
Ko	1.00	1.20	0.039	0.047
F	7.40	7.60	0.291	0.299
P1	11.90	12.10	0.469	0.476
W	15.70	16.30	0.618	0.642

SYMBOL	DIMENSION (MM) MIN	MAX	DIMENSION (INCH) MIN	MAX
A	326.00	330.25	12.835	13.002
B	12.80	13.20	0.504	0.520
C	1.95	2.45	0.077	0.096
D	16.40	18.90	0.646	0.744
E	98.00	102.00	3.858	4.016
F	2.00	2.00	0.079	0.110

Note: For the most current drawing please refer to IR website at http://www.irf.com/package/

Qualification Information†

Qualification level	Industrial (per JEDEC JESD47F †† guidelines)	
Moisture Sensitivity Level	DUAL PQFN 6mm x 6mm	MSL2 (per JEDEC J-STD-020D††)
RoHS Compliant	Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/product-info/reliability

†† Applicable version of JEDEC standard at the time of product release.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting T_J = 25°C,
Q1: L = 0.14 mH, R_G = 50Ω, I_{AS} = 32A;
Q2: L = 0.24 mH, R_G = 50Ω, I_{AS} = 63A.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ R_θ is measured at T_J approximately 90°C.

⑤ When mounted on 1 inch square PCB (FR-4). Please refer to AN-994 for more details:
http://www.irf.com/technical-info/appnotes/an-994.pdf

⑥ Calculated continuous current based on maximum allowable junction temperature.

⑦ Current is limited to Q1 = 60A & Q2 = 60A by source bonding technology.

⑧ Pulsed drain current is limited to 240A by source bonding technology.

International IOR Rectifier

IR WORLD HEADQUARTERS: 101 N. Sepulveda Blvd., El Segundo, California 90245, USA
To contact International Rectifier, please visit http://www.irf.com/whoto-call/

Looking for pricing, stock, or lifecycle information?

Click below to explore more details on WIN SOURCE:

- View IRFHE4250DTRPBF on WIN SOURCE
- Infineon Technologies Information

Optimize Your Supply Chain with WIN SOURCE Solutions

- Global Sourcing Solution
- Obsolete Management
- Cost Control Management
- Shortage Management
- Alternative Solution
- Excess Inventory Management