

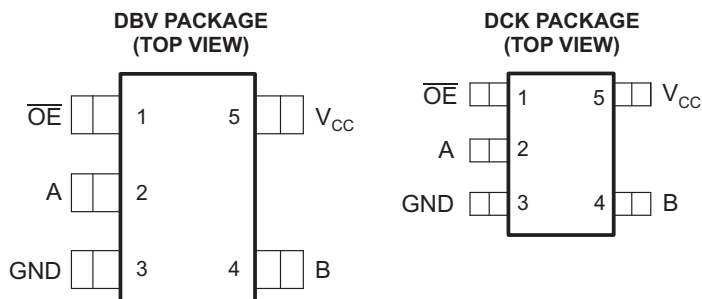


**THE DATASHEET OF  
74CBTLV1G125DCKRG4**



## FEATURES

- 5-Ω Switch Connection Between Two Ports
- Rail-to-Rail Switching on Data I/O Ports
- $I_{off}$  Supports Partial-Power-Down Mode Operation



See mechanical drawings for dimensions.

## DESCRIPTION/ORDERING INFORMATION

The SN74CBTLV1G125 features a single high-speed line switch. The switch is disabled when the output-enable ( $\overline{OE}$ ) input is high.

This device is fully specified for partial-power-down applications using  $I_{off}$ . The  $I_{off}$  feature ensures that damaging current will not backflow through the device when it is powered down. The device has isolation during power off.

To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

## ORDERING INFORMATION

| $T_A$         | PACKAGE <sup>(1)</sup> |              | ORDERABLE PART NUMBER | TOP-SIDE MARKING <sup>(2)</sup> |
|---------------|------------------------|--------------|-----------------------|---------------------------------|
| -40°C to 85°C | SOT (SOT-23) – DBV     | Reel of 3000 | SN74CBTLV1G125DBVR    | V25_                            |
|               | SOT (SC-70) – DCK      | Reel of 3000 | SN74CBTLV1G125DCKR    | VM_                             |

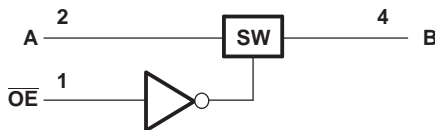
(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at [www.ti.com/sc/package](http://www.ti.com/sc/package).

(2) The actual top-side marking has one additional character that designates the assembly/test site.

## FUNCTION TABLE

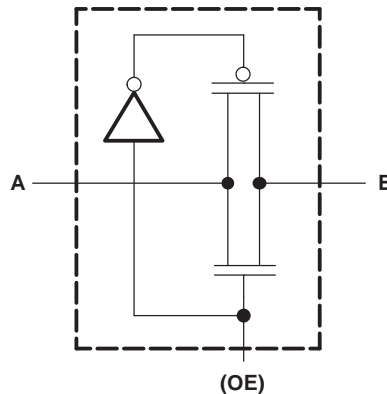
| INPUT $\overline{OE}$ | FUNCTION        |
|-----------------------|-----------------|
| L                     | A port = B port |
| H                     | Disconnect      |

## LOGIC DIAGRAM (POSITIVE LOGIC)



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SIMPLIFIED SCHEMATIC, EACH FET SWITCH



**Absolute Maximum Ratings<sup>(1)</sup>**

over operating free-air temperature range (unless otherwise noted)

|               |  | MIN           | MAX | UNIT |      |
|---------------|--|---------------|-----|------|------|
| $V_{CC}$      | Supply voltage range                     | -0.5          | 4.6 | V    |      |
| $V_I$         | Input voltage range <sup>(2)</sup>       | -0.5          | 4.6 | V    |      |
|               | Continuous channel current               |               | 128 | V    |      |
| $I_{IK}$      | Input clamp current                      | $V_{I/O} < 0$ |     | -50  | mA   |
| $\theta_{JA}$ | Package thermal impedance <sup>(3)</sup> | DBV package   |     | 206  | °C/W |
|               |  | DCK package   |     | 252  |      |
| $T_{stg}$     | Storage temperature range                | -65           | 150 | °C   |      |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) The package thermal impedance is calculated in accordance with JESD 51-7.

**Recommended Operating Conditions<sup>(1)</sup>**

|          |                                  | MIN                                     | MAX | UNIT |   |
|----------|----------------------------------|---|-----|------|---|
| $V_{CC}$ | Supply voltage                   | 2.3                                     | 3.6 | V    |   |
| $V_{IH}$ | High-level control input voltage | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ |     | 1.7  | V |
|          |                                  | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ |     | 2    |   |
| $V_{IL}$ | Low-level control input voltage  | $V_{CC} = 2.3\text{ V to }2.7\text{ V}$ |     | 0.7  | V |
|          |                                  | $V_{CC} = 2.7\text{ V to }3.6\text{ V}$ |     | 0.8  |   |
| $T_A$    | Operating free-air temperature   | -40                                     | 85  | °C   |   |

- (1) All unused control inputs of the device must be held at  $V_{CC}$  or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

## Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER                      |   | TEST CONDITIONS   |                      | MIN | TYP <sup>(1)</sup> | MAX      | UNIT          |
|--------------------------------|---|---|----------------------|-----|--------------------|----------|---------------|
| $V_{IK}$                       |   | $V_{CC} = 3\text{ V}$ , $I_I = -18\text{ mA}$   |                      |     |                    | -1.2     | V             |
| $I_I$                          |   | $V_{CC} = 3.6\text{ V}$ , $V_I = V_{CC}$ or GND                                       |                      |     |                    | $\pm 1$  | $\mu\text{A}$ |
| $I_{off}$                      |   | $V_{CC} = 0$ , $V_I$ or $V_O = 0$ to $3.6\text{ V}$                                   |                      |     |                    | 10       | $\mu\text{A}$ |
| $I_{CC}$                       |   | $V_{CC} = 3.6\text{ V}$ , $I_O = 0$ , $V_I = V_{CC}$ or GND                           |                      |     |                    | 10       | $\mu\text{A}$ |
| $\Delta I_{CC}$ <sup>(2)</sup> | Control inputs  | $V_{CC} = 3.6\text{ V}$ , One input at $3\text{ V}$ , Other inputs at $V_{CC}$ or GND |                      |     |                    | 300      | $\mu\text{A}$ |
| $C_i$                          | Control inputs  | $V_I = 3\text{ V}$ or $0$   |                      |     |                    | 2.5      | pF            |
| $C_{i(OFF)}$                   |   | $V_O = 3\text{ V}$ or $0$ , $\overline{OE} = V_{CC}$                                  |                      |     |                    | 7        | pF            |
| $r_{on}$ <sup>(3)</sup>        | $V_{CC} = 2.3\text{ V}$ ,<br>TYP at $V_{CC} = 2.5\text{ V}$ | $V_I = 0$   | $I_I = 64\text{ mA}$ | 7   | 10                 | $\Omega$ |               |
|                                |   |   | $I_I = 24\text{ mA}$ | 7   | 10                 |          |               |
|                                | $V_{CC} = 3\text{ V}$                                       | $V_I = 1.7\text{ V}$  | $I_I = 15\text{ mA}$ | 15  | 25                 |          |               |
|                                |   |   | $I_I = 64\text{ mA}$ | 5   | 7                  |          |               |
|                                | $V_{CC} = 3\text{ V}$                                       | $V_I = 0$   | $I_I = 24\text{ mA}$ | 5   | 7                  |          |               |
|                                |   |   | $I_I = 15\text{ mA}$ | 10  | 15                 |          |               |

(1) All typical values are at  $V_{CC} = 3.3\text{ V}$  (unless otherwise noted),  $T_A = 25^\circ\text{C}$ .

(2) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than  $V_{CC}$  or GND.

(3) Measured by the voltage drop between A and B terminals at the indicated current through the switch. On-state resistance is determined by the lower of the voltages of the two (A or B) terminals.

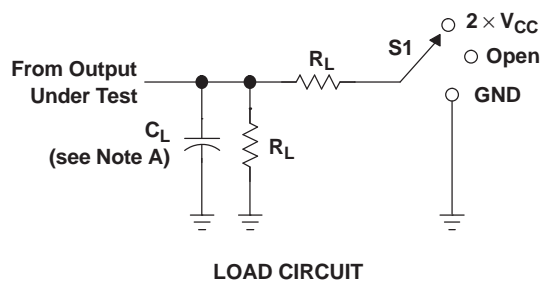
## Switching Characteristics

over recommended operating free-air temperature range (unless otherwise noted) (see [Figure 1](#))

| PARAMETER               | FROM<br>(INPUT) | TO<br>(OUTPUT) | $V_{CC} = 2.5\text{ V}$<br>$\pm 0.2\text{ V}$ |     | $V_{CC} = 3.3\text{ V}$<br>$\pm 0.3\text{ V}$ |     | UNIT |
|-------------------------|-----------------|----------------|---|-----|---|-----|------|
|                         |                 |                | MIN   | MAX | MIN   | MAX |      |
| $t_{pd}$ <sup>(1)</sup> | A or B          | B or A         | 0.15  |     | 0.25  |     | ns   |
| $t_{en}$                | $\overline{OE}$ | A or B         | 1   | 4   | 1   | 4   | ns   |
| $t_{dis}$               | $\overline{OE}$ | A or B         | 1   | 5   | 1   | 4.1 | ns   |

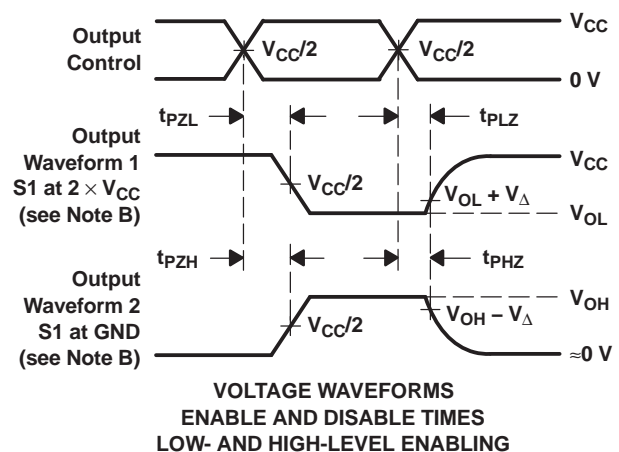
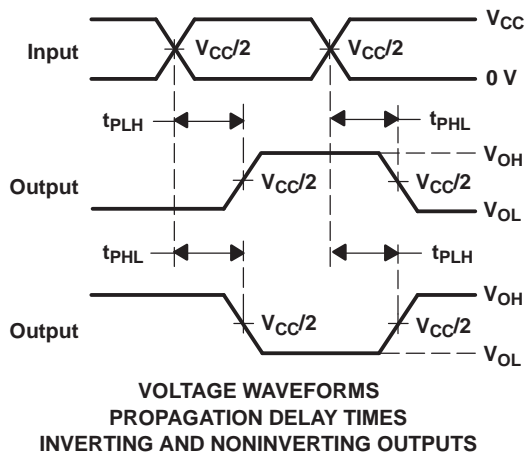
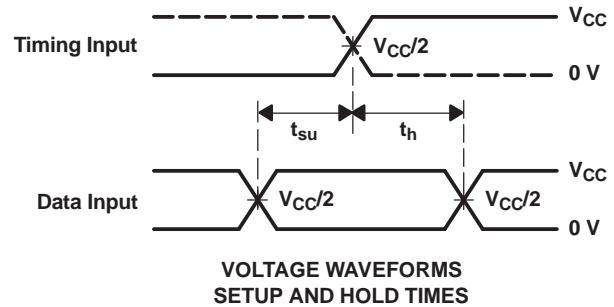
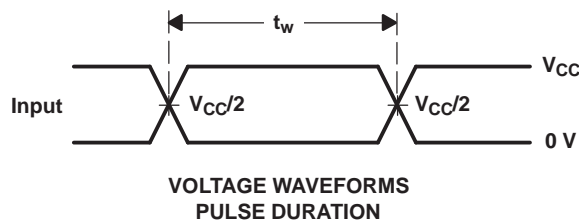
(1) The propagation delay is the calculated RC time constant of the typical on-state resistance of the switch and the specified load capacitance of  $50\text{ pF}$ , when driven by an ideal voltage source (zero output impedance).

**PARAMETER MEASUREMENT INFORMATION**



| TEST              | S1                |
|-------------------|-------------------|
| $t_{PLH}/t_{PHL}$ | Open              |
| $t_{PLZ}/t_{PZL}$ | $2 \times V_{CC}$ |
| $t_{PHZ}/t_{PZH}$ | GND               |

| $V_{CC}$                          | $C_L$ | $R_L$        | $V_{\Delta}$ |
|-----------------------------------|-------|--------------|--------------|
| $2.5 \text{ V} \pm 0.2 \text{ V}$ | 30 pF | 500 $\Omega$ | 0.15 V       |
| $3.3 \text{ V} \pm 0.3 \text{ V}$ | 50 pF | 500 $\Omega$ | 0.3 V        |



- A.  $C_L$  includes probe and jig capacitance.
- B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control.  
Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
- C. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10 \text{ MHz}$ ,  $Z_O = 50 \Omega$ ,  $t_r \leq 2 \text{ ns}$ ,  $t_f \leq 2 \text{ ns}$ .
- D. The outputs are measured one at a time, with one transition per measurement.
- E.  $t_{PLZ}$  and  $t_{PHZ}$  are the same as  $t_{dis}$ .
- F.  $t_{PZL}$  and  $t_{PZH}$  are the same as  $t_{en}$ .
- G.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{pd}$ .
- H. All parameters and waveforms are not applicable to all devices.

**Figure 1. Load Circuit and Voltage Waveforms**

**PACKAGING INFORMATION**

| Orderable Device   | Status<br>(1) | Package Type | Package Drawing | Pins | Package Qty | Eco Plan<br>(2)         | Lead/Ball Finish<br>(6) | MSL Peak Temp<br>(3) | Op Temp (°C) | Device Marking<br>(4/5)    | Samples                 |
|--------------------|---------------|--------------|-----------------|------|-------------|-------------------------|-------------------------|----------------------|--------------|----------------------------|-------------------------|
| 74CBTLV1G125CRG4   | ACTIVE        | SC70         | DCK             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | (VM5, VMJ, VMK, VM O, VMR) | <a href="#">Samples</a> |
| 74CBTLV1G125DBVRE4 | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | (V25J, V25K, V25R)         | <a href="#">Samples</a> |
| 74CBTLV1G125DBVRG4 | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | (V25J, V25K, V25R)         | <a href="#">Samples</a> |
| 74CBTLV1G125DCKRG4 | ACTIVE        | SC70         | DCK             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU               | Level-1-260C-UNLIM   | -40 to 85    | (VM5, VMJ, VMK, VM O, VMR) | <a href="#">Samples</a> |
| SN74CBTLV1G125DBVR | ACTIVE        | SOT-23       | DBV             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | -40 to 85    | (V25J, V25K, V25R)         | <a href="#">Samples</a> |
| SN74CBTLV1G125DCKR | ACTIVE        | SC70         | DCK             | 5    | 3000        | Green (RoHS & no Sb/Br) | CU NIPDAU   CU SN       | Level-1-260C-UNLIM   | -40 to 85    | (VM5, VMJ, VMK, VM O, VMR) | <a href="#">Samples</a> |

(1) The marketing status values are defined as follows:

**ACTIVE:** Product device recommended for new designs.

**LIFEBUY:** TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

**NRND:** Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

**PREVIEW:** Device has been announced but is not in production. Samples may or may not be available.

**OBSELETE:** TI has discontinued the production of the device.

(2) **RoHS:** TI defines "RoHS" to mean semiconductor products that are compliant with the current EU RoHS requirements for all 10 RoHS substances, including the requirement that RoHS substance do not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, "RoHS" products are suitable for use in specified lead-free processes. TI may reference these types of products as "Pb-Free".

**RoHS Exempt:** TI defines "RoHS Exempt" to mean products that contain lead but are compliant with EU RoHS pursuant to a specific EU RoHS exemption.

**Green:** TI defines "Green" to mean the content of Chlorine (Cl) and Bromine (Br) based flame retardants meet JS709B low halogen requirements of <=1000ppm threshold. Antimony trioxide based flame retardants must also meet the <=1000ppm threshold requirement.

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "-" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

<sup>(6)</sup> Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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**OTHER QUALIFIED VERSIONS OF SN74CBTLV1G125 :**

- Automotive: [SN74CBTLV1G125-Q1](#)

NOTE: Qualified Version Definitions:

- Automotive - Q100 devices qualified for high-reliability automotive applications targeting zero defects

**TAPE AND REEL INFORMATION**

**QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE**


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Reel Diameter (mm) | Reel Width W1 (mm) | A0 (mm) | B0 (mm) | K0 (mm) | P1 (mm) | W (mm) | Pin1 Quadrant |
|--------------------|--------------|-----------------|------|------|--------------------|--------------------|---------|---------|---------|---------|--------|---------------|
| SN74CBTLV1G125DBVR | SOT-23       | DBV             | 5    | 3000 | 178.0              | 9.0                | 3.3     | 3.2     | 1.4     | 4.0     | 8.0    | Q3            |
| SN74CBTLV1G125DBVR | SOT-23       | DBV             | 5    | 3000 | 180.0              | 8.4                | 3.23    | 3.17    | 1.37    | 4.0     | 8.0    | Q3            |
| SN74CBTLV1G125DCKR | SC70         | DCK             | 5    | 3000 | 180.0              | 8.4                | 2.47    | 2.3     | 1.25    | 4.0     | 8.0    | Q3            |
| SN74CBTLV1G125DCKR | SC70         | DCK             | 5    | 3000 | 178.0              | 9.0                | 2.4     | 2.5     | 1.2     | 4.0     | 8.0    | Q3            |

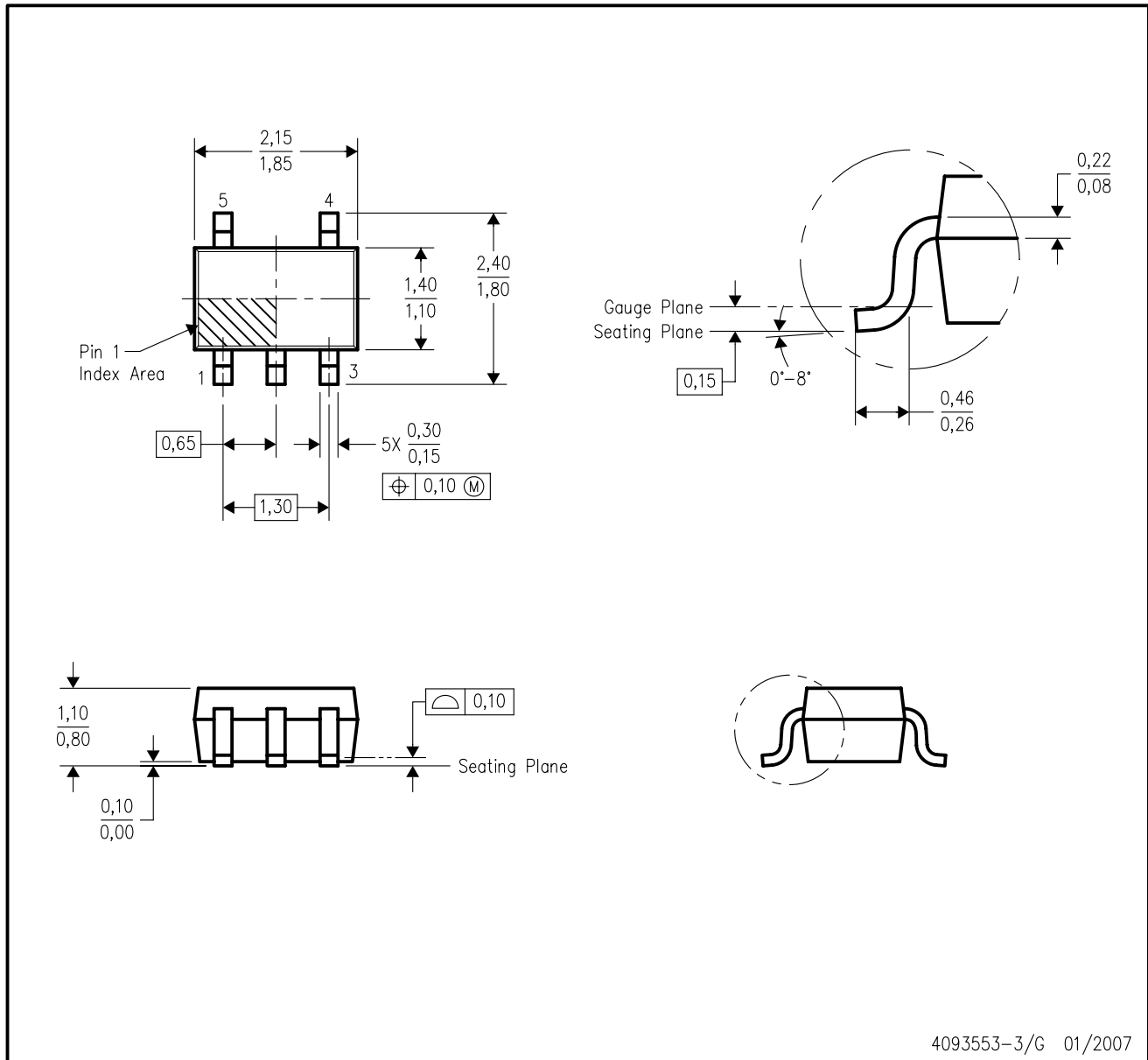
**TAPE AND REEL BOX DIMENSIONS**


\*All dimensions are nominal

| Device             | Package Type | Package Drawing | Pins | SPQ  | Length (mm) | Width (mm) | Height (mm) |
|--------------------|--------------|-----------------|------|------|-------------|------------|-------------|
| SN74CBTLV1G125DBVR | SOT-23       | DBV             | 5    | 3000 | 180.0       | 180.0      | 18.0        |
| SN74CBTLV1G125DBVR | SOT-23       | DBV             | 5    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74CBTLV1G125DCKR | SC70         | DCK             | 5    | 3000 | 202.0       | 201.0      | 28.0        |
| SN74CBTLV1G125DCKR | SC70         | DCK             | 5    | 3000 | 180.0       | 180.0      | 18.0        |

DCK (R-PDSO-G5)

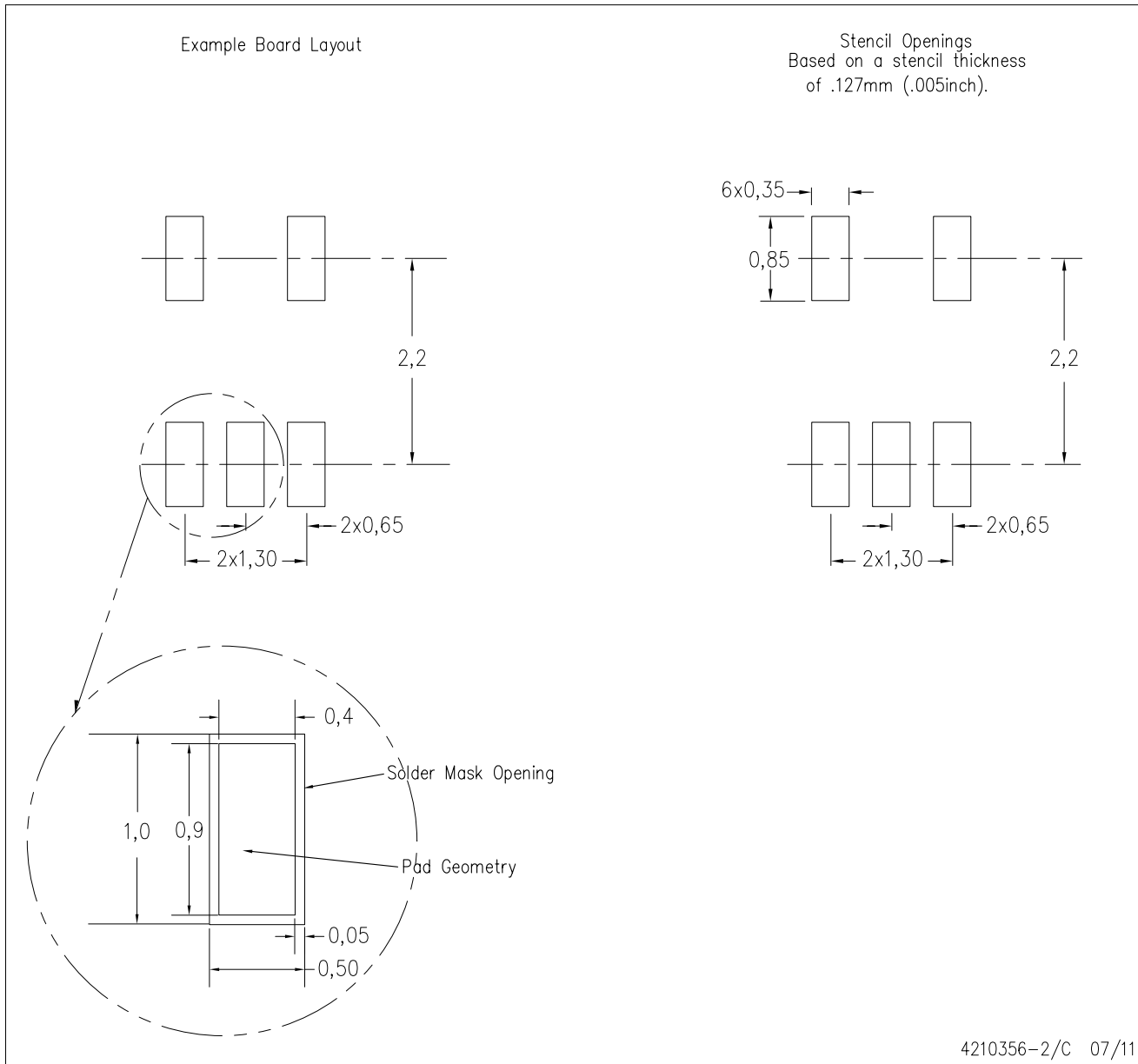
PLASTIC SMALL-OUTLINE PACKAGE



- NOTES:
- A. All linear dimensions are in millimeters.
  - B. This drawing is subject to change without notice.
  - C. Body dimensions do not include mold flash or protrusion. Mold flash and protrusion shall not exceed 0.15 per side.
  - D. Falls within JEDEC MO-203 variation AA.

DCK (R-PDSO-G5)

PLASTIC SMALL OUTLINE



- NOTES:
- All linear dimensions are in millimeters.
  - This drawing is subject to change without notice.
  - Customers should place a note on the circuit board fabrication drawing not to alter the center solder mask defined pad.
  - Publication IPC-7351 is recommended for alternate designs.
  - Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Example stencil design based on a 50% volumetric metal load solder paste. Refer to IPC-7525 for other stencil recommendations.

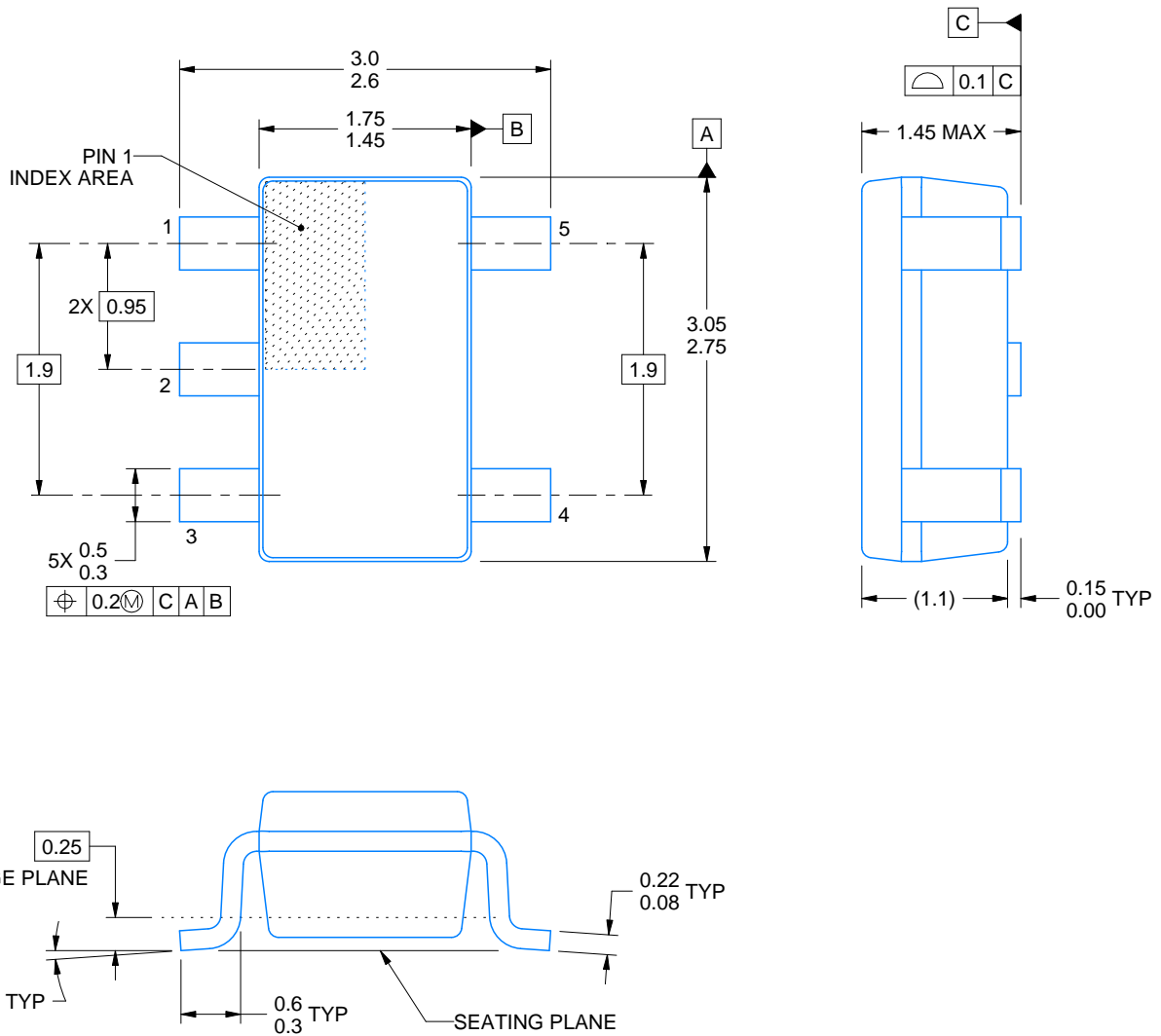
DBV0005A



# PACKAGE OUTLINE

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



4214839/D 11/2018

NOTES:

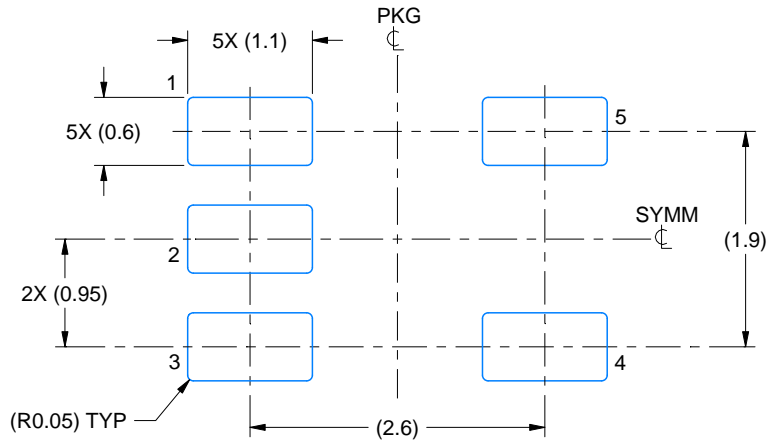
1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Reference JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.

# EXAMPLE BOARD LAYOUT

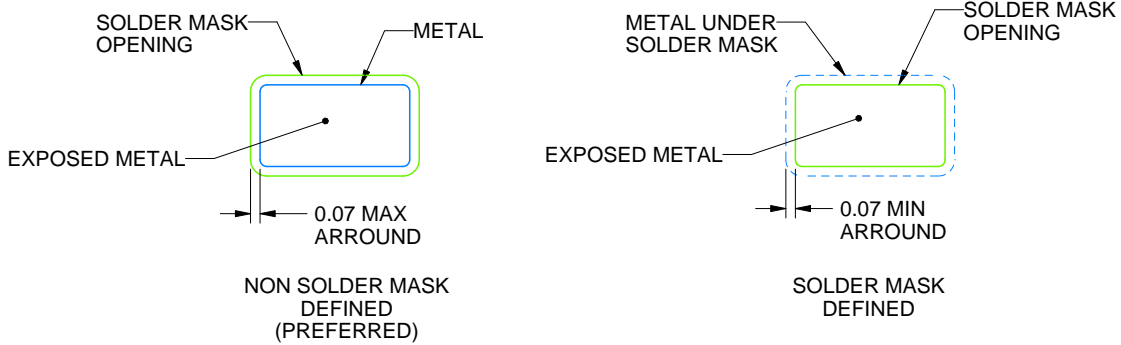
DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



LAND PATTERN EXAMPLE  
EXPOSED METAL SHOWN  
SCALE:15X



SOLDER MASK DETAILS

4214839/D 11/2018

NOTES: (continued)

- 5. Publication IPC-7351 may have alternate designs.
- 6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.

# EXAMPLE STENCIL DESIGN

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



SOLDER PASTE EXAMPLE  
BASED ON 0.125 mm THICK STENCIL  
SCALE:15X

4214839/D 11/2018

NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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