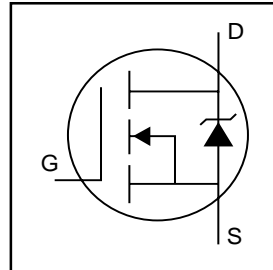


IRLR/U014N

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Surface Mount (IRLR024N)
- Straight Lead (IRLU024N)
- Advanced Process Technology
- Fast Switching
- Fully Avalanche Rated

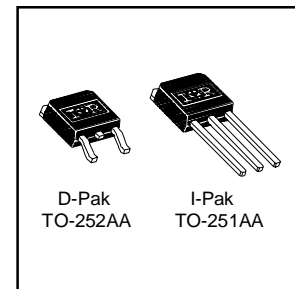


$V_{DSS} = 55V$
$R_{DS(on)} = 0.14\Omega$
$I_D = 10A$

Description

Fifth Generation HEXFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET Power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

The D-PAK is designed for surface mounting using vapor phase, infrared, or wave soldering techniques. The straight lead version (IRFU series) is for through-hole mounting applications. Power dissipation levels up to 1.5 watts are possible in typical surface mount applications.



Absolute Maximum Ratings

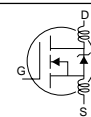
	Parameter	Max.	Units
$I_D @ T_C = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	10	A
$I_D @ T_C = 100^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	7.1	
I_{DM}	Pulsed Drain Current ①	40	
$P_D @ T_C = 25^\circ C$	Power Dissipation	28	W
	Linear Derating Factor	0.2	W/°C
V_{GS}	Gate-to-Source Voltage	± 16	V
E_{AS}	Single Pulse Avalanche Energy②	35	mJ
I_{AR}	Avalanche Current①	6.0	A
E_{AR}	Repetitive Avalanche Energy①	2.8	mJ
dv/dt	Peak Diode Recovery dv/dt ③	5.0	V/ns
T_J	Operating Junction and	-55 to + 175	°C
T_{STG}	Storage Temperature Range		
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	

Thermal Resistance

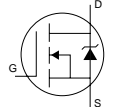
	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	5.3	°C/W
$R_{\theta JA}$	Case-to-Ambient (PCB mount)**	—	50	
$R_{\theta JA}$	Junction-to-Ambient	—	110	

** When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

Electrical Characteristics @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V _{(BR)DSS}	Drain-to-Source Breakdown Voltage	55	—	—	V	V _{GS} = 0V, I _D = 250μA
ΔV _{(BR)DSS/ΔT_J}	Breakdown Voltage Temp. Coefficient	—	0.056	—	V/°C	Reference to 25°C, I _D = 1mA
R _{DSON}	Static Drain-to-Source On-Resistance	—	—	0.14	Ω	V _{GS} = 10V, I _D = 6A ④
		—	—	0.21		V _{GS} = 4.5V, I _D = 5A ④
V _{GS(th)}	Gate Threshold Voltage	1.0	—	—	V	V _{DS} = V _{GS} , I _D = 250μA
g _{fs}	Forward Transconductance	3.1	—	—	S	V _{DS} = 25V, I _D = 6A ⑦
I _{DSS}	Drain-to-Source Leakage Current	—	—	25	μA	V _{DS} = 55V, V _{GS} = 0V
		—	—	250		V _{DS} = 55V, V _{GS} = 0V, T _J = 150°C
I _{GSS}	Gate-to-Source Forward Leakage	—	—	100	nA	V _{GS} = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V _{GS} = -16V
Q _g	Total Gate Charge	—	—	7.9	nC	I _D = 6A
Q _{gs}	Gate-to-Source Charge	—	—	1.4		V _{DS} = 44V
Q _{gd}	Gate-to-Drain ("Miller") Charge	—	—	4.4		V _{GS} = 5.0V, See Fig. 6 and 13 ④
t _{d(on)}	Turn-On Delay Time	—	6.5	—		ns
t _r	Rise Time	—	47	—	I _D = 6A	
t _{d(off)}	Turn-Off Delay Time	—	12	—	R _G = 6.2Ω, V _{GS} = 5.0V	
t _f	Fall Time	—	23	—	R _D = 4.5Ω, See Fig. 10 ④	
L _D	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact ⑥
L _S	Internal Source Inductance	—	7.5	—		
C _{iss}	Input Capacitance	—	265	—	pF	V _{GS} = 0V
C _{oss}	Output Capacitance	—	80	—		V _{DS} = 25V
C _{rss}	Reverse Transfer Capacitance	—	38	—		f = 1.0MHz, See Fig. 5

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I _S	Continuous Source Current (Body Diode)	—	—	10	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I _{SM}	Pulsed Source Current (Body Diode) ①	—	—	40		
V _{SD}	Diode Forward Voltage	—	—	1.3	V	T _J = 25°C, I _S = 6A, V _{GS} = 0V ④
t _{rr}	Reverse Recovery Time	—	37	56	nS	T _J = 25°C, I _F = 6A
Q _{rr}	Reverse Recovery Charge	—	48	71	nC	di/dt = 100A/μs ④
t _{on}	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L _S +L _D)				

Notes:

① Repetitive rating; pulse width limited by max. junction temperature. (See fig. 11)

② Starting T_J = 25°C, L = 1.96mH
R_G = 25Ω, I_{AS} = 6A. (See Figure 12)

③ I_{SD} ≤ 6.0A, di/dt ≤ 210A/μs, V_{DD} ≤

V_{(BR)DSS},
T_J ≤ 175°C
2

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ This is applied for I-PAK, L_S of D-PAK is measured between lead and center of die contact

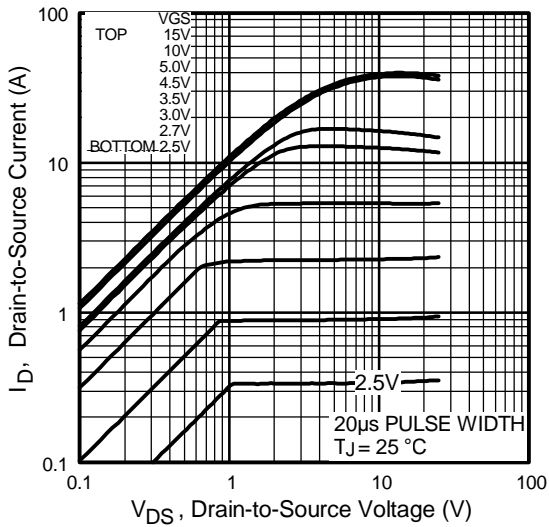


Fig 1. Typical Output Characteristics

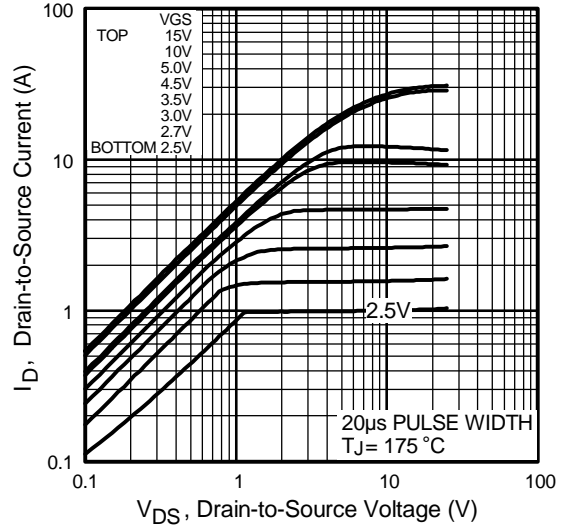


Fig 2. Typical Output Characteristics

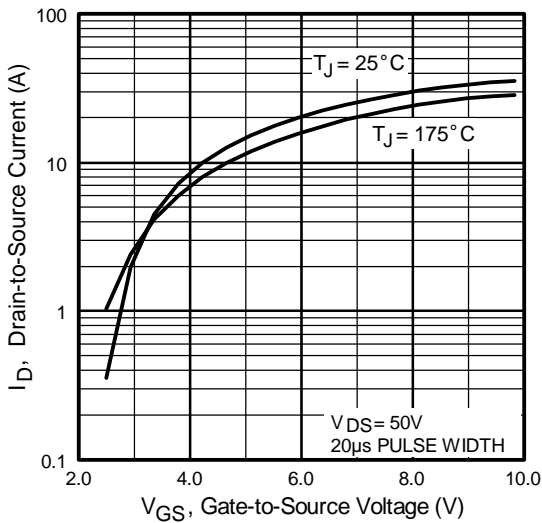


Fig 3. Typical Transfer Characteristics

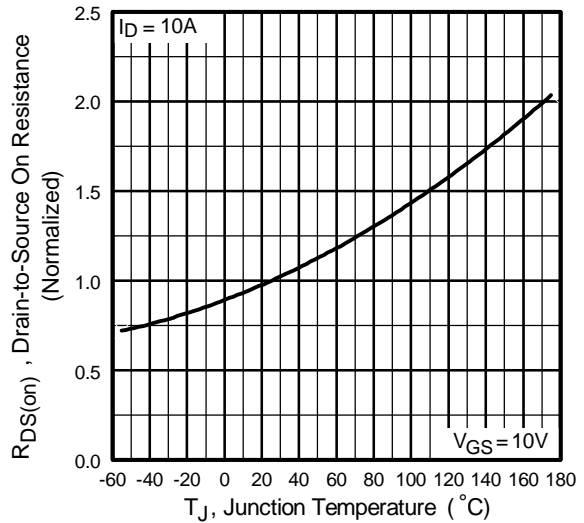


Fig 4. Normalized On-Resistance Vs. Temperature

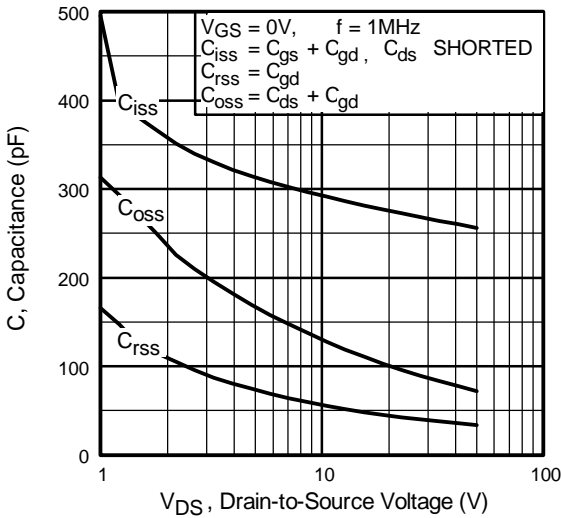


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

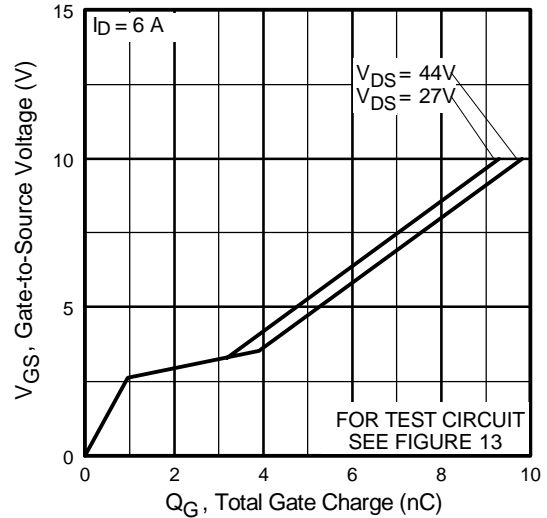


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

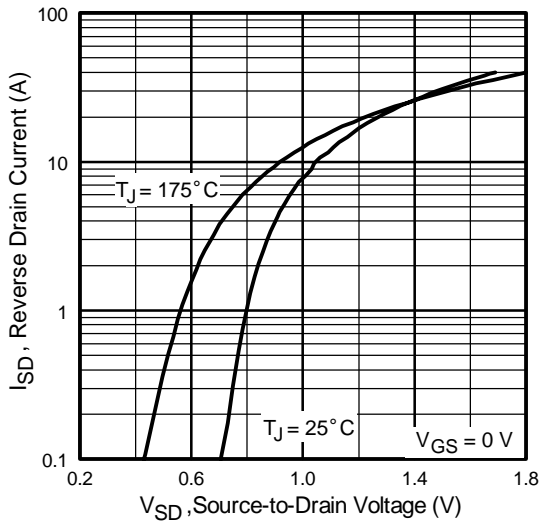


Fig 7. Typical Source-Drain Diode Forward Voltage

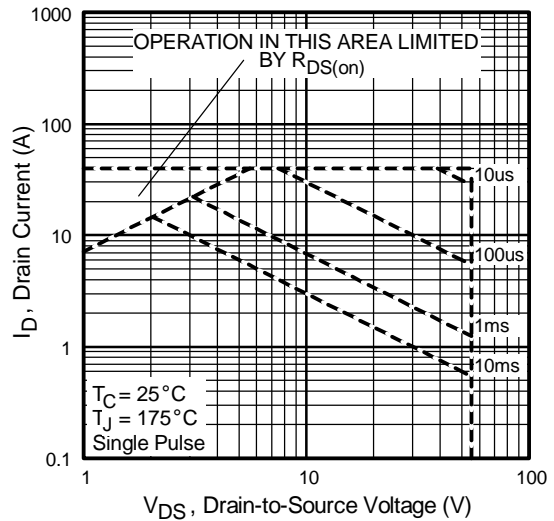


Fig 8. Maximum Safe Operating Area

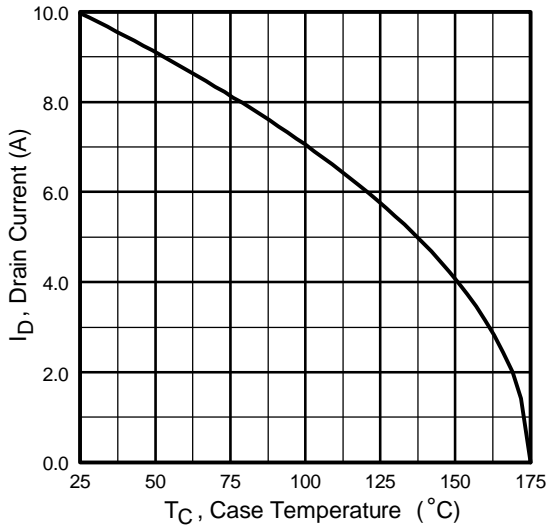


Fig 9. Maximum Drain Current Vs. Case Temperature

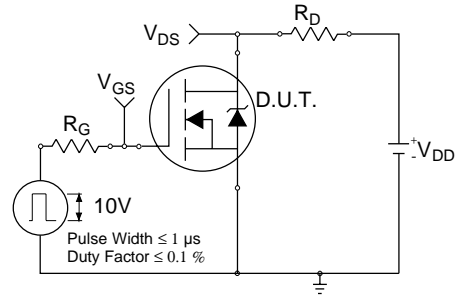


Fig 10a. Switching Time Test Circuit

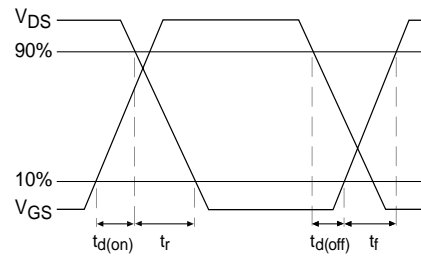


Fig 10b. Switching Time Waveforms

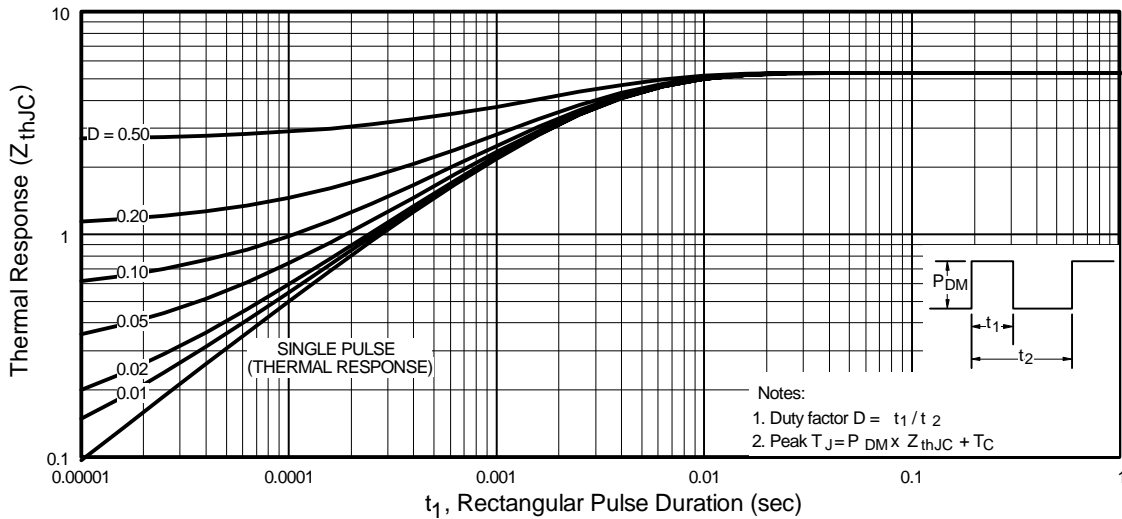


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

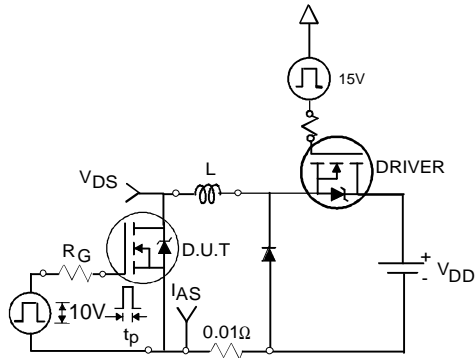


Fig 12a. Unclamped Inductive Test Circuit

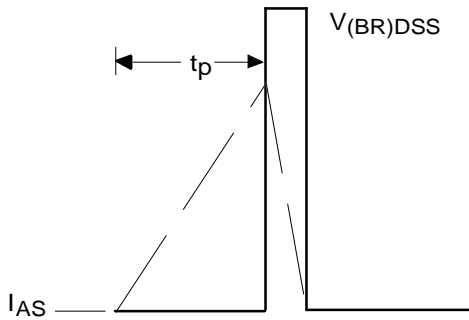


Fig 12b. Unclamped Inductive Waveforms

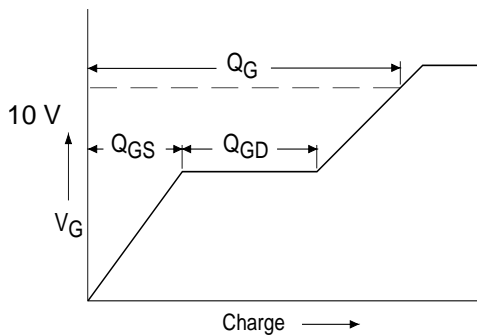


Fig 13a. Basic Gate Charge Waveform

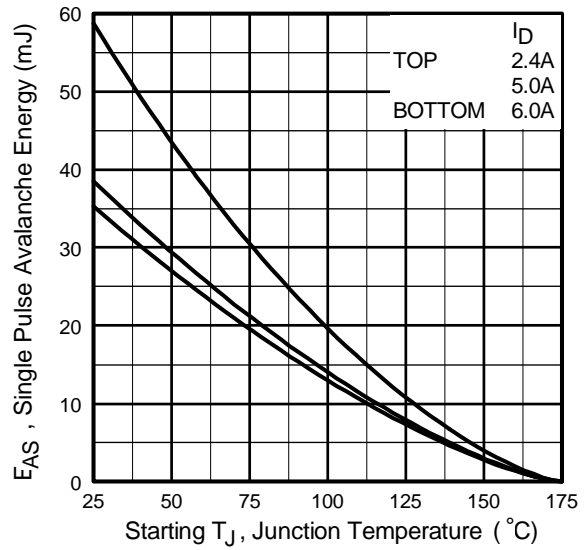


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

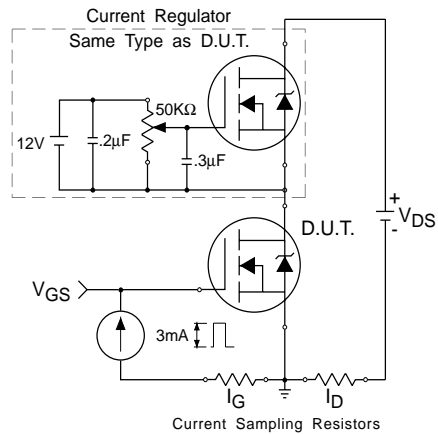
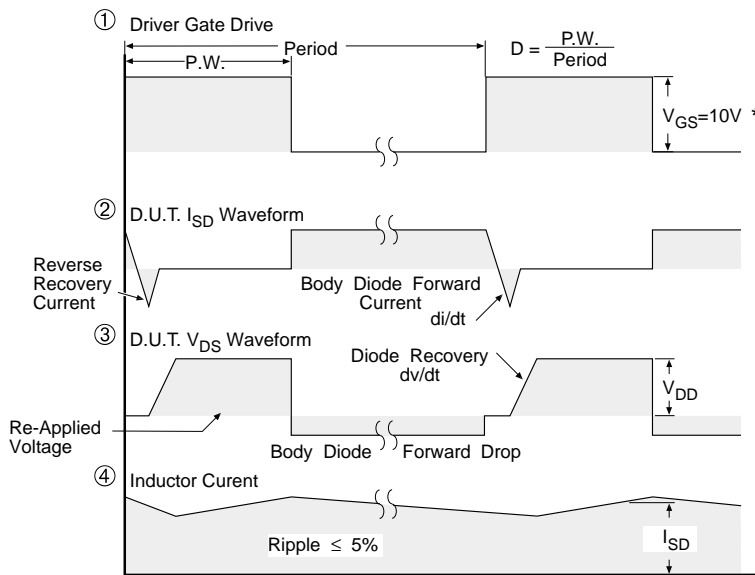
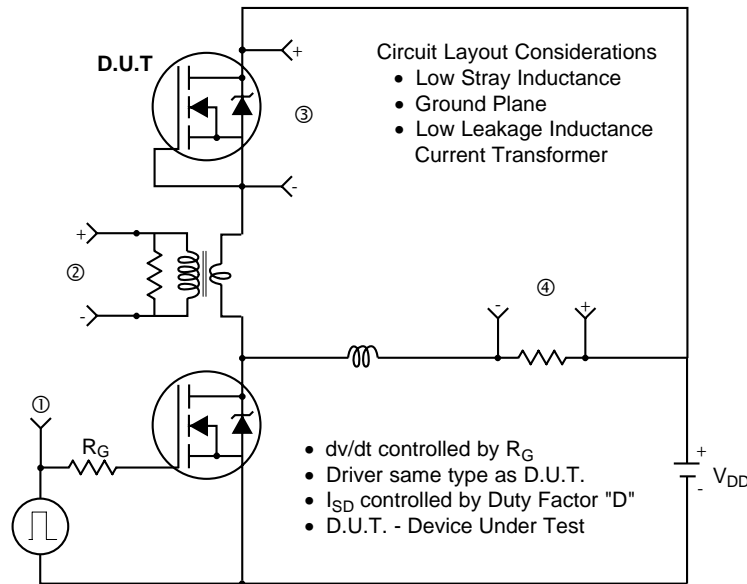


Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



* $V_{GS} = 5V$ for Logic Level Devices

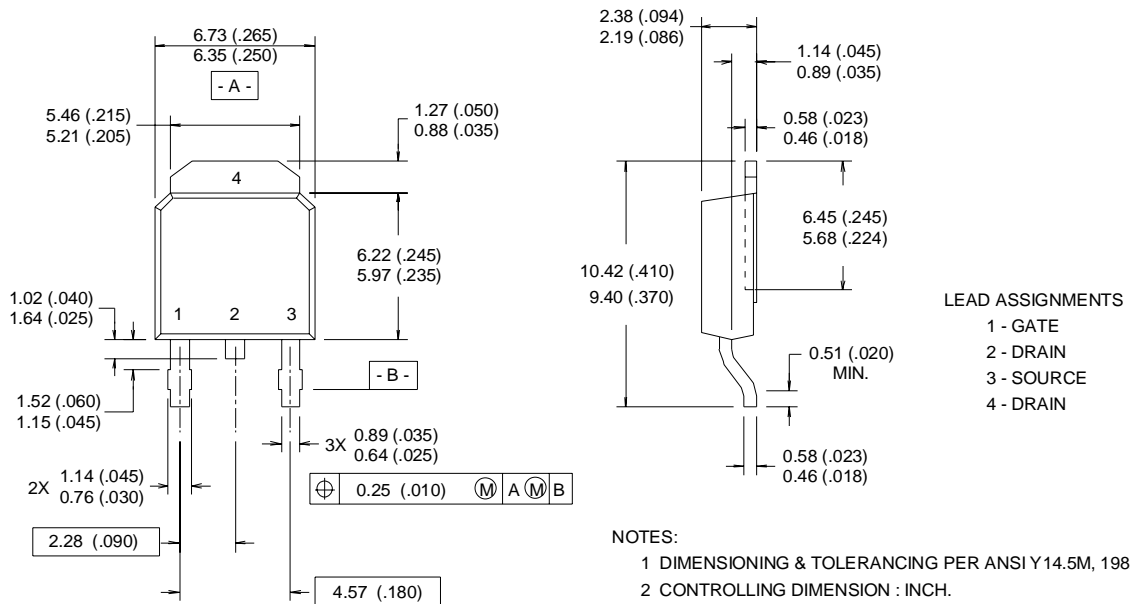
Fig 14. For N-Channel HEXFETS

IRLR/U014N

Package Outline

TO-252AA Outline

Dimensions are shown in millimeters (inches)

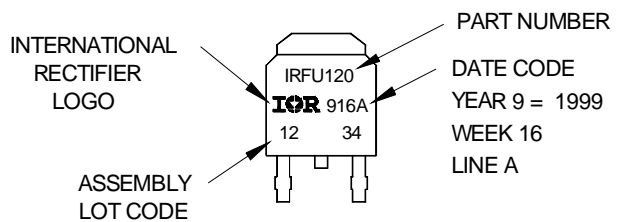


- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
 - 2 CONTROLLING DIMENSION : INCH.
 - 3 CONFORMS TO JEDEC OUTLINE TO-252AA.
 - 4 DIMENSIONS SHOWN ARE BEFORE SOLDER DIP, SOLDER DIP MAX. +0.16 (.006).

Part Marking Information

TO-252AA (D-PAK)

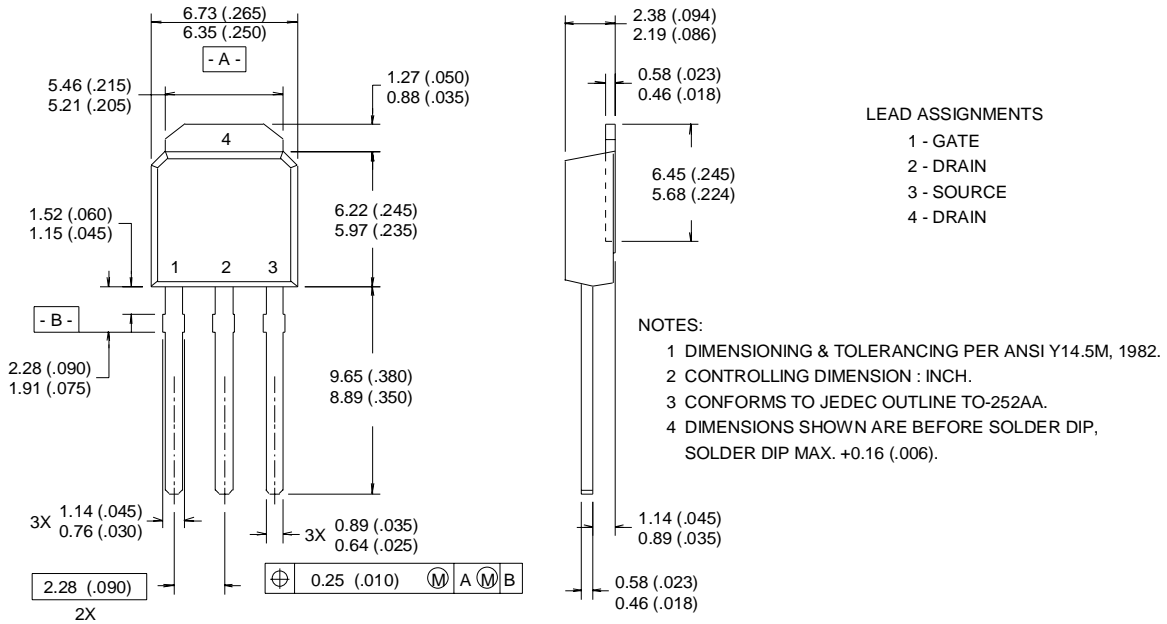
EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"



Package Outline

TO-251AA Outline

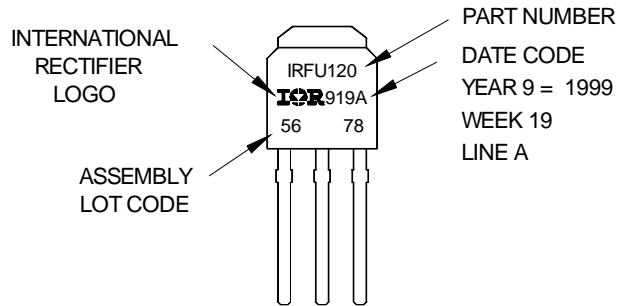
Dimensions are shown in millimeters (inches)



Part Marking Information

TO-251AA (I-PAK)

EXAMPLE: THIS IS AN IRFR120
 WITH ASSEMBLY
 LOT CODE 5678
 ASSEMBLED ON WW 19, 1999
 IN THE ASSEMBLY LINE "A"



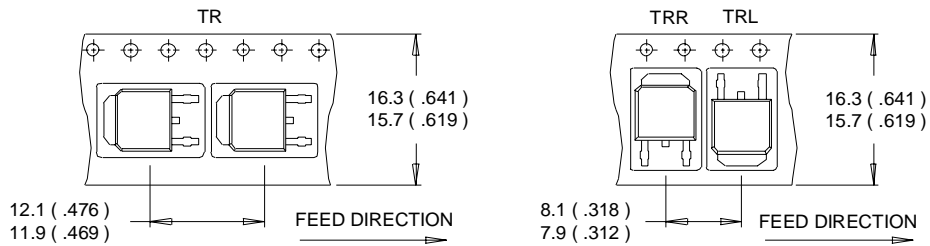
IRLR/U014N

International
IR Rectifier

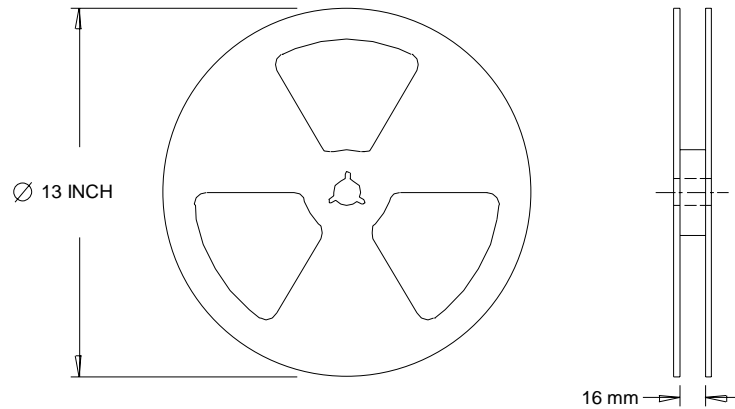
Tape & Reel Information

TO-252AA

Dimensions are shown in millimeters (inches)



- NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
 2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
 3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



- NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Data and specifications subject to change without notice.
This product has been designed and qualified for the Automotive[Q101] market.
Qualification Standards can be found on IR's Web site.

International
IR Rectifier

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Note: For the most current drawings please refer to the IR website at:
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