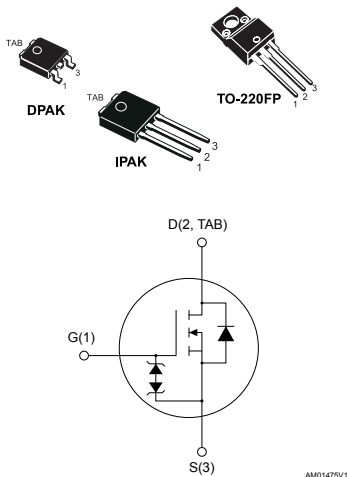




# THE DATASHEET OF STD2N62K3



## N-channel 620 V, 2.9 $\Omega$ typ., 2.2 A MDmesh™ K3 Power MOSFETs in DPAK, TO-220FP and IPAK packages



AM01475V1

### Features

Order code	$V_{DS}$	$R_{DS(on)max.}$	$I_D$	Package
STD2N62K3	620 V	3.6 $\Omega$	2.2 A	DPAK
STF2N62K3				TO-220FP
STU2N62K3				IPAK

- 100% avalanche tested
- Extremely high dv/dt capability
- Very low intrinsic capacitance
- Improved diode reverse recovery characteristics
- Zener-protected

### Applications

- Switching applications

### Description

These MDmesh™ K3 Power MOSFETs are the result of improvements applied to STMicroelectronics' MDmesh™ technology, combined with a new optimized vertical structure. These devices boast an extremely low on-resistance, superior dynamic performance and high avalanche capability, rendering them suitable for the most demanding applications.

#### Product status link

[STD2N62K3](#)
[STF2N62K3](#)
[STU2N62K3](#)

# 1 Electrical ratings

**Table 1. Absolute maximum ratings**

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	IPAK	
$V_{DS}$	Drain-source voltage	620			V
$V_{GS}$	Gate-source voltage	±30			V
$I_D$	Drain current (continuous) at $T_C = 25\text{ °C}$	2.2	2.2 <sup>(1)</sup>	2.2	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ °C}$	1	1 <sup>(1)</sup>	1	A
$I_{DM}^{(2)}$	Drain current (pulsed)	8.8			A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ °C}$	45	20	45	W
$V_{ISO}$	Insulation withstand voltage (RMS) from all three leads to external heat-sink ( $t = 1\text{ s}$ , $T_C = 25\text{ °C}$ )	-	2500	-	V
$dv/dt^{(3)}$	Peak diode recovery voltage slope	12			V/ns
$T_j$	Operating junction temperature range	-55 to 150			°C
$T_{stg}$	Storage temperature range				

- Limited by maximum junction temperature.
- Pulse width limited by safe operating area.
- $I_{SD} \leq 2.2\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{D\text{peak}} \leq V_{(BR)DSS}$ ,  $V_{DD} = 80\% V_{(BR)DSS}$ .

**Table 2. Thermal data**

Symbol	Parameter	Value			Unit
		DPAK	TO-220FP	IPAK	
$R_{thj\text{-case}}$	Thermal resistance junction-case	2.78	6.25	2.78	°C/W
$R_{thj\text{-amb}}$	Thermal resistance junction-ambient		62.5	100	°C/W
$R_{thj\text{-pcb}}^{(1)}$	Thermal resistance junction-pcb	50			°C/W

- When mounted on 1inch<sup>2</sup> FR-4 board, 2 oz Cu.

**Table 3. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}^{(1)}$	Avalanche current, repetitive or not-repetitive	2.2	A
$E_{AS}^{(2)}$	Single pulse avalanche energy	85	mJ

- Pulse width limited by  $T_j$  max.
- Starting  $T_j = 25\text{ °C}$ ,  $I_D = I_{AR}$ ,  $V_{DD} = 50\text{ V}$ .

## 2 Electrical characteristics

( $T_{CASE} = 25\text{ °C}$  unless otherwise specified)

**Table 4. On/off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage	$I_D = 1\text{ mA}$ , $V_{GS} = 0\text{ V}$	620			V
$I_{DSS}$	Zero gate voltage drain current	$V_{GS} = 0\text{ V}$ , $V_{DS} = 620\text{ V}$			1	$\mu\text{A}$
		$V_{GS} = 0\text{ V}$ , $V_{DS} = 620\text{ V}$ , $T_C = 125\text{ °C}$ <sup>(1)</sup>			50	$\mu\text{A}$
$I_{GSS}$	Gate body leakage current	$V_{DS} = 0\text{ V}$ , $V_{GS} = \pm 20\text{ V}$			$\pm 10$	$\mu\text{A}$
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}$ , $I_D = 50\text{ }\mu\text{A}$	3	3.75	4.5	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}$ , $I_D = 1.1\text{ A}$		2.9	3.6	$\Omega$

1. Defined by design, not subject to production test.

**Table 5. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}$ , $f = 1\text{ MHz}$ , $V_{GS} = 0\text{ V}$	-	340	-	$\mu\text{F}$
$C_{oss}$	Output capacitance			26		
$C_{rss}$	Reverse transfer capacitance			4		
$C_{o(tr)}$ <sup>(1)</sup>	Equivalent capacitance time related	$V_{DS} = 0\text{ to }496\text{ V}$ , $V_{GS} = 0\text{ V}$	-	17	-	$\mu\text{F}$
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz}$ open drain	-	5	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 496\text{ V}$ , $I_D = 2.2\text{ A}$ , $V_{GS} = 0\text{ to }10\text{ V}$ (see Figure 17. Test circuit for gate charge behavior)	-	15	-	nC
$Q_{gs}$	Gate-source charge			3		
$Q_{gd}$	Gate-drain charge			9		

1.  $C_{o(tr)}$  is a constant capacitance value that gives the same charging time as  $C_{oss}$  while  $V_{DS}$  is rising from 0 to 80%  $V_{DSS}$ .

**Table 6. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 310\text{ V}$ , $I_D = 1.1\text{ A}$ , $R_G = 4.7\text{ }\Omega$ , $V_{GS} = 10\text{ V}$ (see Figure 16. Test circuit for resistive load switching times and Figure 21. Switching time waveform)	-	8	-	ns
$t_r$	Rise time			4.4		
$t_{d(off)}$	Turn-off delay time			21		
$t_f$	Fall time			22		

**Table 7. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current		-		2.2	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				8.8	
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 2.2 \text{ A}$ , $V_{GS} = 0 \text{ V}$	-		1.6	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.2 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$	-	200		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ (see Figure 18. Test circuit for inductive load switching and diode recovery times)		0.9		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			9		A
$t_{rr}$	Reverse recovery time	$I_{SD} = 2.2 \text{ A}$ , $di/dt = 100 \text{ A}/\mu\text{s}$	-	240		ns
$Q_{rr}$	Reverse recovery charge	$V_{DD} = 60 \text{ V}$ , $T_j = 150 \text{ }^\circ\text{C}$ (see Figure 18. Test circuit for inductive load switching and diode recovery times)		1.15		$\mu\text{C}$
$I_{RRM}$	Reverse recovery current			10		A

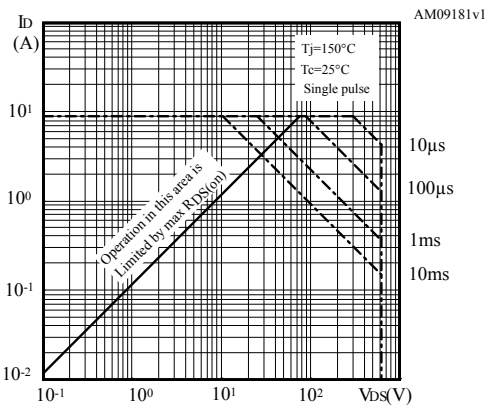
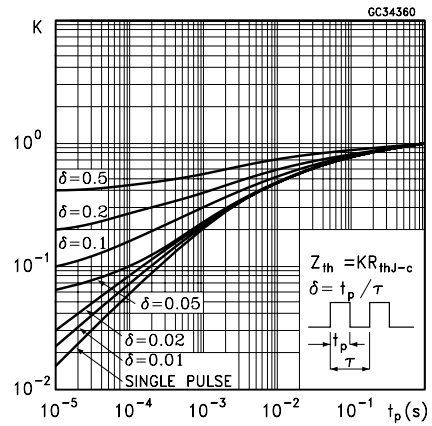
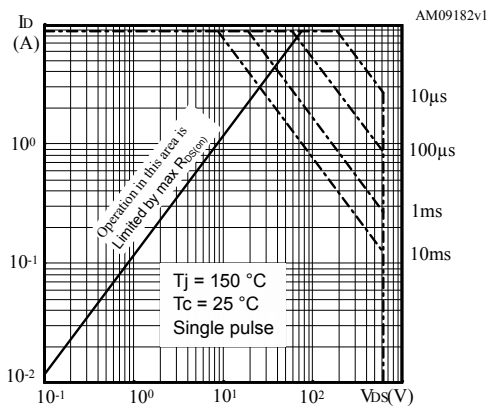
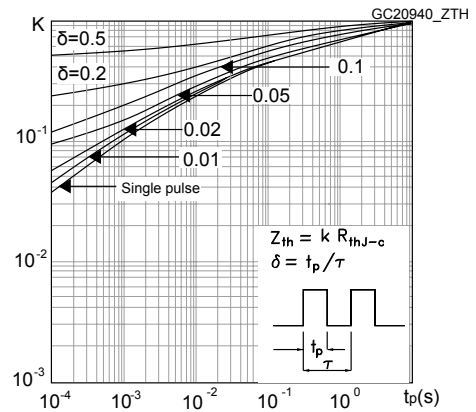
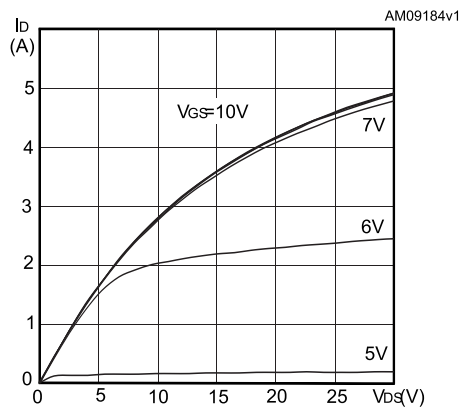
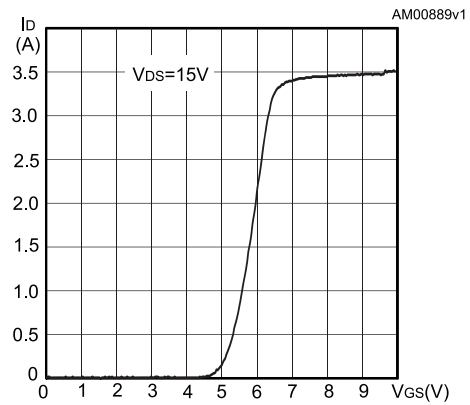
1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%.

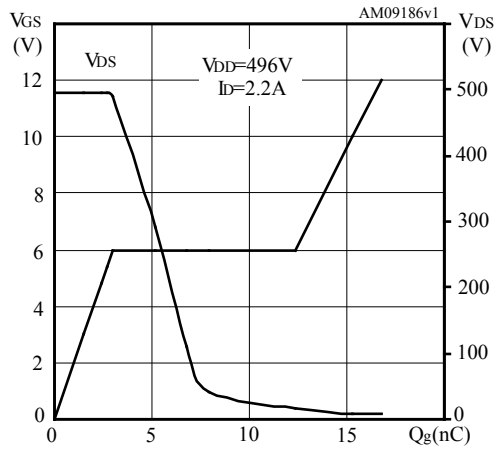
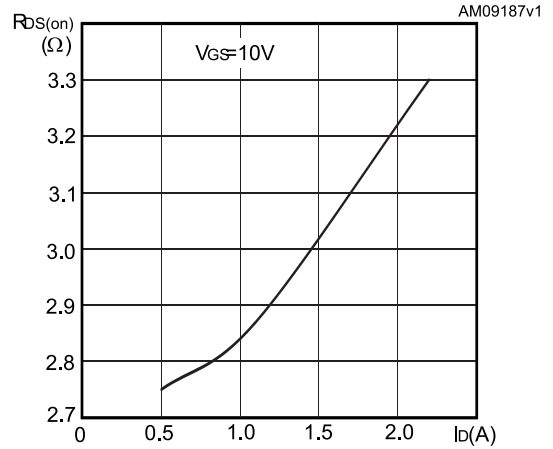
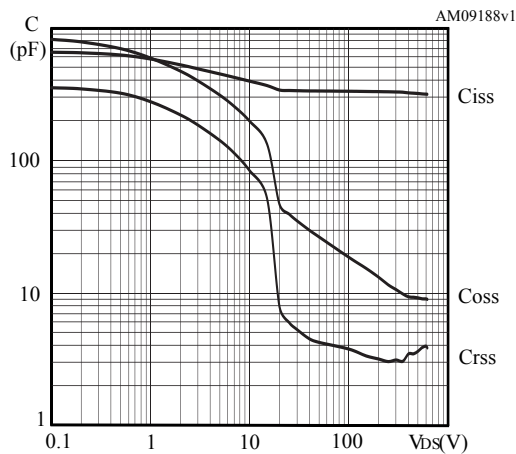
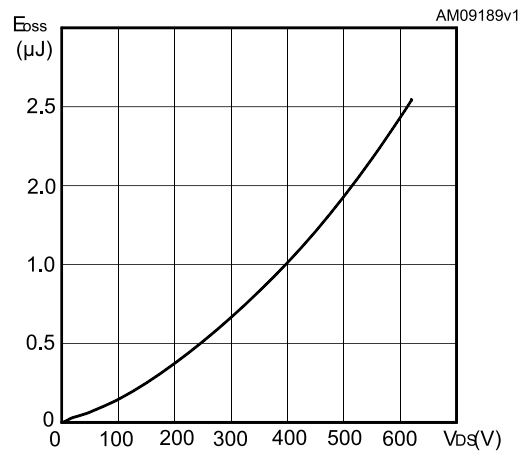
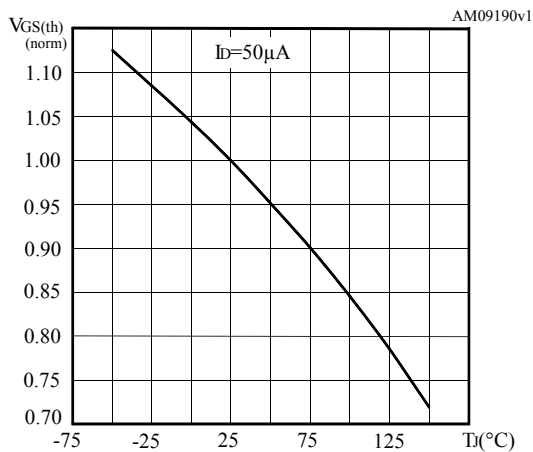
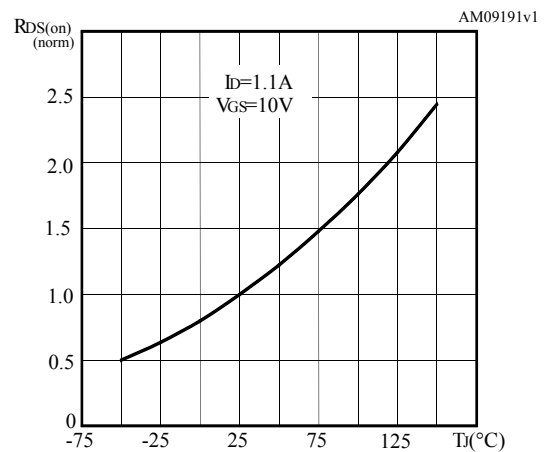
**Table 8. Gate-source Zener diode**

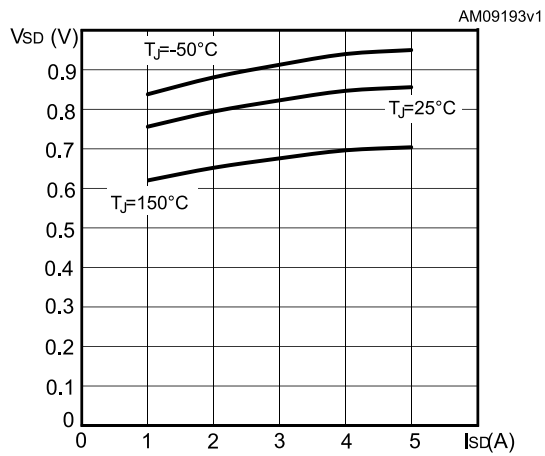
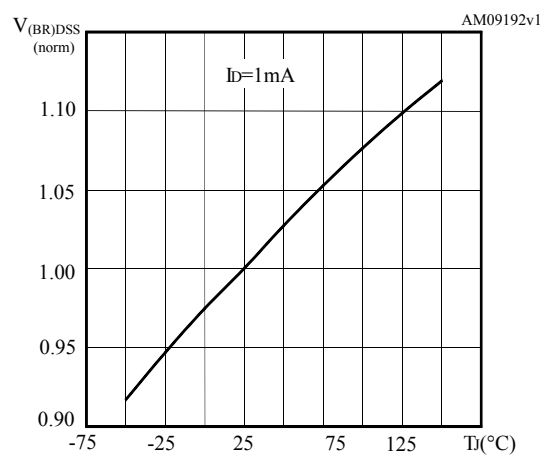
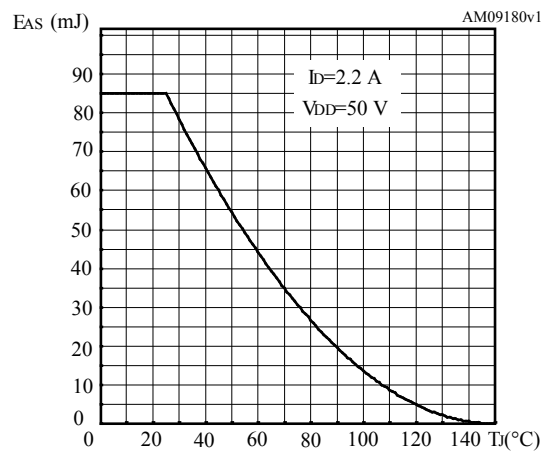
Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)GSO}$	Gate-source breakdown voltage	$I_{GS} = \pm 1 \text{ mA}$ , $I_D = 0 \text{ A}$	$\pm 30$			V

The built-in back-to-back Zener diodes are specifically designed to enhance the ESD performance of the device. The Zener voltage facilitates efficient and cost-effective device integrity protection, thus eliminating the need for additional external componentry.

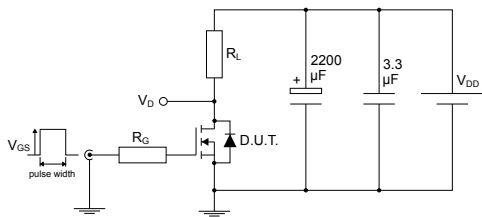
## 2.1 Electrical characteristics curves

**Figure 1. Safe operating area for DPAK and IPAK**

**Figure 2. Thermal impedance for DPAK and IPAK**

**Figure 3. Safe operating area for TO-220FP**

**Figure 4. Thermal impedance for TO-220FP**

**Figure 5. Output characteristics**

**Figure 6. Transfer characteristics**


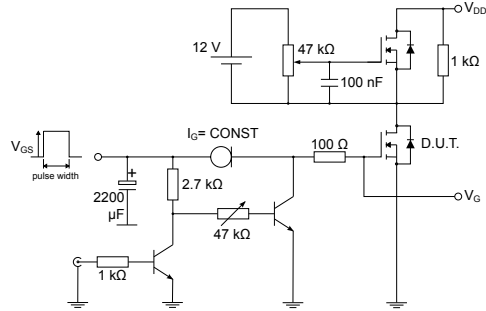
**Figure 7. Gate charge vs gate-source voltage**

**Figure 8. Static drain-source on-resistance**

**Figure 9. Capacitance variations**

**Figure 10. Output capacitance stored energy**

**Figure 11. Normalized gate threshold voltage vs temperature**

**Figure 12. Normalized on-resistance vs temperature**


**Figure 13. Source-drain diode forward characteristics**

**Figure 14. Normalized  $V_{(BR)DSS}$  vs temperature**

**Figure 15. Maximum avalanche energy vs starting  $T_j$** 


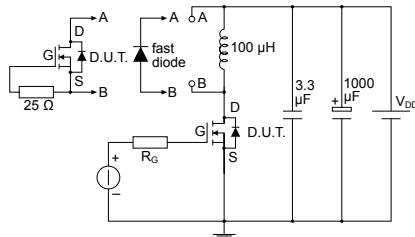
### 3 Test circuits

**Figure 16. Test circuit for resistive load switching times**


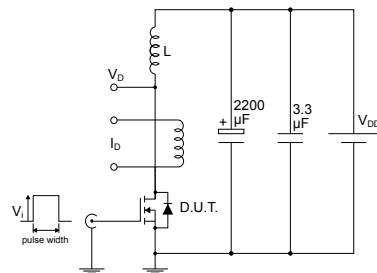
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**Figure 17. Test circuit for gate charge behavior**


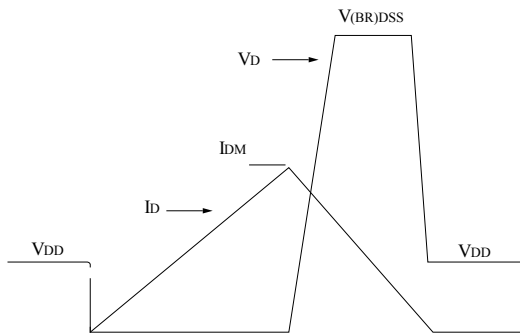
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**Figure 18. Test circuit for inductive load switching and diode recovery times**


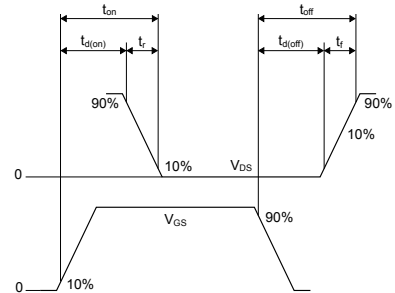
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**Figure 19. Unclamped inductive load test circuit**


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**Figure 20. Unclamped inductive waveform**


AM01472v1

**Figure 21. Switching time waveform**


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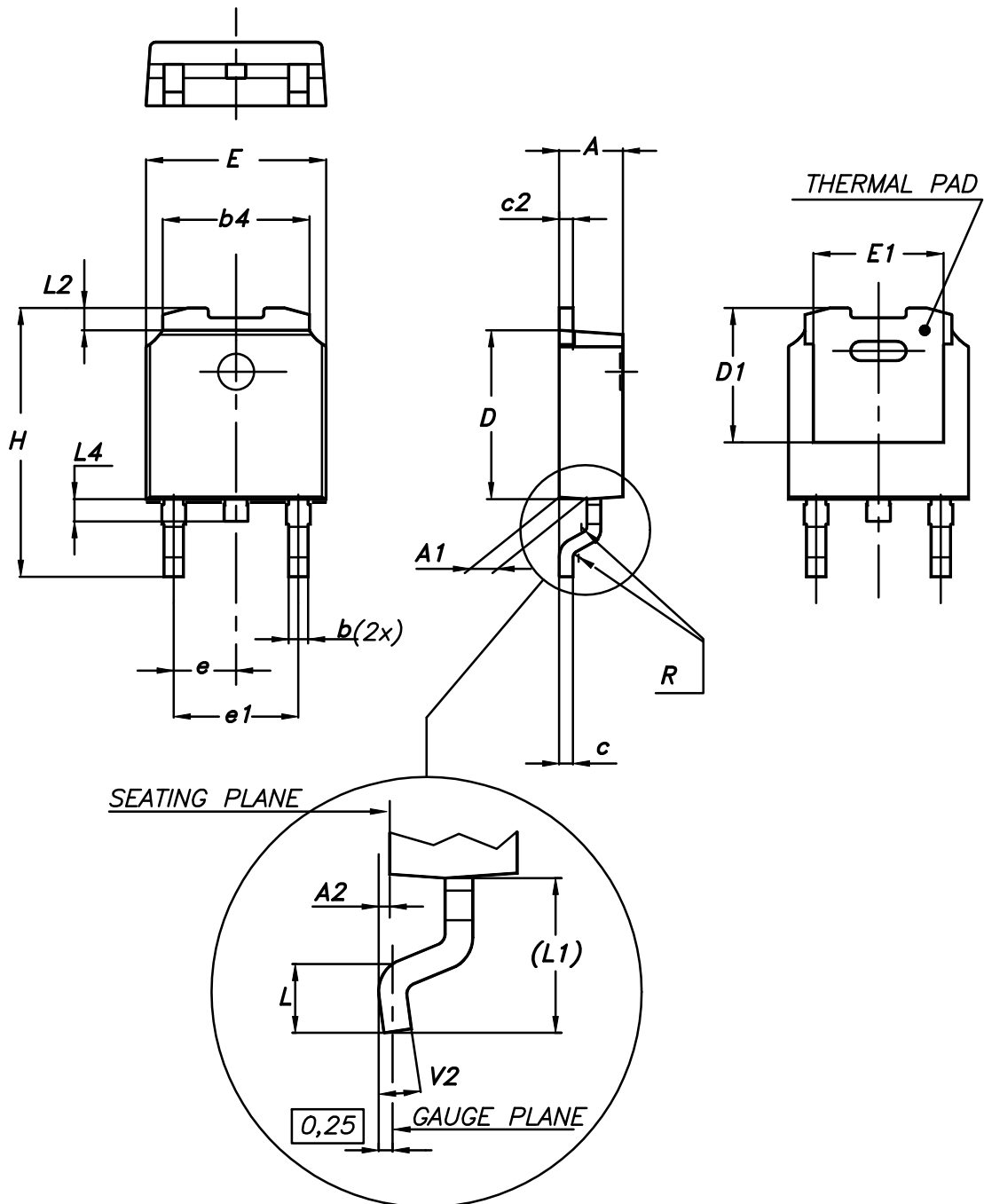
## 4 Package information

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In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK® specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK® is an ST trademark.

**4.1 DPAK (TO-252) type A package information**

Figure 22. DPAK (TO-252) type A package outline



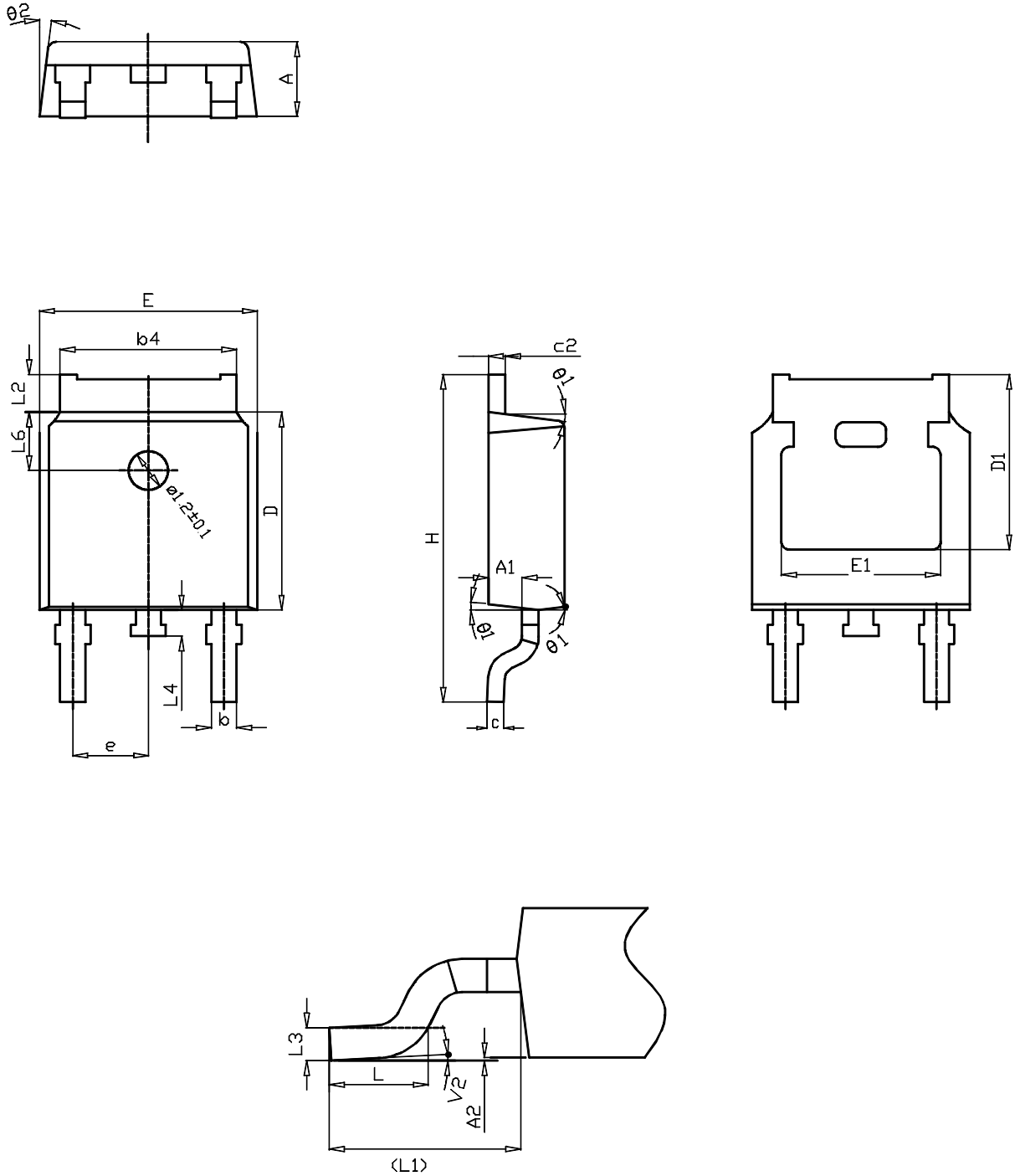
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**Table 9. DPAK (TO-252) type A mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1	4.95	5.10	5.25
E	6.40		6.60
E1	4.60	4.70	4.80
e	2.159	2.286	2.413
e1	4.445	4.572	4.699
H	9.35		10.10
L	1.00		1.50
(L1)	2.60	2.80	3.00
L2	0.65	0.80	0.95
L4	0.60		1.00
R		0.20	
V2	0°		8°

## 4.2 DPAK (TO-252) type C package information

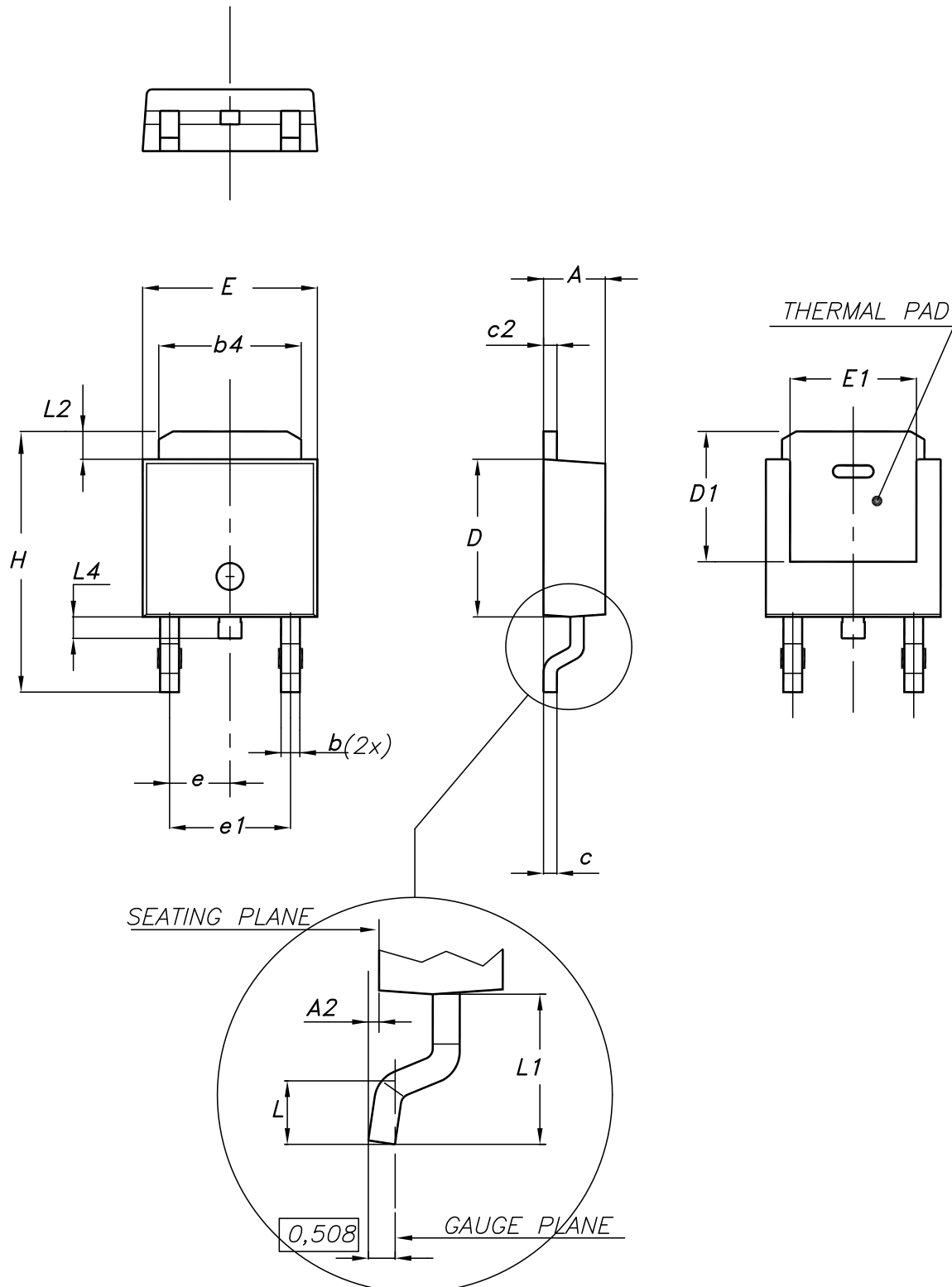
Figure 23. DPAK (TO-252) type C package outline



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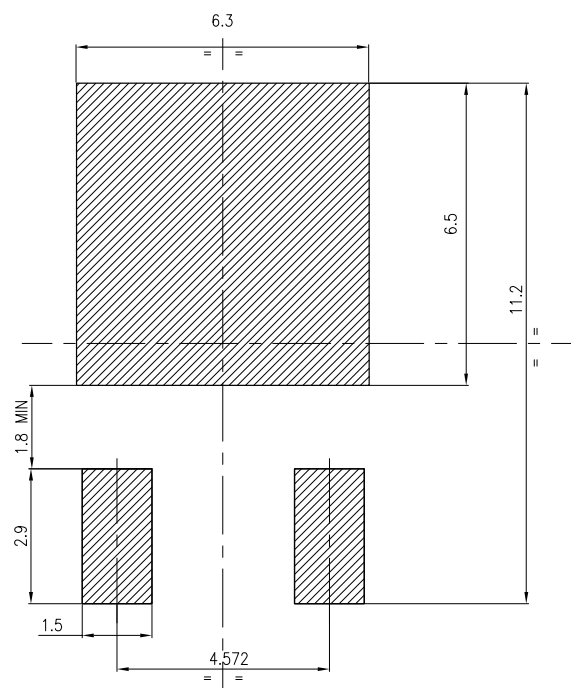
**Table 10. DPAK (TO-252) type C mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.38
A1	0.90	1.01	1.10
A2	0.00		0.10
b	0.72		0.85
b4	5.13	5.33	5.46
c	0.47		0.60
c2	0.47		0.60
D	6.00	6.10	6.20
D1	5.25		
E	6.50	6.60	6.70
E1	4.70		
e	2.186	2.286	2.386
H	9.80	10.10	10.40
L	1.40	1.50	1.70
L1	2.90 REF		
L2	0.90		1.25
L3	0.51 BSC		
L4	0.60	0.80	1.00
L6	1.80 BSC		
θ1	5°	7°	9°
θ2	5°	7°	9°
V2	0°		8°

**4.3 DPAK (TO-252) type E package information**
**Figure 24. DPAK (TO-252) type E package outline**


**Table 11. DPAK (TO-252) type E mechanical data**

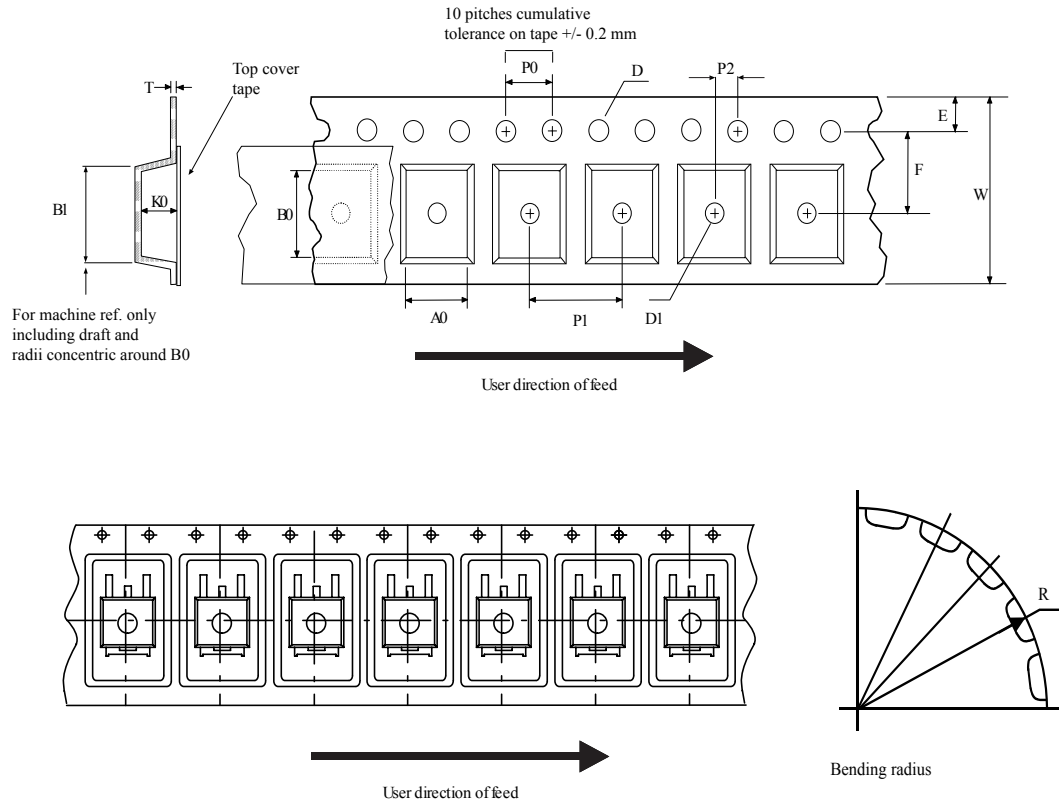
Dim.	mm		
	Min.	Typ.	Max.
A	2.18		2.39
A2			0.13
b	0.65		0.884
b4	4.95		5.46
c	0.46		0.61
c2	0.46		0.60
D	5.97		6.22
D1	5.21		
E	6.35		6.73
E1	4.32		
e		2.286	
e1		4.572	
H	9.94		10.34
L	1.50		1.78
L1		2.74	
L2	0.89		1.27
L4			1.02

**Figure 25. DPAK (TO-252) recommended footprint (dimensions are in mm)**


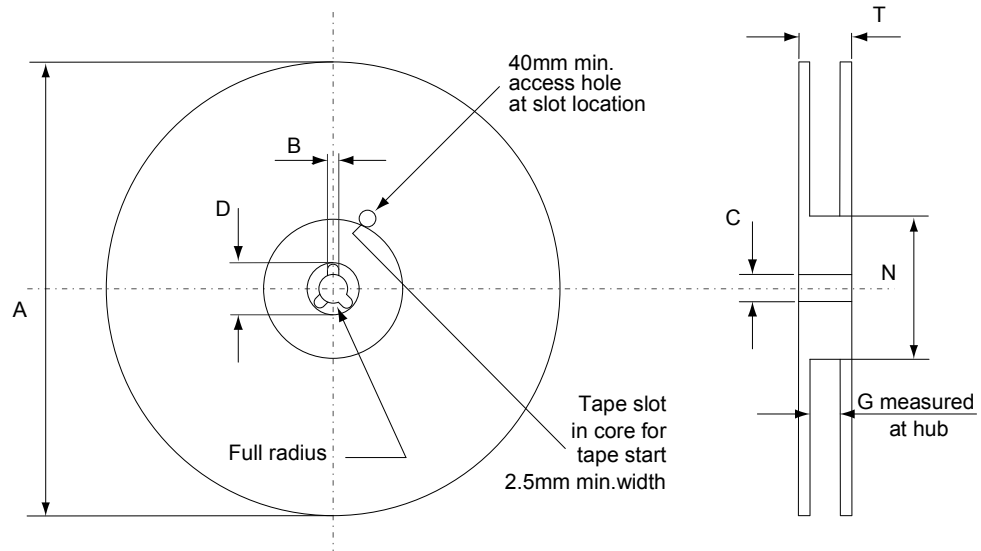
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### 4.4 DPAK (TO-252) packing information

Figure 26. DPAK (TO-252) tape outline



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**Figure 27. DPAK (TO-252) reel outline**


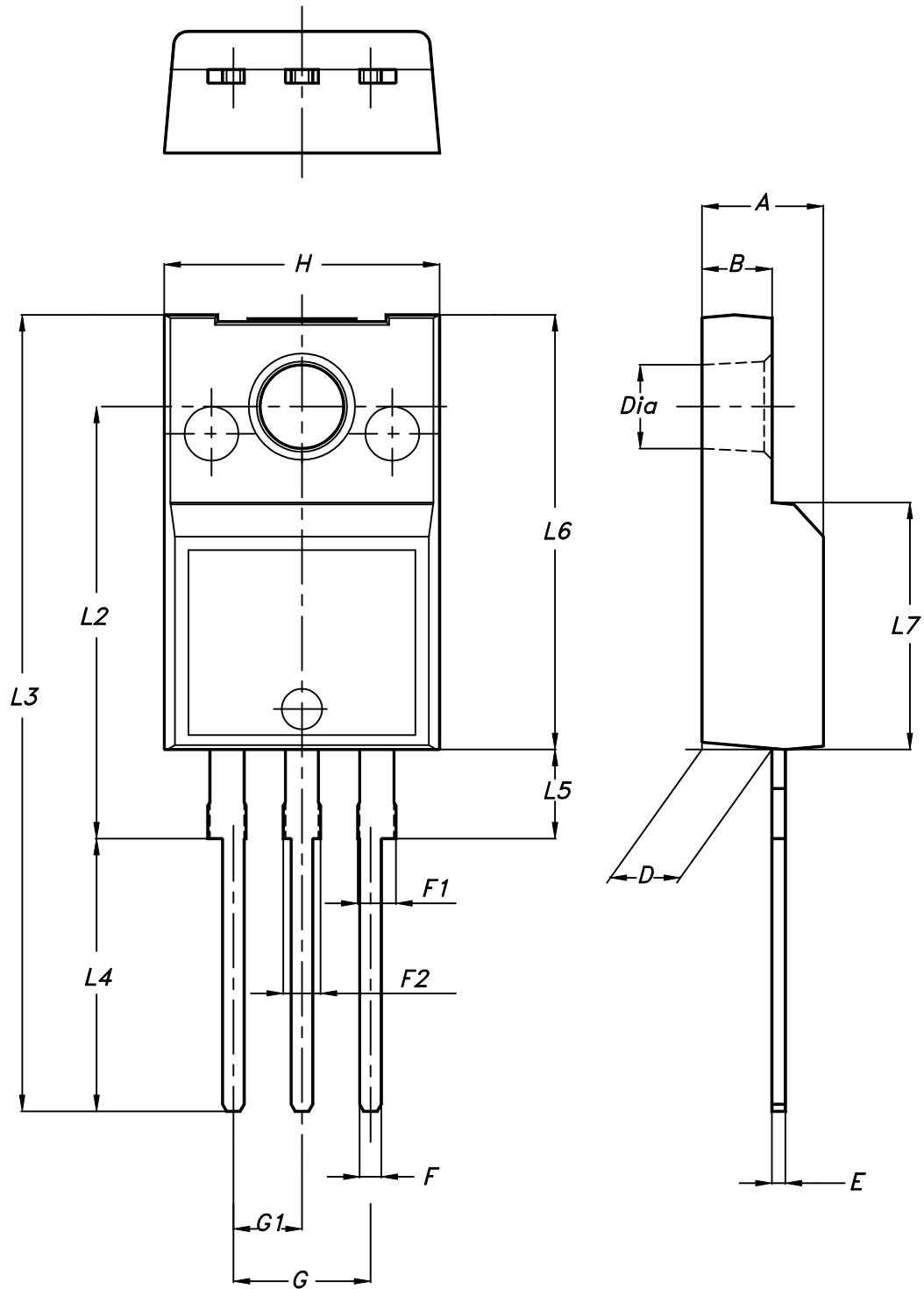
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**Table 12. DPAK (TO-252) tape and reel mechanical data**

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

### 4.5 TO-220FP package information

Figure 28. TO-220FP package outline



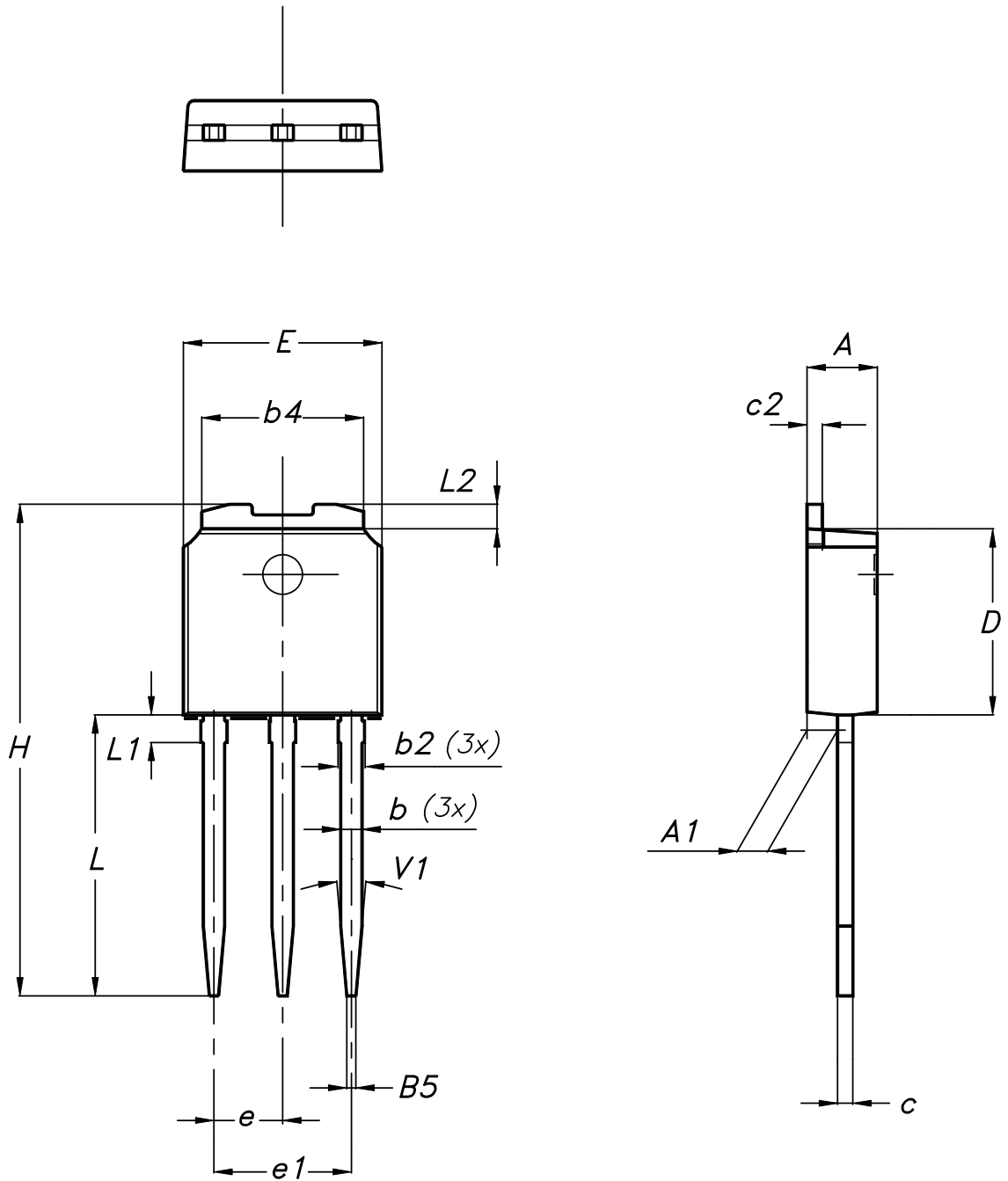
7012510\_Rev\_12\_B

**Table 13. TO-220FP package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	4.4		4.6
B	2.5		2.7
D	2.5		2.75
E	0.45		0.7
F	0.75		1
F1	1.15		1.70
F2	1.15		1.70
G	4.95		5.2
G1	2.4		2.7
H	10		10.4
L2		16	
L3	28.6		30.6
L4	9.8		10.6
L5	2.9		3.6
L6	15.9		16.4
L7	9		9.3
Dia	3		3.2

#### 4.6 IPAK (TO-251) type A package information

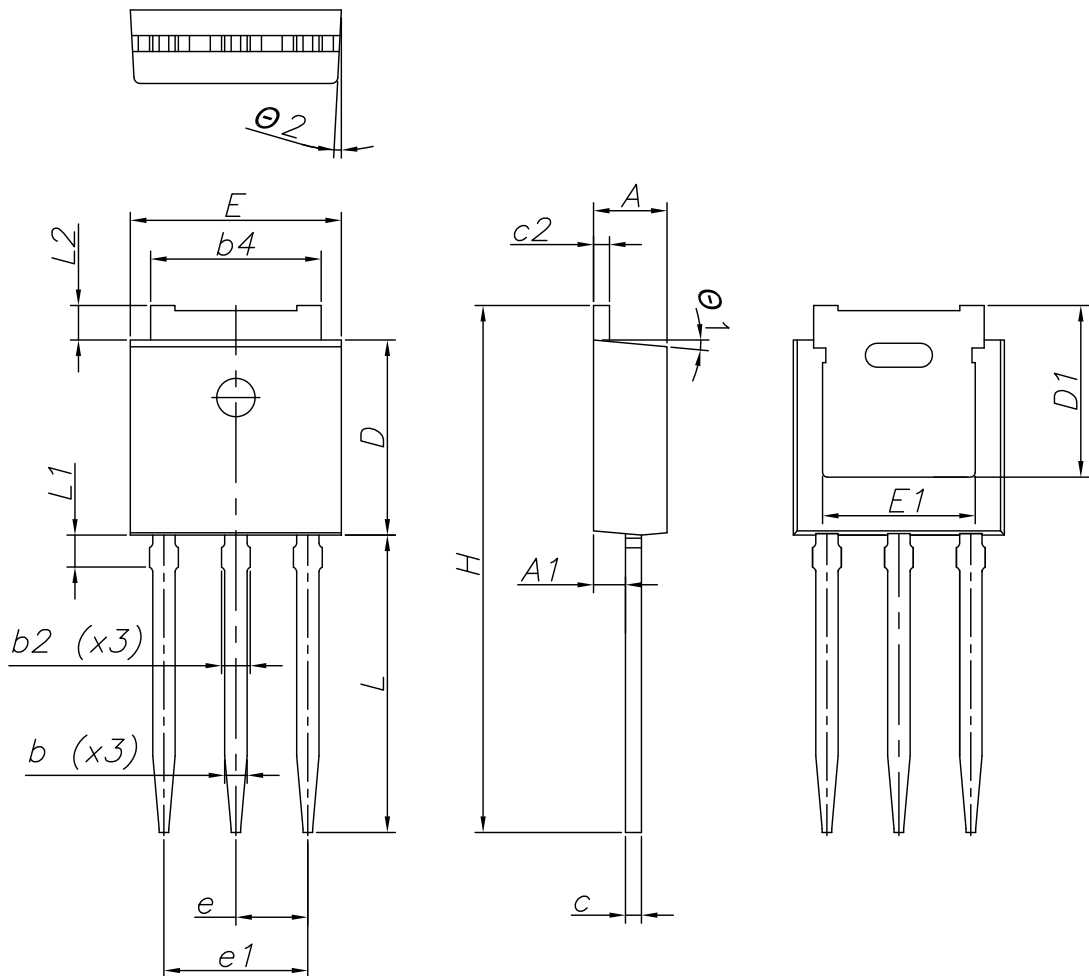
Figure 29. IPAK (TO-251) type A package outline



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**Table 14. IPAK (TO-251) type A package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
b	0.64		0.90
b2			0.95
b4	5.20		5.40
B5		0.30	
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
E	6.40		6.60
e		2.28	
e1	4.40		4.60
H		16.10	
L	9.00		9.40
L1	0.80		1.20
L2		0.80	1.00
V1		10°	

**4.7 IPAK (TO-251) type C package information**
**Figure 30. IPAK (TO-251) type C package outline**


0068771\_IK\_typeC\_rev14

**Table 15. IPAK (TO-251) type C package mechanical data**

Dim.	mm		
	Min.	Typ.	Max.
A	2.20	2.30	2.35
A1	0.90	1.00	1.10
b	0.66		0.79
b2			0.90
b4	5.23	5.33	5.43
c	0.46		0.59
c2	0.46		0.59
D	6.00	6.10	6.20
D1	5.20	5.37	5.55
E	6.50	6.60	6.70
E1	4.60	4.78	4.95
e	2.20	2.25	2.30
e1	4.40	4.50	4.60
H	16.18	16.48	16.78
L	9.00	9.30	9.60
L1	0.80	1.00	1.20
L2	0.90	1.08	1.25
θ1	3°	5°	7°
θ2	1°	3°	5°

## 5 Ordering information

Table 16. Order codes

Order code	Marking	Package	Packing
STD2N62K3	2N62K3	DPAK	Tape and reel
STF2N62K3		TO-220FP	Tube
STU2N62K3		IPAK	

## Revision history

**Table 17. Document revision history**

Date	Version	Changes
31-May-2011	1	First release
20-Mar-2012	2	Added new package: D <sup>2</sup> PAK – Table 1: Device summary, Section 4: Package mechanical data and Section 5: Packaging mechanical data have been modified. Minor text changes.
04-Jun-2018	3	The part numbers STB2N62K3 and STP2N62K3 have been moved to a separate datasheet. Removed maturity status indication from cover page. The document status is production data. Updated title and features in cover page. Updated <a href="#">Section 1 Electrical ratings</a> , <a href="#">Section 2 Electrical characteristics</a> , <a href="#">Section 2.1 Electrical characteristics curves</a> and <a href="#">Section 4 Package information</a> . Minor text changes.

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