THE DATASHEET OF

LM2611BMF/NOPB

LM2611 1.4-MHz Cuk Converter

1 Features

- 1.4-MHz Switching Frequency
- Low $R_{DS(ON)}$ DMOS FET
- 1-mVp-p Output Ripple
- −5 V at 300 mA From 5-V Input
- Better Regulation Than a Charge Pump
- Uses Tiny Capacitors and Inductors
- Wide Input Range: 2.7 V to 14 V
- Low Shutdown Current: <1 µA
- 5-Pin SOT-23 Package

2 Applications

- MR Head Bias
- Digital Camera CCD Bias
- LCD Bias
- GaAs FET Bias
- Positive to Negative Conversion

3 Description

The LM2611 is a current mode, PWM inverting switching regulator. Operating from a 2.7-V to 4-V supply, it is capable of producing a regulated negative output voltage of up to −(36 $V_{IN(MAX)}$). The LM2611 utilizes an input and output inductor, which enables low voltage ripple and RMS current on both the input and the output. With a switching frequency of 1.4 MHz, the inductors and output capacitor can be physically small and low cost. High efficiency is achieved through the use of a low $R_{DS(ON)}$ FET.

The LM2611 features a shutdown pin, which can be activated when the part is not needed to lower the Iq and save battery life. A negative feedback (NFB) pin provides a simple method of setting the output voltage, using just two resistors. Cycle-by-cycle current limiting and internal compensation further simplify the use of the LM2611.

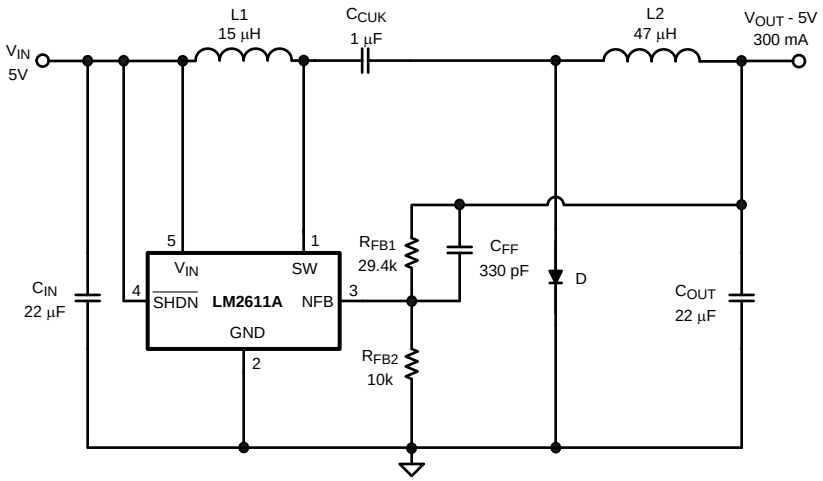
The LM2611 is available as a small 5-pin, SOT-23 package and comes in two grades. Grade A has a 1.2-A current limit and 0.5-Ω $R_{DS(ON)}$, and Grade B has a 0.9-A current limit and 0.7-Ω $R_{DS(ON)}$.

Device Information(1)

PART NUMBER	PACKAGE	BODY SIZE (NOM)
LM2611	SOT-23 (5)	1.60 mm × 2.90 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Typical Application Circuit



C_{IN}: TAIYO YUDEN X5R JMK325BJ226MM
C_{CUK}: TAIYO YUDEN X5R EMK316BJ105MF
C_{OUT}: TAIYO YUDEN X5R JMK325BJ226MM
D: ON SEMICONDUCTOR MBR0520
L1: SUMIDA CR32-150
L2: SUMIDA CR32-470

Table of Contents

4 Revision History

NOTE: Page numbers for previous revisions may differ from page numbers in the current version.

Changes from Revision I (April 2013) to Revision J **Page**

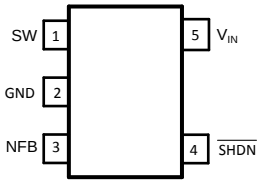
- Added *ESD Ratings* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section. ... 1

Changes from Revision H (April 2013) to Revision I **Page**

- Changed layout of National Data Sheet to TI format ... 19

5 Pin Configuration and Functions

DBV Package
5-Pin SOT-23
Top View



Pin Functions

PIN		TYPE(1)	DESCRIPTION
NO.	NAME		
1	SW	A	Drain of internal switch. Connect at the node of the input inductor and Cuk capacitor.
2	GND	GND	Analog and power ground.
3	NFB	A	Negative feedback. Connect to output via external resistor divider to set output voltage.
4	$\overline{SHDN}$	I	Shutdown control input. V_{IN} = Device on. Ground = Device in shutdown.
5	V_{IN}	PWR	Analog and power input. Filter out high frequency noise with a 0.1-µF ceramic capacitor placed close to the pin.

(1) A = Analog, I = Input, GND = Ground, PWR = Power

6 Specifications

6.1 Absolute Maximum Ratings

over operating free-air temperature range (unless otherwise noted)(1)

	MIN	MAX	UNIT
Input voltage, V_{IN}		14.5	V
SW voltage	–0.4	36	V
NFB voltage	–6	0.4	V
$\overline{SHDN}$ voltage	–0.4	14.5	V
Maximum junction temperature		125	°C
Power dissipation (2)	Internally limited		
Lead temperature		300	°C
Storage temperature, T_{stg}	−65	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, which do not imply functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions*. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_{J(MAX)}$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the *Electrical Characteristics* table for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using: P_D (MAX) = ($T_{J(MAX)}$ − T_A)/θ_{JA}. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human-body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)(2)	±2000	V
		Machine Model (MM)(3)	±200	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) The human body model is a 100-pF capacitor discharged through a 1.5-kΩ resistor into each pin.
(3) The machine model is a 200-pF capacitor discharged directly into each pin.

6.3 Recommended Operating Conditions

	MIN	NOM	MAX	UNIT
Supply voltage	2.7		14	V
Operating junction temperature, T_J	−40		125	°C

6.4 Thermal Information

THERMAL METRIC[1]		LM2611 DBV (SOT-23) 5 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	163.5	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	115.2	°C/W
$R_{\theta JB}$	Junction-to-board thermal resistance	27.4	°C/W
ψ_{JT}	Junction-to-top characterization parameter	12.9	°C/W
ψ_{JB}	Junction-to-board characterization parameter	26.9	°C/W
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	n/a	°C/W

(1) For more information about traditional and new thermal metrics, see the *Semiconductor and IC Package Thermal Metrics* application report, SPRA953.

6.5 Electrical Characteristics

Specifications in standard type face are for T_J = 25°C, unless otherwise specified. V_{IN} = 5 V and I_L = 0 A, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
V_{IN}	Input voltage	T_J = −40°C to +85°C	2.7		14	V
I_{SW}	Switch current limit	Grade A		1.2		A
		Grade A; T_J = −40°C to +85°C	1		2	
		Grade B		0.9		
		Grade B; T_J = −40°C to +85°C	0.7			
R_{DSON}	Switch ON resistance	Grade A		0.5	0.65	Ω
		Grade B		0.7	0.9	
$SHDN_{TH}$	Shutdown threshold	Device enabled; T_J = −40°C to +85°C	1.5			V
		Device disabled; T_J = −40°C to +85°C			0.5	
I_{SHDN}	Shutdown pin bias current	V_{SHDN} = 0 V		0		µA
		V_{SHDN} = 5 V		0		
		V_{SHDN} = 5 V; T_J = −40°C to +85°C			1	
NFB	Negative feedback reference	V_{IN} = 3 V		−1.23		V
		V_{IN} = 3 V; T_J = −40°C to +85°C	−1.205		−1.255	
I_{NFB}	NFB pin bias current	V_{NFB} =−1.23 V		−4.7		µA
		V_{NFB} =−1.23 V; T_J = −40°C to +85°C	−2.7		−6.7	
I_q	Quiescent current	V_{SHDN} = 5 V, Switching		1.8		mA
		V_{SHDN} = 5 V, Switching; T_J = −40°C to +85°C			3.5	
		V_{SHDN} = 5 V, Not Switching		270		µA
		V_{SHDN} = 5 V, Not Switching; T_J = −40°C to +85°C			500	
		V_{SHDN} = 0 V		0.024		µA
		V_{SHDN} = 0 V; T_J = −40°C to +85°C			1	
$\%V_{OUT}/\Delta V_{IN}$	Reference line regulation	2.7 V ≤ V_{IN} ≤ 14 V		0.02		%/V

(1) All limits are specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% tested through statistical analysis. All limits at temperature extremes via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the expected value of the parameter.

Electrical Characteristics (continued)

Specifications in standard type face are for T_J = 25°C, unless otherwise specified. V_{IN} = 5 V and I_L = 0 A, unless otherwise specified.

PARAMETER		TEST CONDITIONS	MIN (1)	TYP (2)	MAX (1)	UNIT
f_S	Switching frequency	T_J = 25°C		1.4		MHz
		T_J = −40°C to +85°C	1		1.8	
D_{MAX}	Maximum duty cycle	T_J = 25°C		88%		
		T_J = −40°C to +85°C	82%			
I_L	Switch leakage	V_{SW} = 5 V, Not Switching			1	µA

6.6 Typical Characteristics

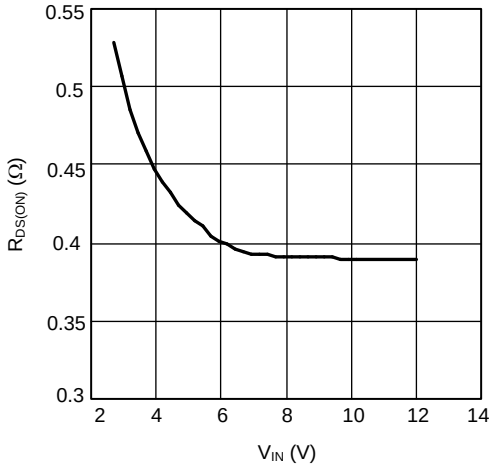
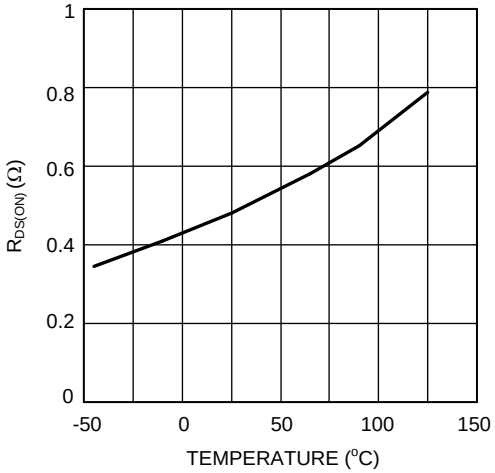


Figure 1. $R_{DS(ON)}$ vs V_{IN}



V_{IN} = 5 V

Figure 2. $R_{DS(ON)}$ vs Ambient Temperature

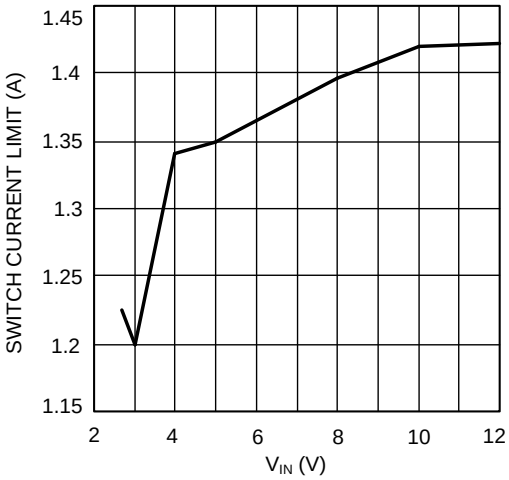
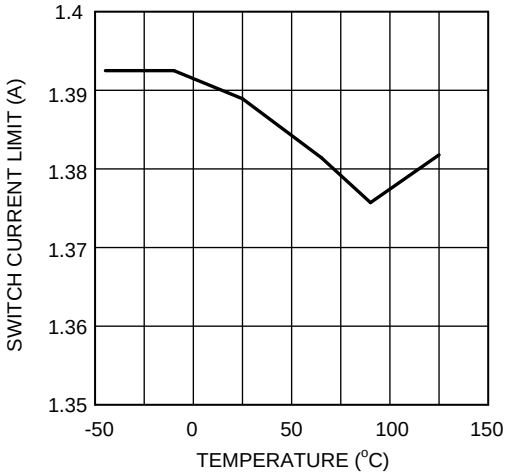


Figure 3. Switch Current Limit vs V_{IN}



V_{IN} = 5 V

Figure 4. Switch Current Limit vs Ambient Temperature

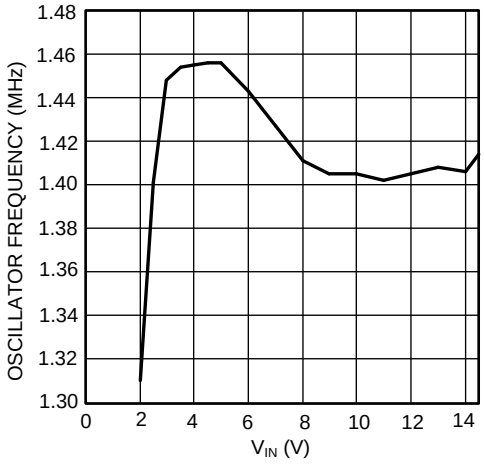
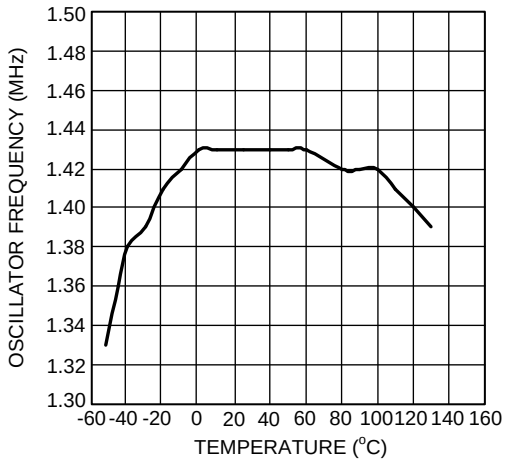


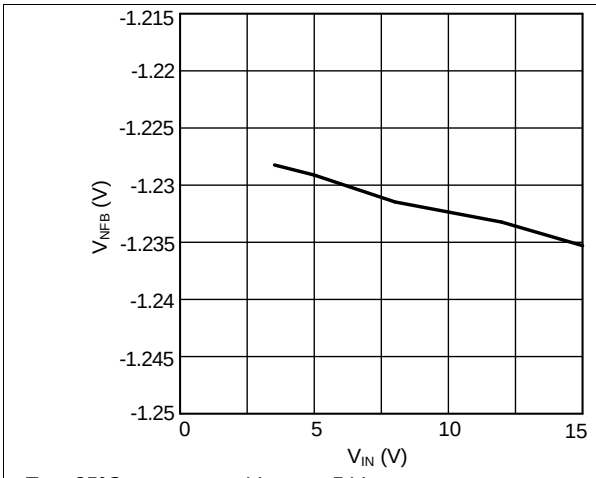
Figure 5. Oscillator Frequency vs V_{IN}



V_{IN} = 5 V

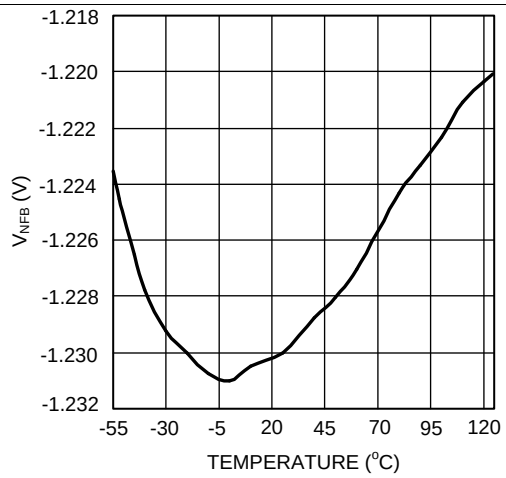
Figure 6. Oscillator Frequency vs Ambient Temperature

Typical Characteristics (continued)



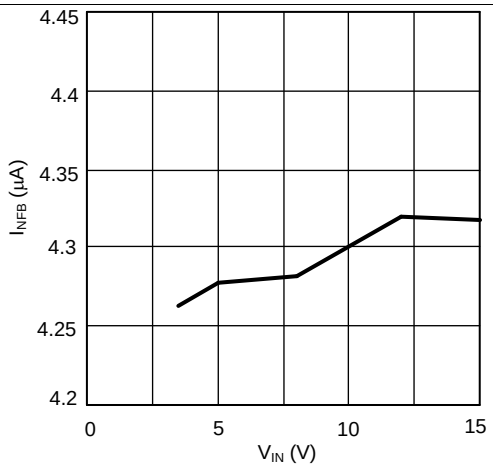
T_A = 25°C V_{OUT} = −5 V

Figure 7. V_{NFB} vs V_{IN}



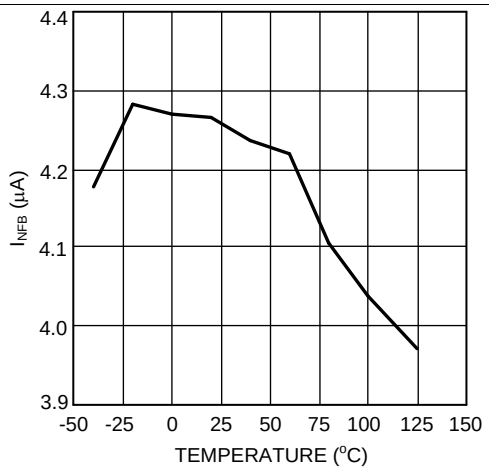
V_{IN} = 5 V

Figure 8. V_{NFB} vs Ambient Temperature



T_A = 25°C V_{OUT} = −5 V

Figure 9. I_{NFB} vs V_{IN}



V_{IN} = 3.5 V V_{OUT} = −5 V

Figure 10. I_{NFB} vs Ambient Temperature

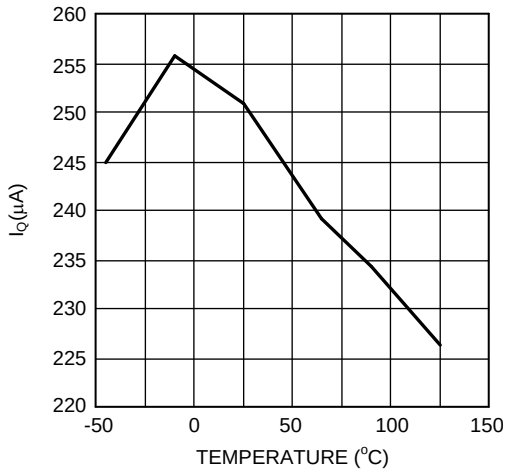
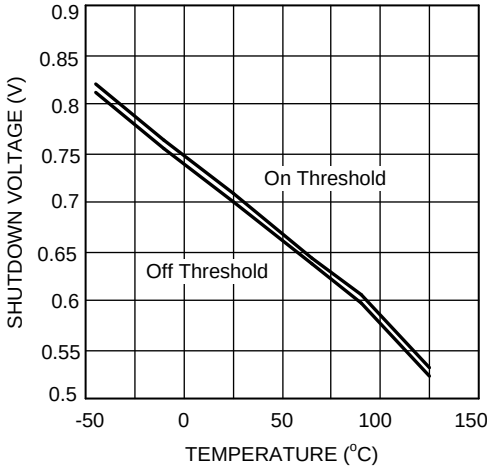


Figure 11. I_q vs Ambient Temperature (No Load)



V_{IN} = 5 V

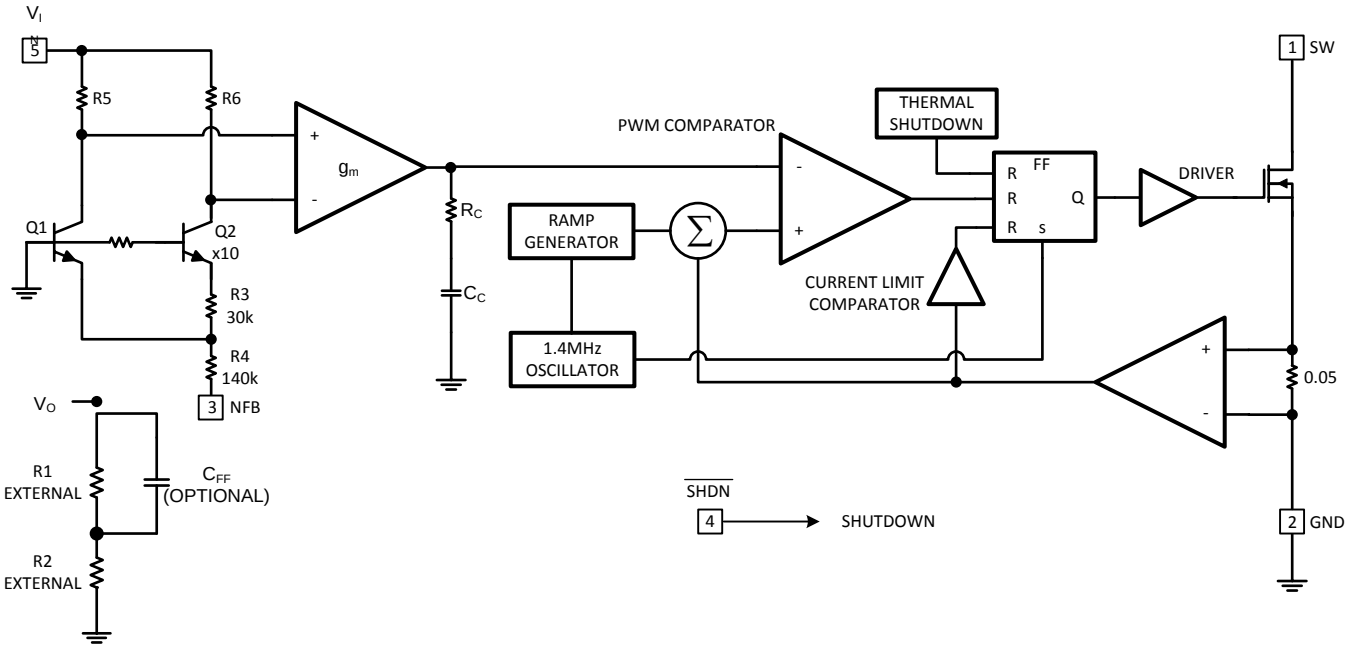
Figure 12. $V_{SHUTDOWN}$ vs Ambient Temperature

7 Detailed Description

7.1 Overview

The LM2611 consists of a current mode controller with an integrated primary switch and integrated current sensing circuitry. The feedback is connected to the internal error amplifier and a type II/III internal compensation scheme is used. A ramp generator provides some slope compensation to the system. $\overline{SHDN}$ pin is a logic input designed to shut down the converter.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Cuk Converter

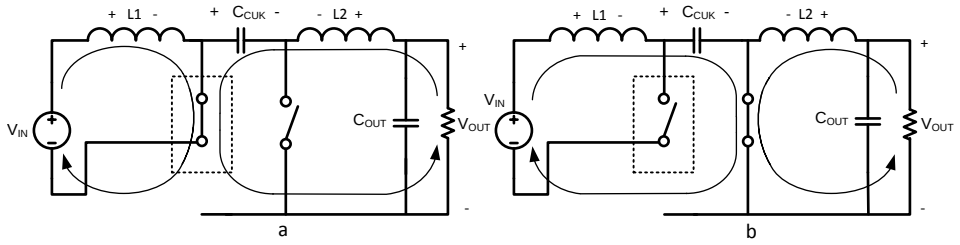


Figure 13. Operating Cycles of a Cuk Converter

The LM2611 is a current mode, fixed frequency PWM switching regulator with a −1.23-V reference that makes it ideal for use in a Cuk converter. The Cuk converter inverts the input and can step up or step down the absolute value. Using inductors on both the input and output, the Cuk converter produces very little input and output current ripple. This is a significant advantage over other inverting topologies such as the buck-boost and flyback.

The operating states of the Cuk converter are shown in Figure 13. During the first cycle, the transistor switch is closed and the diode is open. L1 is charged by the source and L2 is charged by C_{CUK}, while the output current is provided by L2. In the second cycle, L1 charges C_{CUK} and L2 discharges through the load. By applying the volt-second balance to either of the inductors, use Equation 1 to determine the relationship of V_{OUT} to the duty cycle (D).

Feature Description (continued)

$$V_{OUT} = -V_{IN} \frac{D}{1-D} \quad (1)$$

The following sections review the steady-state design of the LM2611 Cuk converter.

7.3.2 Output and Input Inductor

Figure 14 and Figure 15 show the steady-state voltage and current waveforms for L1 and L2, respectively. Referring to Figure 13 (a), when the switch is closed, V_{IN} is applied across L1. In the next cycle, the switch opens and the diode becomes forward biased, and V_{OUT} is applied across L1 (the voltage across C_{CUK} is $V_{IN} - V_{OUT}$.)

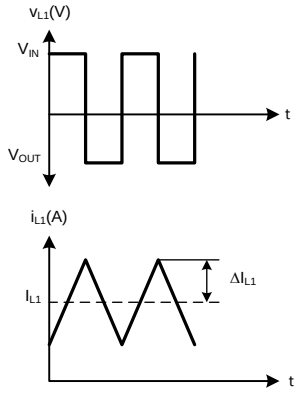
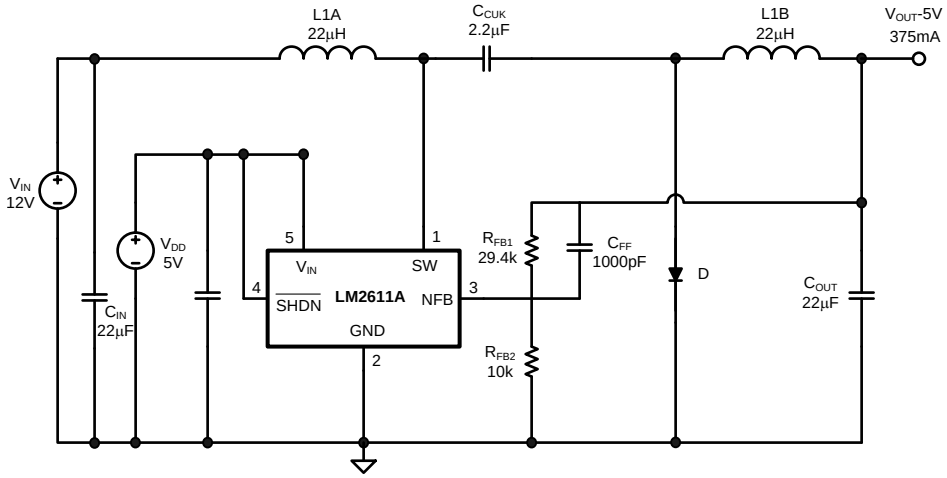


Figure 14. Voltage and Current Waveforms in Inductor L1 of a Cuk Converter

The voltage and current waveforms of inductor L2 are shown in Figure 15. During the first cycle of operation, when the switch is closed, V_{IN} is applied across L2. When the switch opens, V_{OUT} is applied across L2.



CIN: VISHAY/SPRAGUE 595D226X0020C2T
CCUK: TAIYO YUDEN X5R LMK212BJ105MG
COUT: TAIYO YUDEN X5R JMK325BJ226MM
D: ON SEMICONDUCTOR MBR0520
L1: SUMIDA CLS62-220 or MURATA LZH3C220 (UNCOUPLED)

Figure 15. Schematic of the Cuk Converter Using LM2611

Equation 2 to Equation 5 define the values given in Figure 14 and Figure 15:

$$I_{L2} = I_{OUT} \quad (2)$$

Feature Description (continued)

$$\Delta i_{L2} = \frac{V_{IN} \times D \times T_S}{2 \times L_2} \quad (3)$$

$$I_{L1} = \frac{D}{1\text{-}D} I_{L2} = \frac{D}{1\text{-}D} I_{OUT} \quad (4)$$

$$\Delta i_{L1} = \frac{V_{IN} \times D \times T_S}{2 \times L_1} \quad (5)$$

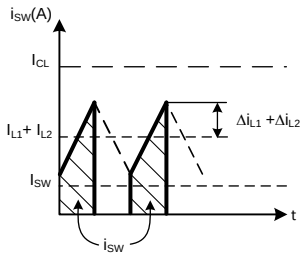
Use these equations to choose correct core sizes for the inductors. The design of the LM2611's internal compensation assumes L1 and L2 are equal to 10 to 22 µH, thus TI recommends staying within this range.

7.3.3 Switch Current Limit

The LM2611 incorporates a separate current limit comparator, making current limit independent of any other variables. The current limit comparator measures the switch current versus a reference that represents current limit. If at any time the switch current surpasses the current limit, the switch opens until the next switching period. To determine the maximum load for a given set of conditions, both the input and output inductor currents must be considered. The switch current is equal to $i_{L1} + i_{L2}$, and is drawn in Figure 16. In summary, Equation 6 shows:

$$i_{SW(PEAK)} = i_{L1} + i_{L2} = I_{L1} + I_{L2} + \Delta i_{L1} + \Delta i_{L2}$$
$$= I_{OUT} \times \left(1 + \frac{D}{1\text{-}D}\right) + \frac{V_{IN} \times D \times T_S}{2} \times \left(\frac{1}{L_1} + \frac{1}{L_2}\right) \quad (6)$$

$I_{SW(PEAK)}$ must be less than the current limit (1.2 A typical), but will also be limited by the thermal resistivity of the LM2611 device's 5-pin, SOT-23 package (θ_{JA} = 265°C/W).



The peak value is equal to the sum of the average currents through L1 and L2 and the average-to-peak current ripples through L1 and L2.

Figure 16. Switch Current Waveform in a Cuk Converter.

7.3.4 Input Capacitor

The input current waveform to a Cuk converter is continuous and triangular, as shown in Figure 14. The input inductor insures that the input capacitor sees fairly low ripple currents. However, as the input inductor gets smaller, the input ripple goes up. The RMS current in the input capacitor is shown in Equation 7.

$$I_{CIN(RMS)} = \frac{1}{2\sqrt{3}} \frac{V_{IN}}{f_s L_1 \left(\frac{V_i}{|V_o|} + 1\right)} \quad (7)$$

The input capacitor should be capable of handling the RMS current. Although the input capacitor is not so critical in a Cuk converter, a 10-µF or higher value good quality capacitor prevents any impedance interactions with the input supply. TI recommends connecting a 0.1-µF or 1-µF ceramic bypass capacitor on the V_{IN} pin (pin 5) of the IC. This capacitor must be connected very close to pin 5 (within 0.2 inches).

Feature Description (continued)

7.3.5 Output Capacitor

Like the input current, the output current is also continuous, triangular, and has low ripple (see I_{L2} in Figure 15). The output capacitor must be rated to handle its RMS current:

$$I_{COUT(RMS)} = \frac{\Delta i_{L2}}{\sqrt{3}} = \frac{1}{2\sqrt{3}} \frac{V_{IN}}{f_s L_2 \left(\frac{V_i}{|V_o|} + 1 \right)} \quad (8)$$

For example, $I_{COUT(RMS)}$ can range from 30 mA to 180 mA with 10 µH ≤ $L_{1,2}$ ≤ 22 µH, −10 V ≤ V_{OUT} ≤ −3.3 V, and 2.7 V ≤ V_{IN} ≤ 30 V (V_{IN} may be 30 V if using separate power and analog supplies, see *Split Supply Operation* in the *Typical Application* section). The worst case conditions are with $L_{1,2}$, $V_{OUT(MAX)}$, and $V_{IN(MAX)}$. Many capacitor technologies will provide this level of RMS current, but ceramic capacitors are ideally suited for the LM2611. Ceramic capacitors provide a good combination of capacitance and equivalent series resistance (ESR) to keep the zero formed by the capacitance and ESR at high frequencies. Use Equation 9 to calculate the ESR zero.

$$f_{ESR} = \frac{1}{2\pi C_{OUT} ESR} (Hz) \quad (9)$$

A general rule of thumb is to keep f_{ESR} > 80 kHz for LM2611 Cuk designs. Low ESR tantalum capacitors will usually be rated for at least 180 mA in a voltage rating of 10 V or above. However the ESR in a tantalum capacitor (even in a low ESR tantalum capacitor) is much higher than in a ceramic capacitor and could place f_{ESR} low enough to cause the LM2611 to become unstable.

7.3.6 Improving Transient Response and Compensation

The compensator in the LM2611 is internal. However, a zero-pole pair can be added to the open-loop frequency response by inserting a feed-forward capacitor, C_{FF}, in parallel to the top feedback resistor (R_{FB1}). Phase margin and bandwidth can be improved with the added zero-pole pair. This in turn improves the transient response to a step load change (see Figure 17 and Figure 18). The position of the zero-pole pair is a function of the feedback resistors and the capacitor value:

$$\omega_Z = \frac{1}{C_{FF} R_{FB1}} (rad/s) \quad (10)$$

$$\omega_p = \frac{1}{C_{FF} R_{FB1}} \left(1 + \frac{R_{FB1}}{R_{FB2}} \right) (rad/s) \quad (11)$$

The optimal position for this zero-pole pair will vary with circuit parameters such as D, I_{OUT}, C_{OUT}, L1, L2, and C_{CUK}. For most cases, the value for the zero frequency is between 5 kHz to 20 kHz. Notice how the pole position, ω_p, is dependant on the feedback resistors R_{FB1} and R_{FB2}, and therefore also dependant on the output voltage. As the output voltage becomes closer to −1.26 V, the pole moves towards the zero, tending to cancel it out. If the absolute magnitude of the output voltage is less than 3.3 V, adding the zero-pole pair will not have much effect on the response.

Feature Description (continued)

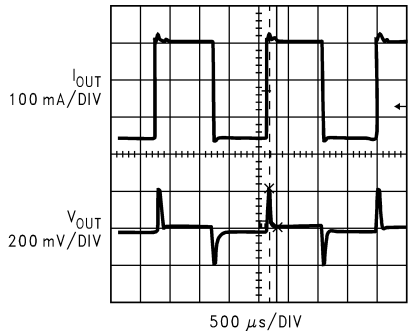


Figure 17. 130-mA to 400-mA Transient Response of the Circuit in Figure 24 With C_{FF}= 1 nF

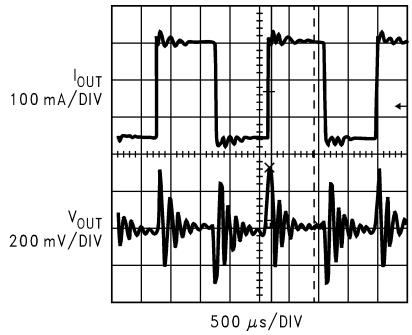


Figure 18. 130-mA to 400-mA Transient Response of the Circuit in Figure 24 With C_{FF} Disconnected

7.4 Device Functional Modes

7.4.1 Hysteretic Mode

As the output current decreases, the energy stored in the Cuk capacitor eventually exceeds the energy required by the load. The excess energy is absorbed by the output capacitor, causing the output voltage to increase out of regulation. The LM2611 detects when this happens and enters a pulse-skipping, or hysteretic mode. In pulse-skipping mode, the output voltage increases as illustrated in Figure 20 as opposed to the regular PWM operation shown in Figure 19. Figure 19 shows the LM2611 in PWM Mode with very-low ripple. Figure 20 shows the LM2611 in pulse-skipping mode at low loads. In this mode, the output ripple increases slightly.

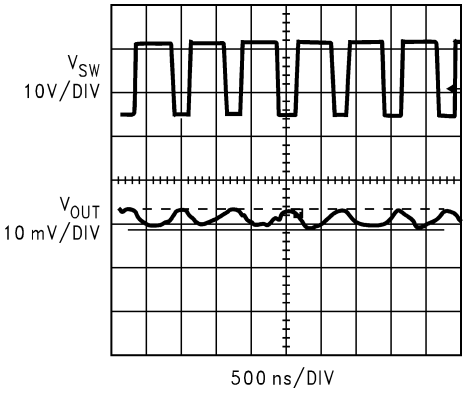


Figure 19. PWM Mode

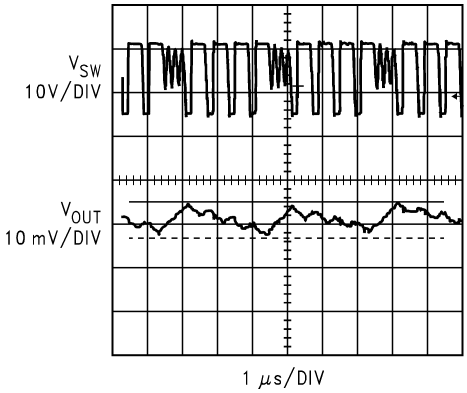


Figure 20. Pulse-Skipping Mode

7.4.1.1 Thermal Shutdown

If the junction temperature of the LM2611 exceeds 163°C, the device enters thermal shutdown. In thermal shutdown, the part deactivates the driver and the switch turns off. The switch remains off until the junction temperature drops to 155°C, at which point the part begins switching again. It will typically take 10 ms for the junction temperature to drop from 163°C to 155°C with the switch off.

8 Application and Implementation

NOTE

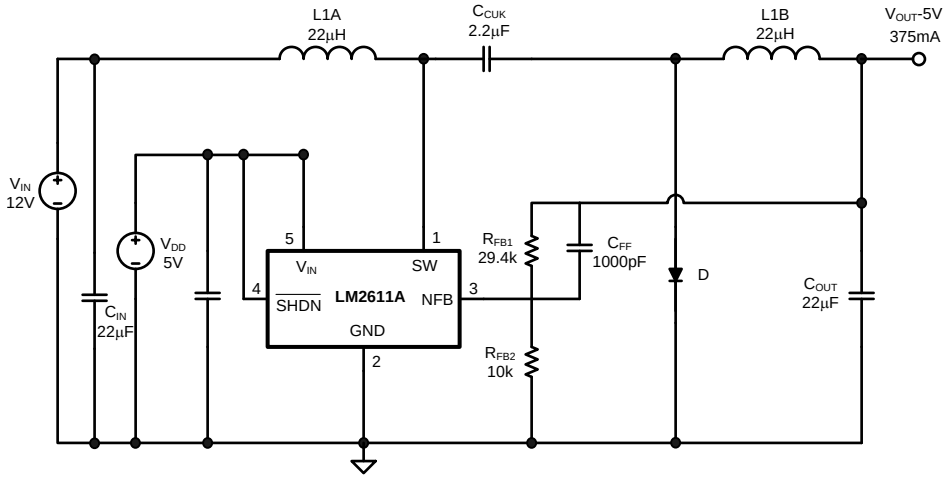
Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The LM2611 is a Cuk controller with an integrated switch. The following section provides an approach to sizing the components for the target application and shows some typical examples of applications to help the designer.

8.2 Typical Application

8.2.1 Cuk Converter With Integrated Switch



CIN: VISHAY/SPRAGUE 595D226X0020C2T
CCUK: TAIYO YUDEN X5R LMK212BJ105MG
COUT: TAIYO YUDEN X5R JMK325BJ226MM
D: ON SEMICONDUCTOR MBR0520
L1: SUMIDA CLS62-220 or MURATA LZH3C220 (UNCOUPLED)

Figure 21. Typical Cuk Converter Implementation Using LM26211

8.2.1.1 Design Requirements

The first variables needed are the output voltage and the input voltage range (min to max). The input voltage range ensures that the IC is suitable for the application and that the absolute maximum voltage are respected. The expected maximum output current is also needed to verify that the IC can deliver the required current.

8.2.1.2 Detailed Design Procedure

The first components to choose are the power inductors. Typically a smaller inductance yields a smaller solution footprint and lower cost but the higher ripple makes a smaller inductance not compatible with every application. Due to the internal compensation, TI recommends a 10-µH to 22-µH inductor. Try to choose the inductors so that the peak-to-peak ripple is lower than 0.3 A of the average current by using Equation 3 and Equation 5.

Using the maximum output current and the input voltage range, calculate the worst case peak current in the switch using Equation 6. If the peak current is above the peak current limit for this part, consider increasing the inductance and re-calculate. If the inductance is above 22 µH for each inductor, the designer will have to pay special attention to stability over the extended range of operation (it's always a good practice to do so even if the inductance is within the recommended range).

Using the desired output voltage, calculate the value of the feedback resistors. The reference voltage is 1.23 V. Resistors of 50 kΩ or less must be used due to the leakage at the NFB pin.

Typical Application (continued)

It is a good idea to add a placeholder for a small capacitor across the top feedback resistor to act as a feed-forward component to optimize transient response. Optimization of the feed-forward capacitor depends a lot on the specific parameters including the parasitic components associated with the capacitors. Experimentation is key to ensure ideal sizing of the capacitor (either using load transient response or a loop response analyzer). See *Improving Transient Response and Compensation* for details regarding the C_{FF} capacitor.

8.2.1.3 Application Curves

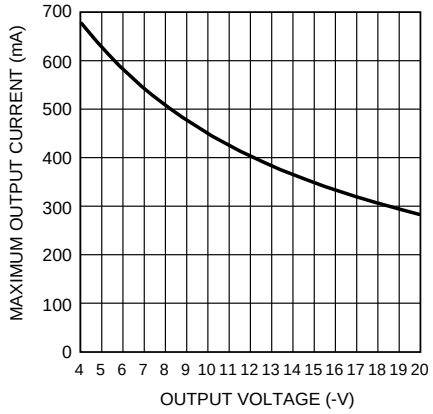


Figure 22. Maximum Output Current vs Output Voltage at V_{IN} = 12 V (L1 = L2 = 22 µH)

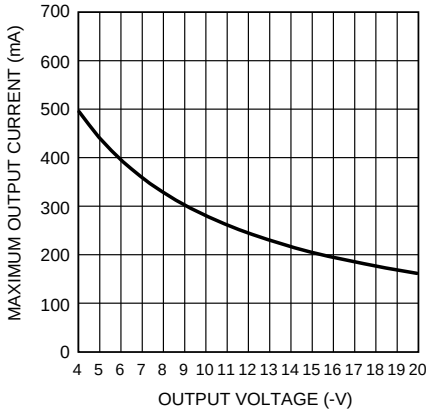
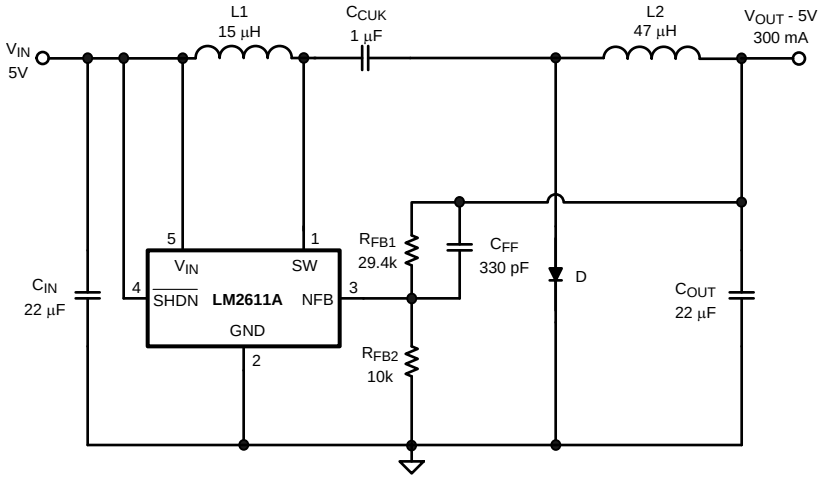


Figure 23. Maximum Output Current vs Output Voltage at V_{IN} = 5 V (L1 = L2 = 22 µH)

8.2.2 5-V to –5-V Inverting Converter



C_{IN}: TAIYO YUDEN X5R JMK325BJ226MM
C_{CUK}: TAIYO YUDEN X5R EMK316BJ105MF
C_{OUT}: TAIYO YUDEN X5R JMK325BJ226MM
D: ON SEMICONDUCTOR MBR0520
L1: SUMIDA CR32-150
L2: SUMIDA CR32-470

Figure 24. 5-V to –5-V Inverting Converter Schematic

8.2.2.1 Design Requirements

This design converts 5 V (V_{IN}) to –5 V (V_{OUT}). Adjust R_{FB2} to set a different output voltage.

Typical Application (continued)

8.2.2.2 Application Curves

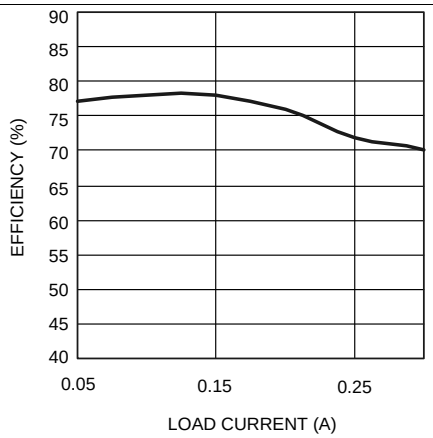


Figure 25. Efficiency vs Load Current

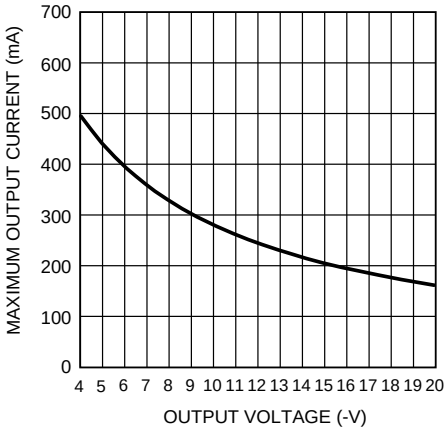
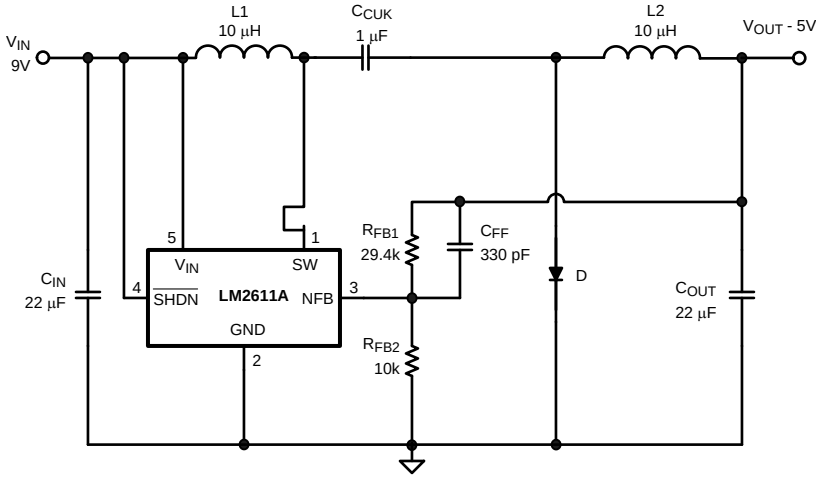


Figure 26. Maximum Output Current vs Output Voltage, 5 V to –5 V

8.2.3 9-V to –5-V Inverting Converter



CIN: TAIYO YUDEN X5R JMK325BJ226MM
CCUK: TAIYO YUDEN X5R EMK316BJ105MF
COUT: TAIYO YUDEN X5R JMK325BJ226MM
D: ON SEMICONDUCTOR MBR0520
L1: SUMIDA CR32-100
L2: SUMIDA CR32-100

Figure 27. 9-V to –5-V Inverting Converter Schematic

8.2.3.1 Design Requirements

This design converts 9 V (V_{IN}) to –5 V (V_{OUT}). Adjust R_{FB2} to set a different output voltage.

Typical Application (continued)

8.2.3.2 Application Curve

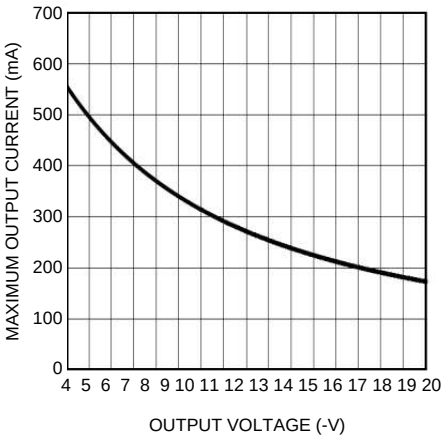
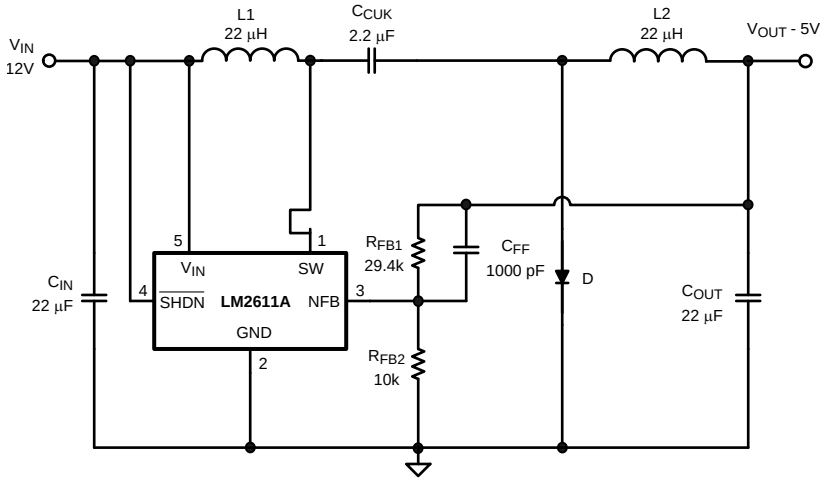


Figure 28. Maximum Output Current vs Output Voltage, 9 V to – 5 V

8.2.4 12-V to –5-V Inverting Converter



C_{IN}: TAIYO YUDEN X5R JMK325BJ226MM
C_{CUK}: TAIYO YUDEN X5R EMK316BJ225ML
C_{OUT}: TAIYO YUDEN X5R JMK325BJ226MM
D: ON SEMICONDUCTOR MBR0520
L1: SUMIDA CR32-220
L2: SUMIDA CR32-220

The maximum output current vs output voltage (adjust R_{FB2} to set a different output voltage) when the input voltage is 12 V.

Figure 29. 12-V to –5-V Inverting Converter Schematic

8.2.4.1 Design Requirements

This design converts 12 V (V_{IN}) to –5 V (V_{OUT}). Adjust R_{FB2} to set a different output voltage.

Typical Application (continued)

8.2.4.2 Application Curve

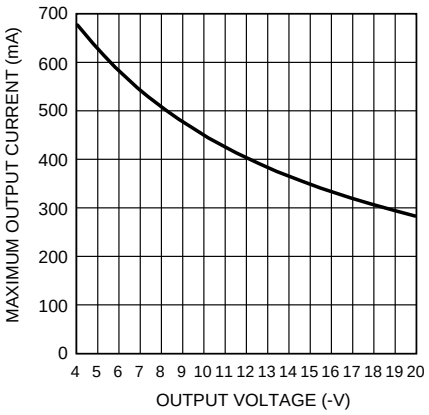


Figure 30. Maximum Output Current vs Output Voltage, 12 V to –5 V

8.2.5 LM2611 Operating With Separate Power and Biasing Supplies

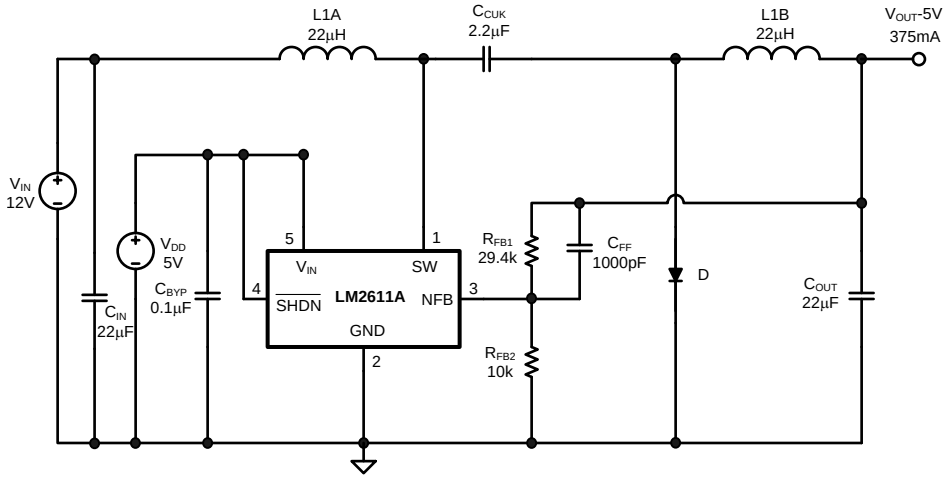


Figure 31. LM2611 Operating With Separate Power and Biasing Supplies Schematic

8.2.5.1 Design Requirements

Follow the design requirements in *Cuk Converter With Integrated Switch*.

8.2.5.2 Detailed Design Procedure

8.2.5.2.1 Split Supply Operation

The LM2611 may be operated with separate power and bias supplies. In the circuit shown in Figure 31, V_{IN} is the power supply that the regulated voltage is derived from, and V_{DD} is a low current supply used to bias the LM2611. Equation 12 and Equation 13 show the conditions for the supplies are:

$$2.7\ V \le V_{DD} \le 14\ V \quad (12)$$

$$0\ V \le V_{IN} \le (36 - |V_{OUT}|)\ V \quad (13)$$

Typical Application (continued)

As the input voltage increases, the maximum output current capacbility increases. Using a separate, higher voltage supply for power conversion enables the LM2611 to provide higher output currents than it would with a single supply that is limited in voltage by $V_{IN(MAX)}$.

8.2.6 Shutdown and Soft-Start

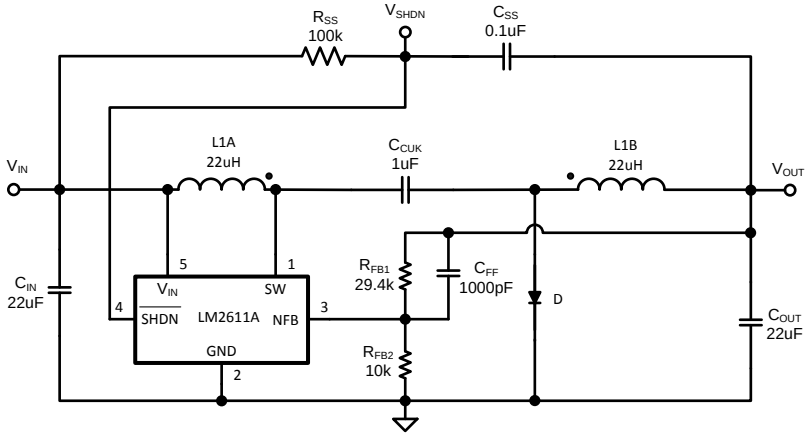


Figure 32. LM2611 Soft-Start Circuit

8.2.6.1 Design Requirements

Follow the design requirements in *Cuk Converter With Integrated Switch*.

8.2.6.2 Detailed Design Procedure

8.2.6.2.1 Shutdown and Soft-Start

A soft-start circuit is used in switching power supplies to limit the input inrush current upon start-up. Without a soft-start circuit, the inrush current can be several times the steady-state load current, and thus apply unnecessary stress to the input source. The LM2611 does not have soft-start circuitry, but implementing the circuit in Figure 32 lowers the peak inrush current. The $\overline{SHDN}$ pin is coupled to the output through C_{SS}. The LM2611 is toggled between shutdown and run states while the output slowly decreases to its steady-state value. The energy required to reach steady state is spread over a longer time and the input current spikes decrease (see Figure 33 and Figure 34).

8.2.6.3 Application Curves

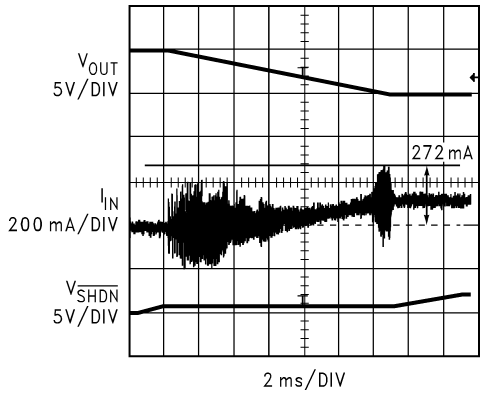


Figure 33. Start-Up Waveforms With a Soft-Start Circuit

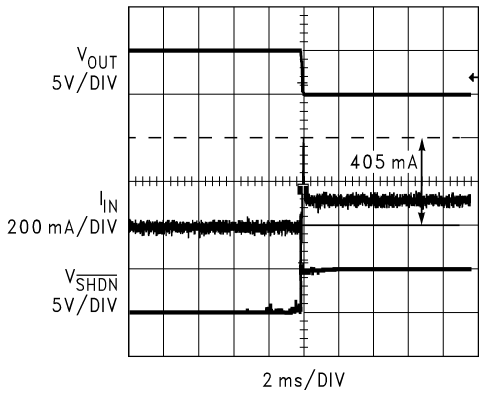


Figure 34. Start-Up Waveforms Without a Soft-Start Circuit

Typical Application (continued)

8.2.7 High Duty Cycle and Load Current

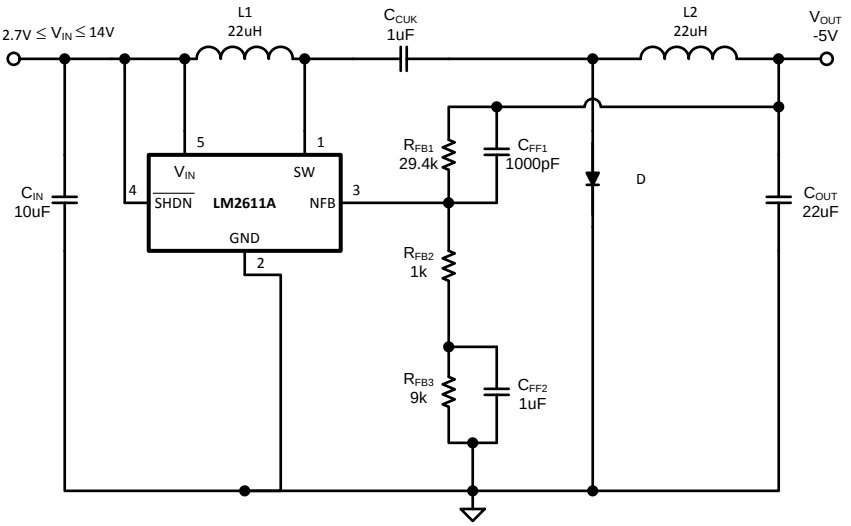


Figure 35. LM2611 High Current Schematic

8.2.7.1 Design Requirements

Follow the design requirements in *Cuk Converter With Integrated Switch*.

8.2.7.2 Detailed Design Procedure

8.2.7.2.1 High Duty Cycle and Load Current Operation

The circuit in Figure 35 is used for high duty cycles (D > 0.5) and high load currents. The duty cycle begins to increase beyond 50% as the input voltage drops below the absolute magnitude of the output voltage. R_{FB3} and C_{FF2} are added to the feedback network to introduce a low frequency lag compensation (pole-zero pair) necessary to stabilize the circuit under the combination of high duty cycle and high load currents.

9 Power Supply Recommendations

The power supply must never exceed the absolute maximum rating of the device given in *Absolute Maximum Ratings*. If the regulator is connected to the input supply through long wires or PCB traces, special care is required to achieve good performance. The parasitic inductance and resistance of the input cables can have an adverse effect on the operation of the regulator. The parasitic inductance, in combination with the low ESR ceramic input capacitors, can form an under-damped resonant circuit. This circuit may cause overvoltage transients at the VIN pin, each time the input supply is cycled on and off.

10 Layout

10.1 Layout Guidelines

- Connection between L1 and SW pin should be kept as short as possible to minimize inductance
- Connection between C_{CUK} and SW should also be kept short
- The feedback resistor should be placed close to the NFB pin to minimize the path of the higher impedance feedback node
- The feedback trace leading from Vout to the output to the feedback resistors should not pass under the switch node between L1 and C_{CUK} and the switch node between C_{CUK}, L2 and D
- The feedback trace leading from Vout to the output to the feedback resistors should not pass under the inductors L1 and L2
- A bypass capacitor C_{BYP} of 0.1 µF should be placed close to VIN and GND pin

10.2 Layout Example

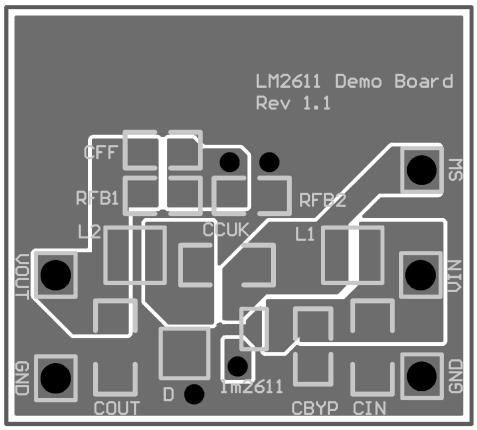


Figure 36. Example Layout Top

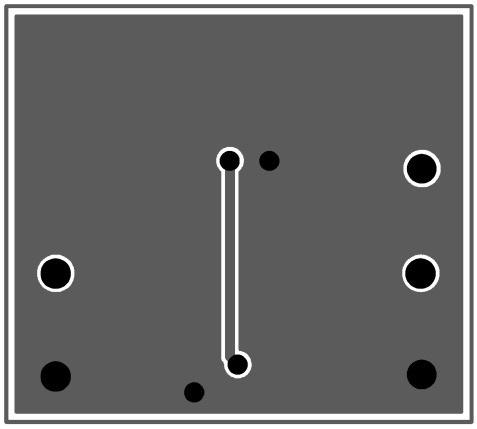


Figure 37. Example Layout Bottom

11 Device and Documentation Support

11.1 Community Resources

The following links connect to TI community resources. Linked contents are provided "AS IS" by the respective contributors. They do not constitute TI specifications and do not necessarily reflect TI's views; see TI's Terms of Use.

TI E2E™ Online Community ***TI's Engineer-to-Engineer (E2E) Community.*** Created to foster collaboration among engineers. At e2e.ti.com, you can ask questions, share knowledge, explore ideas and help solve problems with fellow engineers.

Design Support ***TI's Design Support*** Quickly find helpful E2E forums along with design support tools and contact information for technical support.

11.2 Trademarks

E2E is a trademark of Texas Instruments.
All other trademarks are the property of their respective owners.

11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM2611AMF	NRND	SOT-23	DBV	5	1000	TBD	Call TI	Call TI	-40 to 125	S40A	
LM2611AMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S40A	Samples
LM2611AMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S40A	Samples
LM2611BMF/NOPB	ACTIVE	SOT-23	DBV	5	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S40B	Samples
LM2611BMFX/NOPB	ACTIVE	SOT-23	DBV	5	3000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	S40B	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

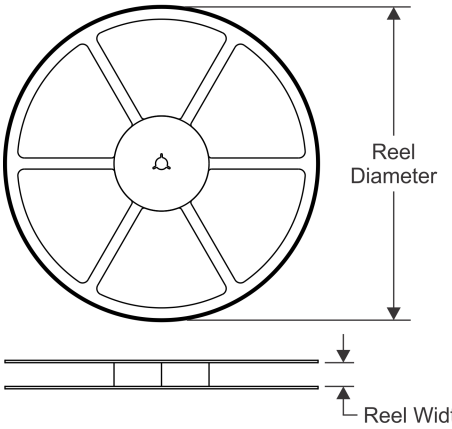
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

Important Information and Disclaimer: The information provided on this page represents TI's knowledge and belief as of the date that it is provided. TI bases its knowledge and belief on information provided by third parties, and makes no representation or warranty as to the accuracy of such information. Efforts are underway to better integrate information from third parties. TI has taken and continues to take reasonable steps to provide representative and accurate information but may not have conducted destructive testing or chemical analysis on incoming materials and chemicals. TI and TI suppliers consider certain information to be proprietary, and thus CAS numbers and other limited information may not be available for release.

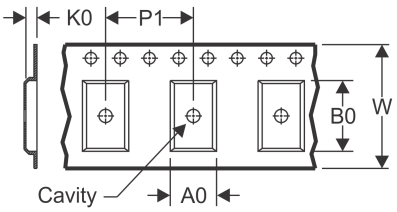
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

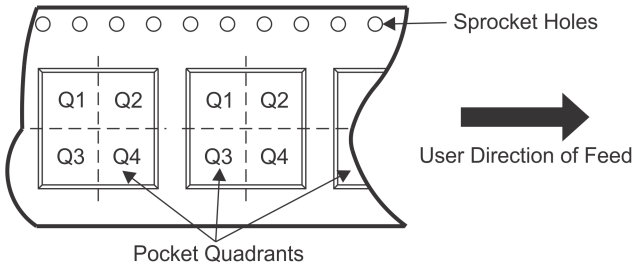


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

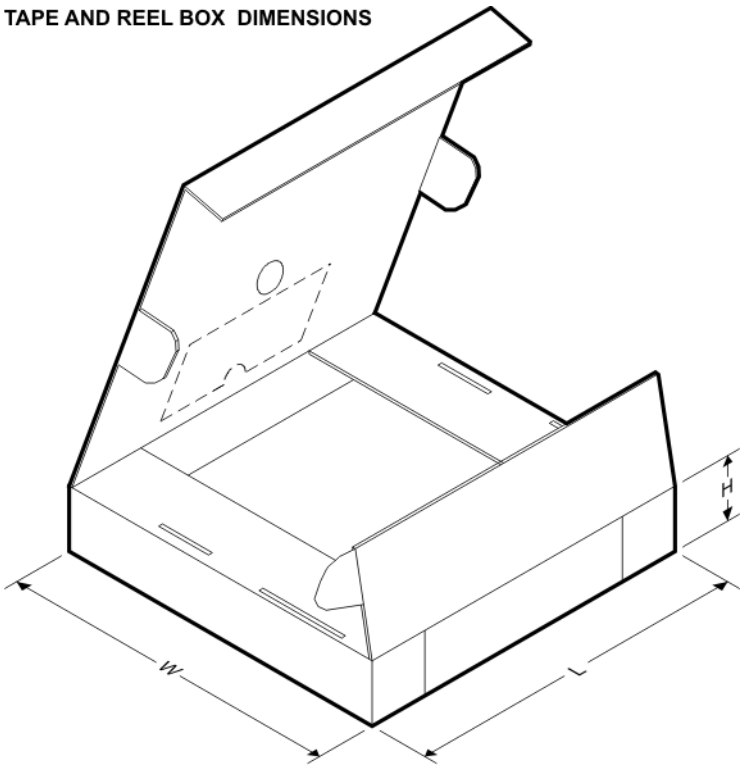
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM2611AMF	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2611AMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2611AMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2611BMF/NOPB	SOT-23	DBV	5	1000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3
LM2611BMFX/NOPB	SOT-23	DBV	5	3000	178.0	8.4	3.2	3.2	1.4	4.0	8.0	Q3

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

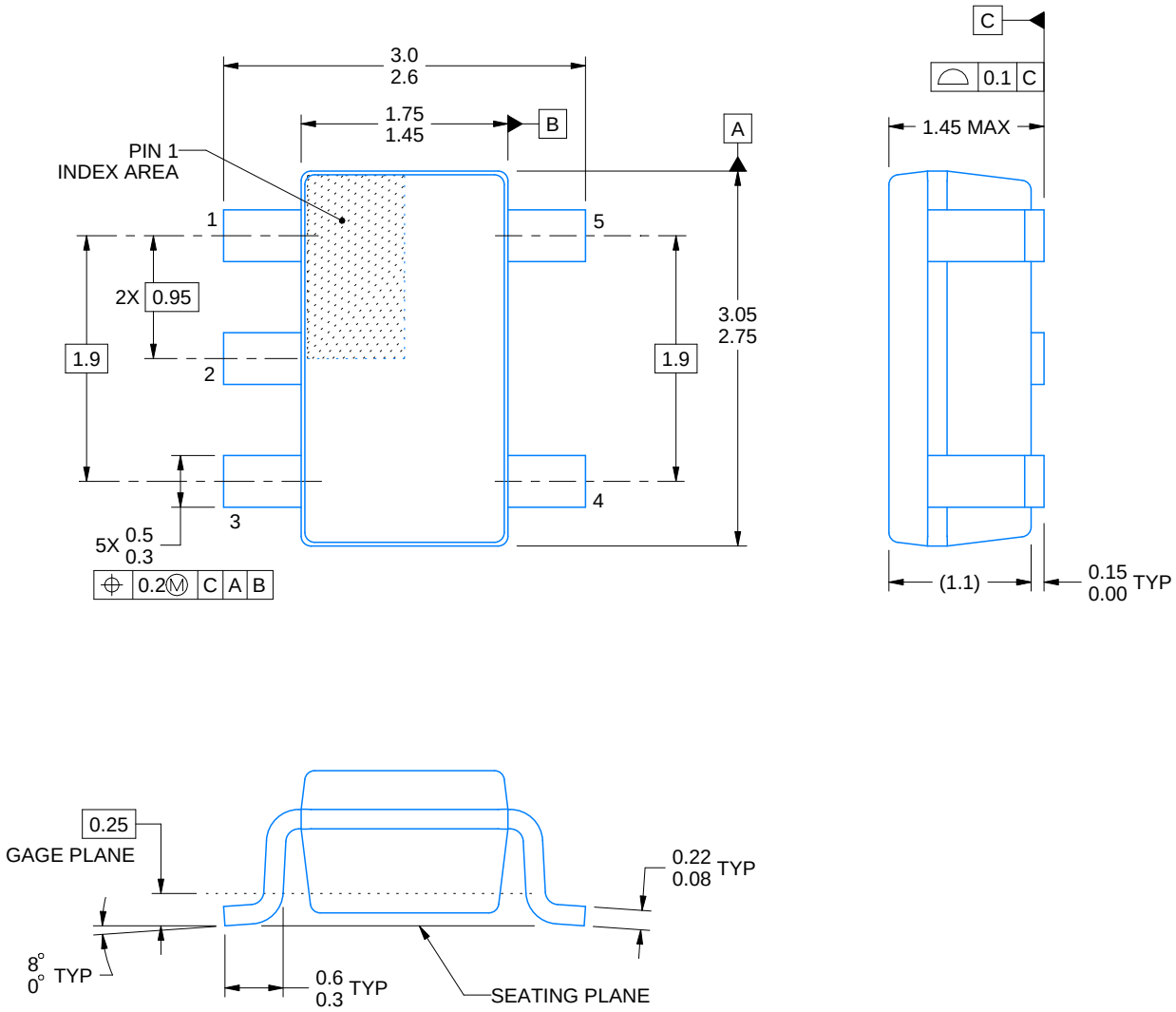
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM2611AMF	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2611AMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2611AMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0
LM2611BMF/NOPB	SOT-23	DBV	5	1000	210.0	185.0	35.0
LM2611BMFX/NOPB	SOT-23	DBV	5	3000	210.0	185.0	35.0

PACKAGE OUTLINE

DBV0005A

SOT-23 - 1.45 mm max height

SMALL OUTLINE TRANSISTOR



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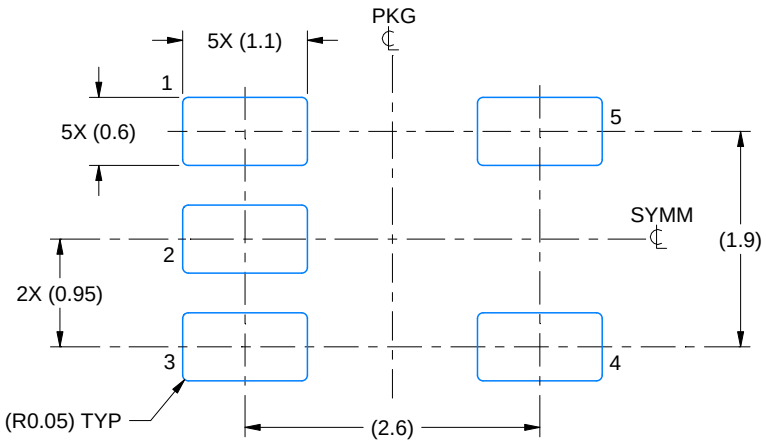
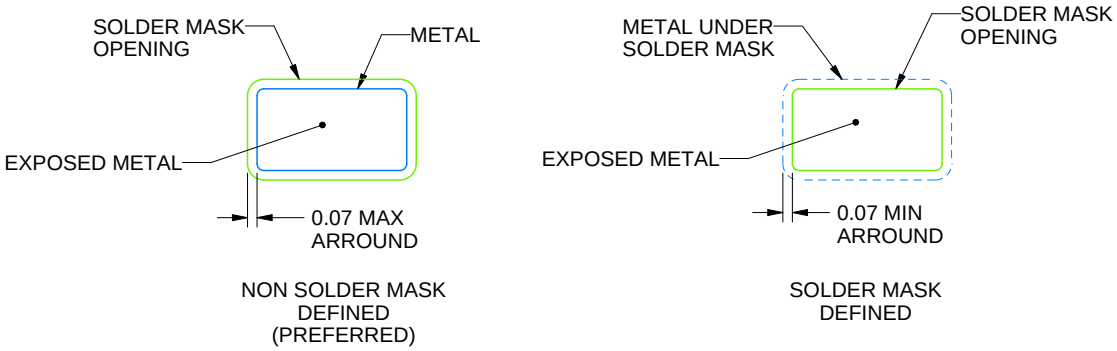
NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. Refernce JEDEC MO-178.
4. Body dimensions do not include mold flash, protrusions, or gate burrs. Mold flash, protrusions, or gate burrs shall not exceed 0.15 mm per side.



LAND PATTERN EXAMPLE
EXPOSED METAL SHOWN
SCALE:15X



SOLDER MASK DETAILS

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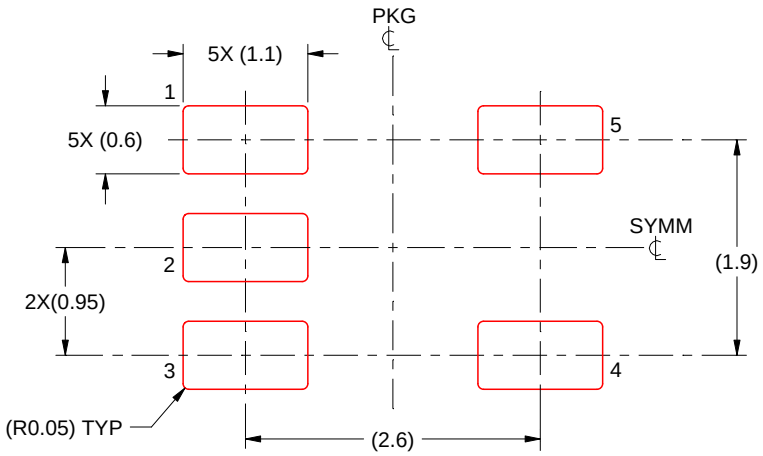
NOTES: (continued)

5. Publication IPC-7351 may have alternate designs.
6. Solder mask tolerances between and around signal pads can vary based on board fabrication site.



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL
SCALE:15X

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NOTES: (continued)

7. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.
8. Board assembly site may have different recommendations for stencil design.

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