



**THE DATASHEET OF  
PMDPB70EN,115**



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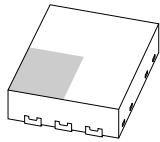
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Kind regards,

Team Nexperia



# PMDPB70EN

30 V, dual N-channel Trench MOSFET

Rev. 1 — 25 April 2012

Product data sheet

## 1. Product profile

### 1.1 General description

Dual N-channel enhancement mode Field-Effect Transistor (FET) in a small and leadless ultra thin DFN2020-6 (SOT1118) Surface-Mounted Device (SMD) plastic package using Trench MOSFET technology.

### 1.2 Features and benefits

- Very fast switching
- Trench MOSFET technology
- Small and leadless ultra thin SMD plastic package: 2 x 2 x 0.65 mm
- Exposed drain pad for excellent thermal conduction

### 1.3 Applications

- Charging switch for portable devices
- DC-to-DC converters
- Small brushless DC motor drive
- Power management in battery-driven portables
- Hard disc and computing power management

### 1.4 Quick reference data

Table 1. Quick reference data

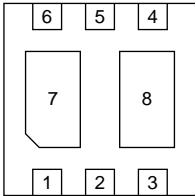
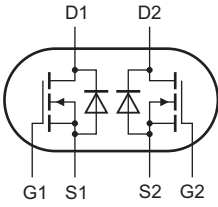
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Per transistor</b>						
$V_{DS}$	drain-source voltage	$T_j = 25\text{ °C}$	-	-	30	V
$V_{GS}$	gate-source voltage		-20	-	20	V
$I_D$	drain current	$V_{GS} = 10\text{ V}; T_{amb} = 25\text{ °C}; t \leq 5\text{ s}$	[1]	-	4.5	A
<b>Static characteristics (per transistor)</b>						
$R_{DS(on)}$	drain-source on-state resistance	$V_{GS} = 10\text{ V}; I_D = 3.5\text{ A}; T_j = 25\text{ °C}$	-	46	57	m $\Omega$

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.



## 2. Pinning information

**Table 2. Pinning information**

Pin	Symbol	Description	Simplified outline	Graphic symbol
1	S1	source TR1	 <p>Transparent top view</p> <p><b>DFN2020-6 (SOT1118)</b></p>	 <p>017aaa254</p>
2	G1	gate TR1		
3	D2	drain TR2		
4	S2	source TR2		
5	G2	gate TR2		
6	D1	drain TR1		
7	D1	drain TR1		
8	D2	drain TR2		

## 3. Ordering information

**Table 3. Ordering information**

Type number	Package		
	Name	Description	Version
PMDPB70EN	DFN2020-6	plastic thermal enhanced ultra thin small outline package; no leads; 6 terminals	SOT1118

## 4. Marking

**Table 4. Marking codes**

Type number	Marking code
PMDPB70EN	1M

## 5. Limiting values

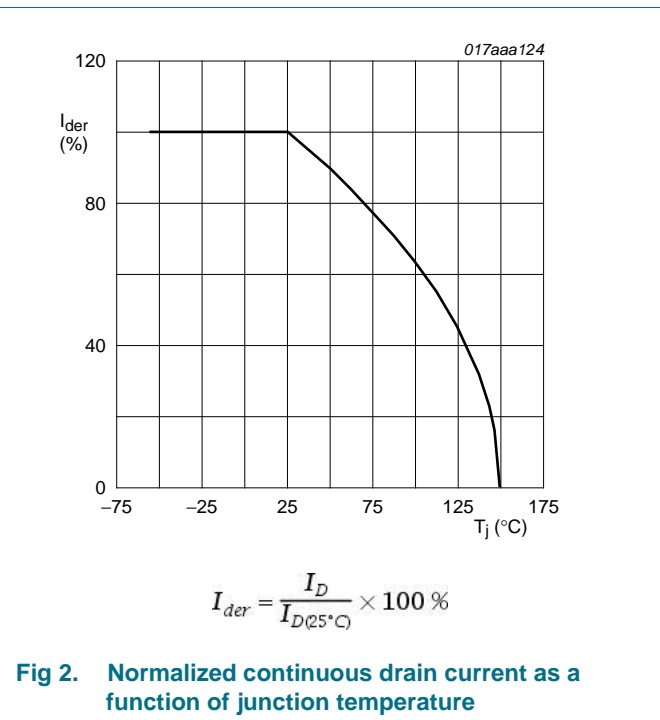
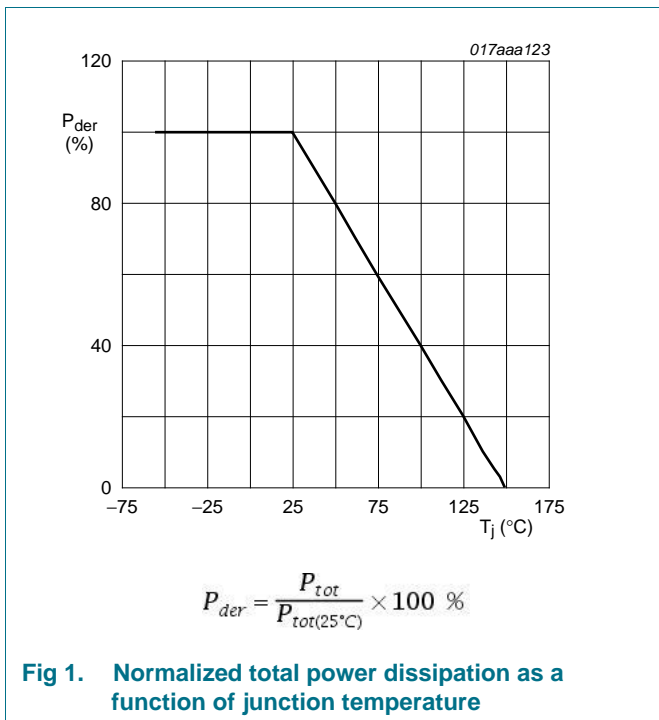
**Table 5. Limiting values**

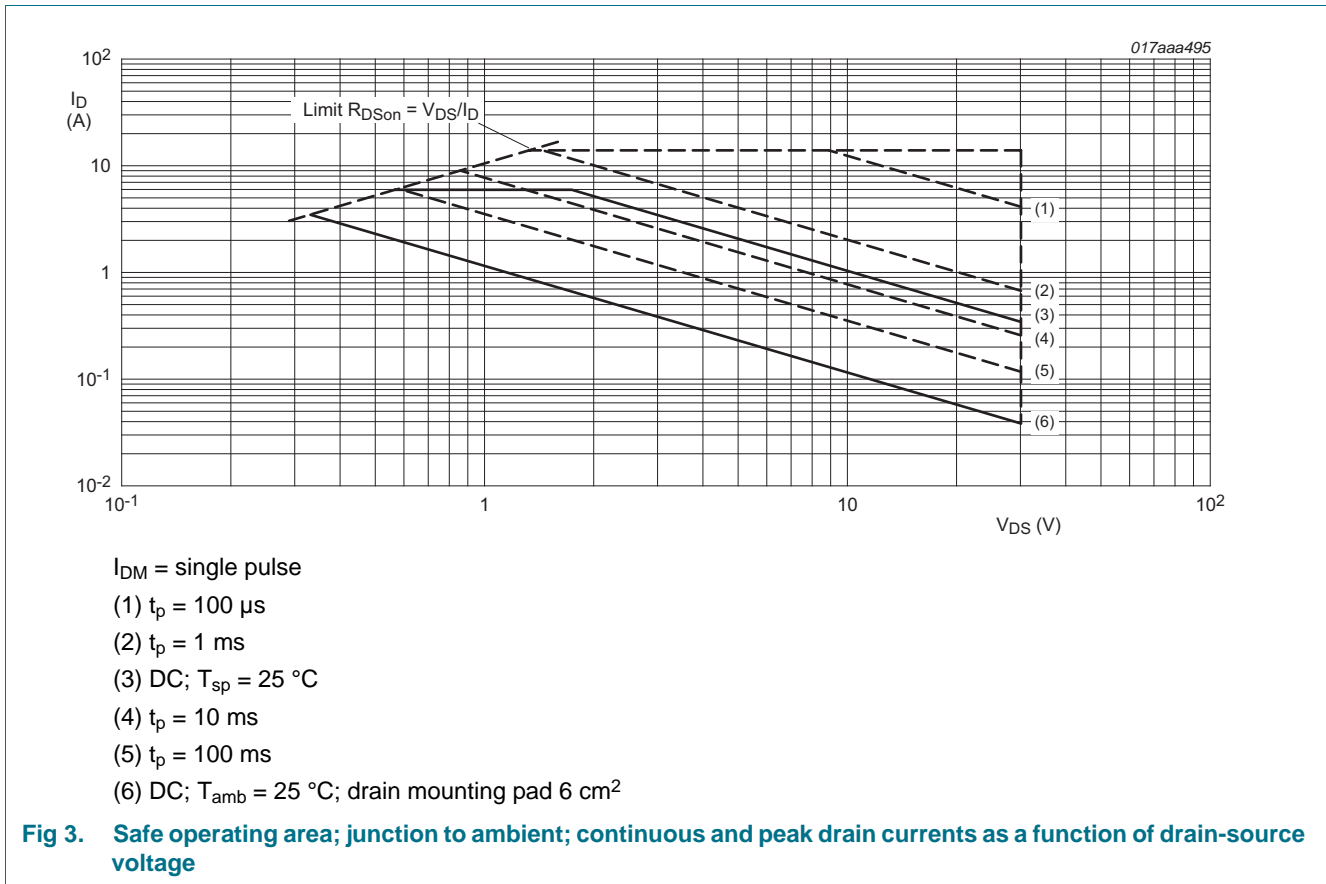
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit	
<b>Per transistor</b>						
V <sub>DS</sub>	drain-source voltage	T <sub>j</sub> = 25 °C	-	30	V	
V <sub>GS</sub>	gate-source voltage		-20	20	V	
I <sub>D</sub>	drain current	V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C; t ≤ 5 s	[1]	-	4.5	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 25 °C	[1]	-	3.5	A
		V <sub>GS</sub> = 10 V; T <sub>amb</sub> = 100 °C	[1]	-	2.2	A
I <sub>DM</sub>	peak drain current	T <sub>amb</sub> = 25 °C; single pulse; t <sub>p</sub> ≤ 10 μs	-	14	A	
P <sub>tot</sub>	total power dissipation	T <sub>amb</sub> = 25 °C	[2]	-	510	mW
			[1]	-	1165	mW
		T <sub>sp</sub> = 25 °C		-	8330	mW
<b>Source-drain diode</b>						
I <sub>S</sub>	source current	T <sub>amb</sub> = 25 °C	[1]	-	0.7	A
<b>Per device</b>						
T <sub>j</sub>	junction temperature		-55	150	°C	
T <sub>amb</sub>	ambient temperature		-55	150	°C	
T <sub>stg</sub>	storage temperature		-65	150	°C	

[1] Device mounted on an FR4 Printed-Circuit Board (PCB), single-sided copper, tin-plated, mounting pad for drain 6 cm<sup>2</sup>.

[2] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.



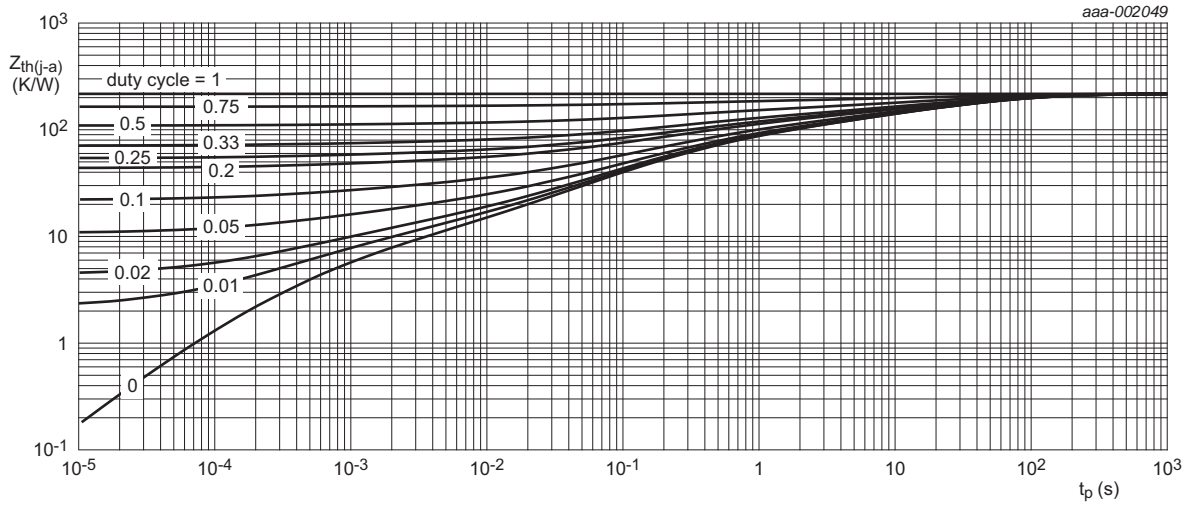


## 6. Thermal characteristics

**Table 6. Thermal characteristics**

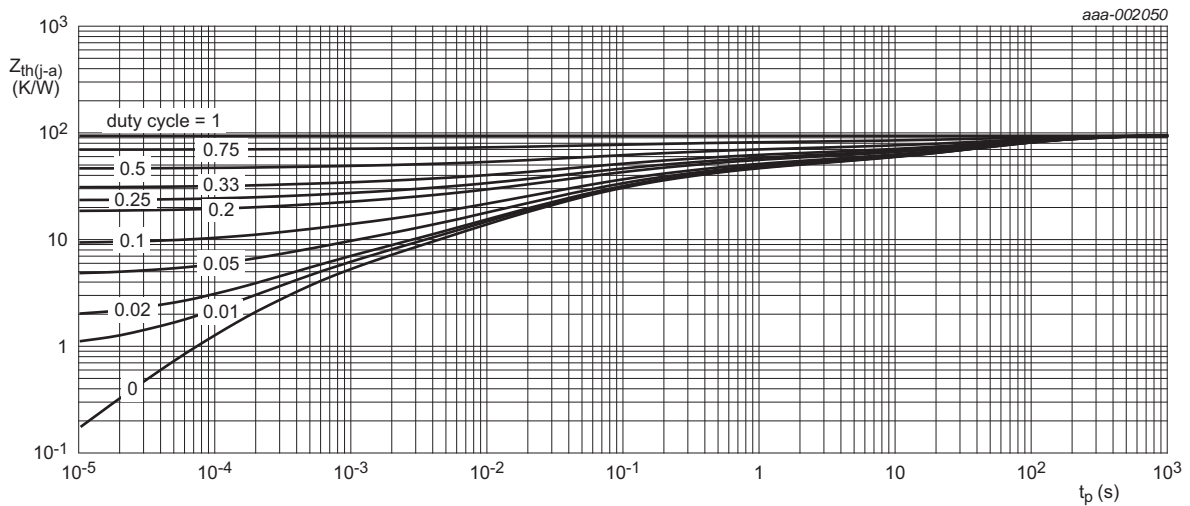
Symbol	Parameter	Conditions	Min	Typ	Max	Unit	
<b>Per transistor</b>							
$R_{th(j-a)}$	thermal resistance from junction to ambient	in free air	[1]	-	213	245	K/W
			[2]	-	93	107	K/W
			[3]	-	55	64	K/W
$R_{th(j-sp)}$	thermal resistance from junction to solder point		-	12	15	K/W	

- [1] Device mounted on an FR4 PCB, single-sided copper, tin-plated and standard footprint.
- [2] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6 \text{ cm}^2$ .
- [3] Device mounted on an FR4 PCB, single-sided copper, tin-plated, mounting pad for drain  $6 \text{ cm}^2$ ,  $t \leq 5 \text{ s}$ .



FR4 PCB standard footprint

Fig 4. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values



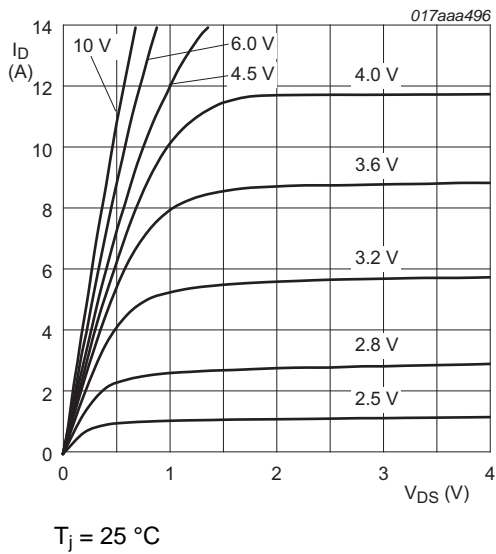
FR4 PCB, mounting pad for drain  $6 \text{ cm}^2$

Fig 5. Transient thermal impedance from junction to ambient as a function of pulse duration; typical values

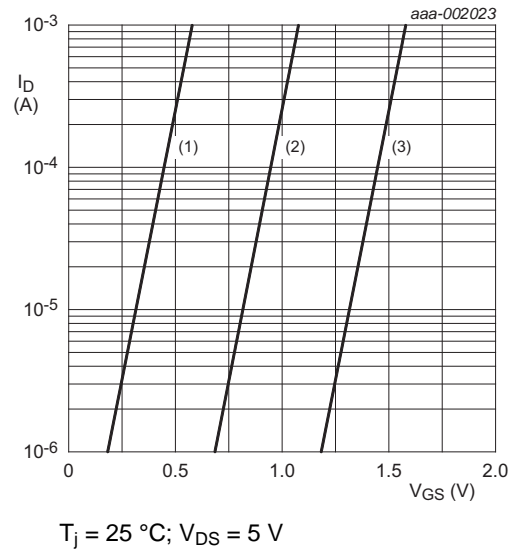
## 7. Characteristics

Table 7. Characteristics

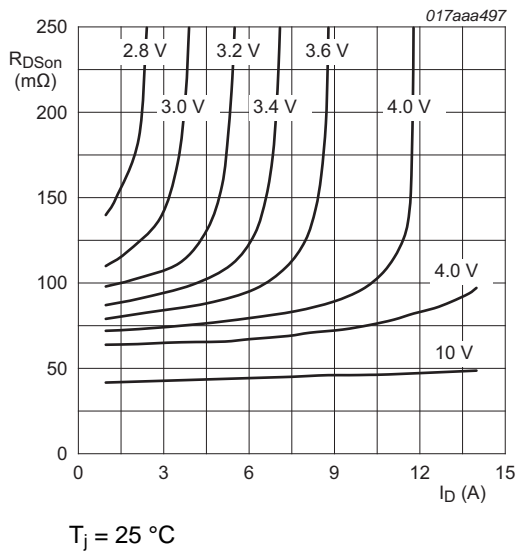
Symbol	Parameter	Conditions	Min	Typ	Max	Unit
<b>Static characteristics (per transistor)</b>						
$V_{(BR)DSS}$	drain-source breakdown voltage	$I_D = 250 \mu\text{A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	30	-	-	V
$V_{GSth}$	gate-source threshold voltage	$I_D = 250 \mu\text{A}$ ; $V_{DS} = V_{GS}$ ; $T_j = 25 \text{ }^\circ\text{C}$	1	1.5	2.5	V
$I_{DSS}$	drain leakage current	$V_{DS} = 30 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	1	$\mu\text{A}$
		$V_{DS} = 30 \text{ V}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	-	10	$\mu\text{A}$
$I_{GSS}$	gate leakage current	$V_{GS} = 20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
		$V_{GS} = -20 \text{ V}$ ; $V_{DS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	-	100	nA
$R_{DSon}$	drain-source on-state resistance	$V_{GS} = 10 \text{ V}$ ; $I_D = 3.5 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	46	57	m $\Omega$
		$V_{GS} = 10 \text{ V}$ ; $I_D = 3.5 \text{ A}$ ; $T_j = 150 \text{ }^\circ\text{C}$	-	76	94	m $\Omega$
		$V_{GS} = 4.5 \text{ V}$ ; $I_D = 2.8 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	67	88	m $\Omega$
$g_{fs}$	forward transconductance	$V_{DS} = 10 \text{ V}$ ; $I_D = 3.5 \text{ A}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	6.4	-	S
<b>Dynamic characteristics (per transistor)</b>						
$Q_{G(tot)}$	total gate charge	$V_{DS} = 15 \text{ V}$ ; $I_D = 3.5 \text{ A}$ ; $V_{GS} = 10 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	3	4.5	nC
$Q_{GS}$	gate-source charge		-	0.52	-	nC
$Q_{GD}$	gate-drain charge		-	0.4	-	nC
$C_{iss}$	input capacitance	$V_{DS} = 15 \text{ V}$ ; $f = 1 \text{ MHz}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	130	-	pF
$C_{oss}$	output capacitance		-	33	-	pF
$C_{rss}$	reverse transfer capacitance		-	14	-	pF
$t_{d(on)}$	turn-on delay time	$V_{DS} = 15 \text{ V}$ ; $I_D = 3.5 \text{ A}$ ; $V_{GS} = 10 \text{ V}$ ; $R_{G(ext)} = 6 \Omega$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	3	-	ns
$t_r$	rise time		-	16	-	ns
$t_{d(off)}$	turn-off delay time		-	15	-	ns
$t_f$	fall time		-	5	-	ns
<b>Source-drain diode (per transistor)</b>						
$V_{SD}$	source-drain voltage	$I_S = 0.7 \text{ A}$ ; $V_{GS} = 0 \text{ V}$ ; $T_j = 25 \text{ }^\circ\text{C}$	-	0.8	1.2	V



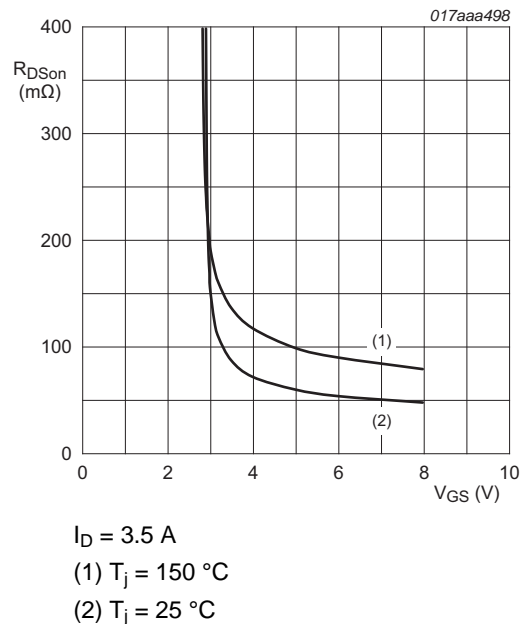
**Fig 6. Output characteristics: drain current as a function of drain-source voltage; typical values**



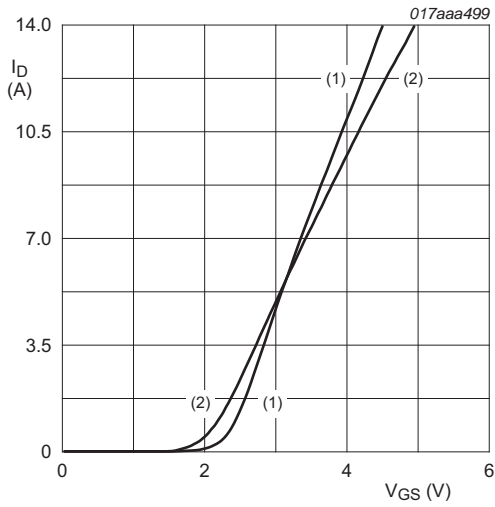
**Fig 7. Sub-threshold drain current as a function of gate-source voltage**



**Fig 8. Drain-source on-state resistance as a function of drain current; typical values**

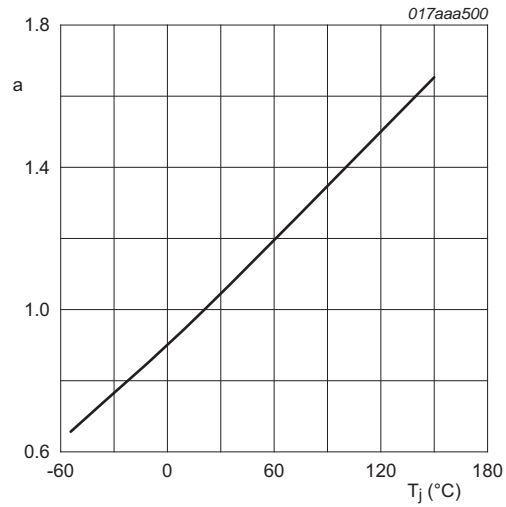


**Fig 9. Drain-source on-state resistance as a function of gate-source voltage; typical values**



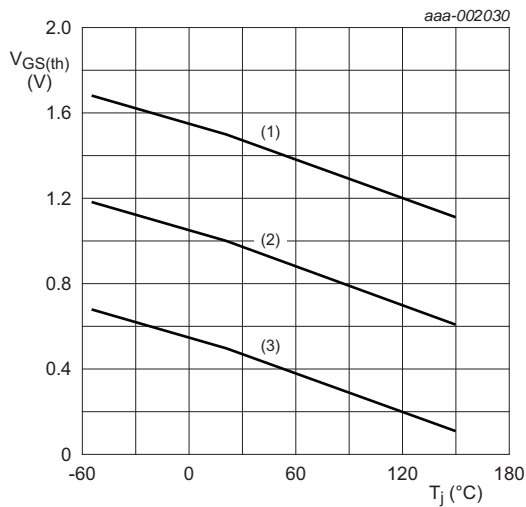
$V_{DS} > I_D \times R_{DS(on)}$   
 (1)  $T_j = 25\text{ }^\circ\text{C}$   
 (2)  $T_j = 150\text{ }^\circ\text{C}$

**Fig 10. Transfer characteristics: drain current as a function of gate-source voltage; typical values**



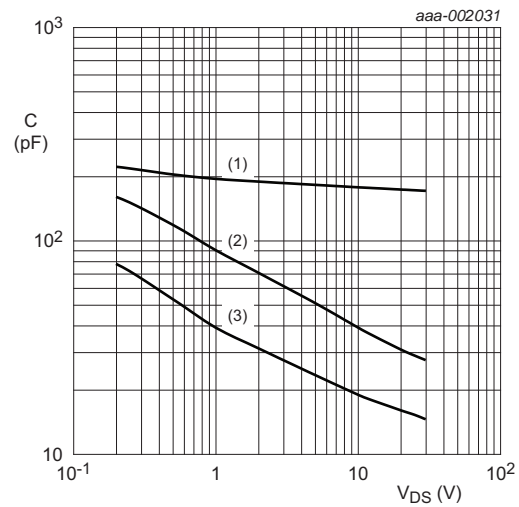
$$a = \frac{R_{DS(on)}}{R_{DS(on)(25^\circ\text{C})}}$$

**Fig 11. Normalized drain-source on-state resistance as a function of junction temperature; typical values**



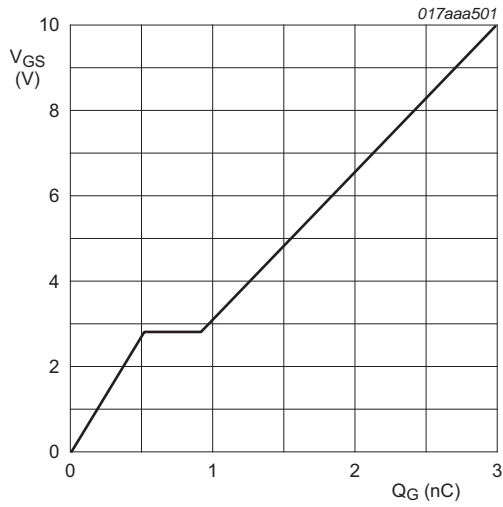
$I_D = 3.1\text{ A}; V_{DS} = V_{GS}$   
 (1) maximum values  
 (2) typical values  
 (3) minimum values

**Fig 12. Gate-source threshold voltage as a function of junction temperature**



$f = 1\text{ MHz}; V_{GS} = 0\text{ V}$   
 (1)  $C_{iss}$   
 (2)  $C_{oss}$   
 (3)  $C_{rss}$

**Fig 13. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values**



$I_D = 3.5$  A;  $V_{DS} = 15$  V;  $T_{amb} = 25$  °C

Fig 14. Gate-source voltage as a function of gate charge; typical values

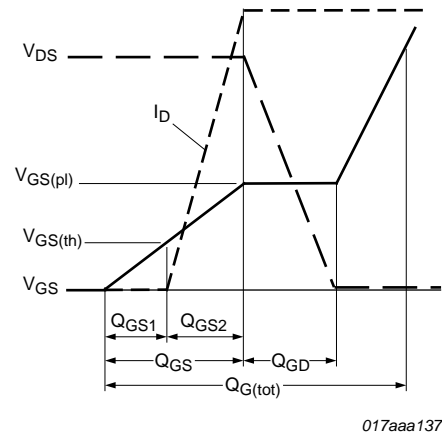
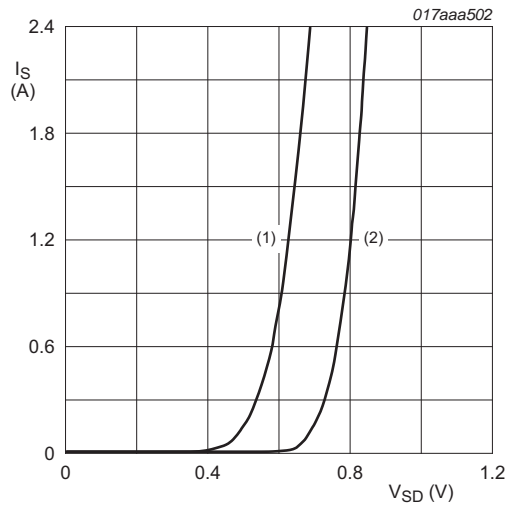


Fig 15. Gate charge waveform definitions



$V_{GS} = 0$  V  
 (1)  $T_{amb} = 150$  °C  
 (2)  $T_{amb} = 25$  °C

Fig 16. Source current as a function of source-drain voltage; typical values

## 8. Test information

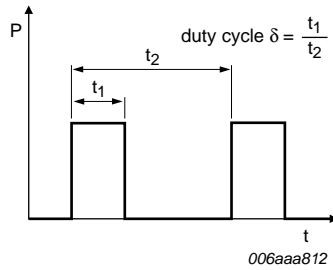


Fig 17. Duty cycle definition

## 9. Package outline

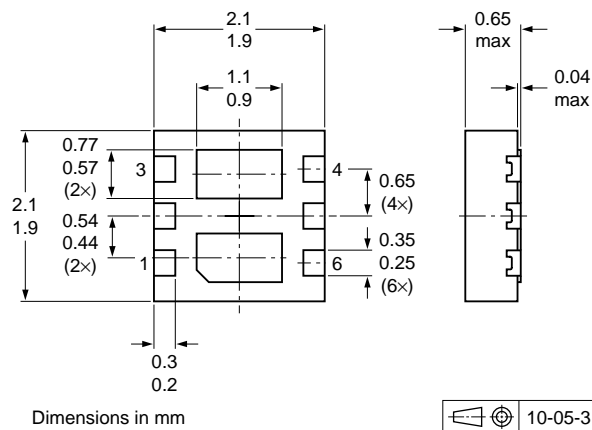
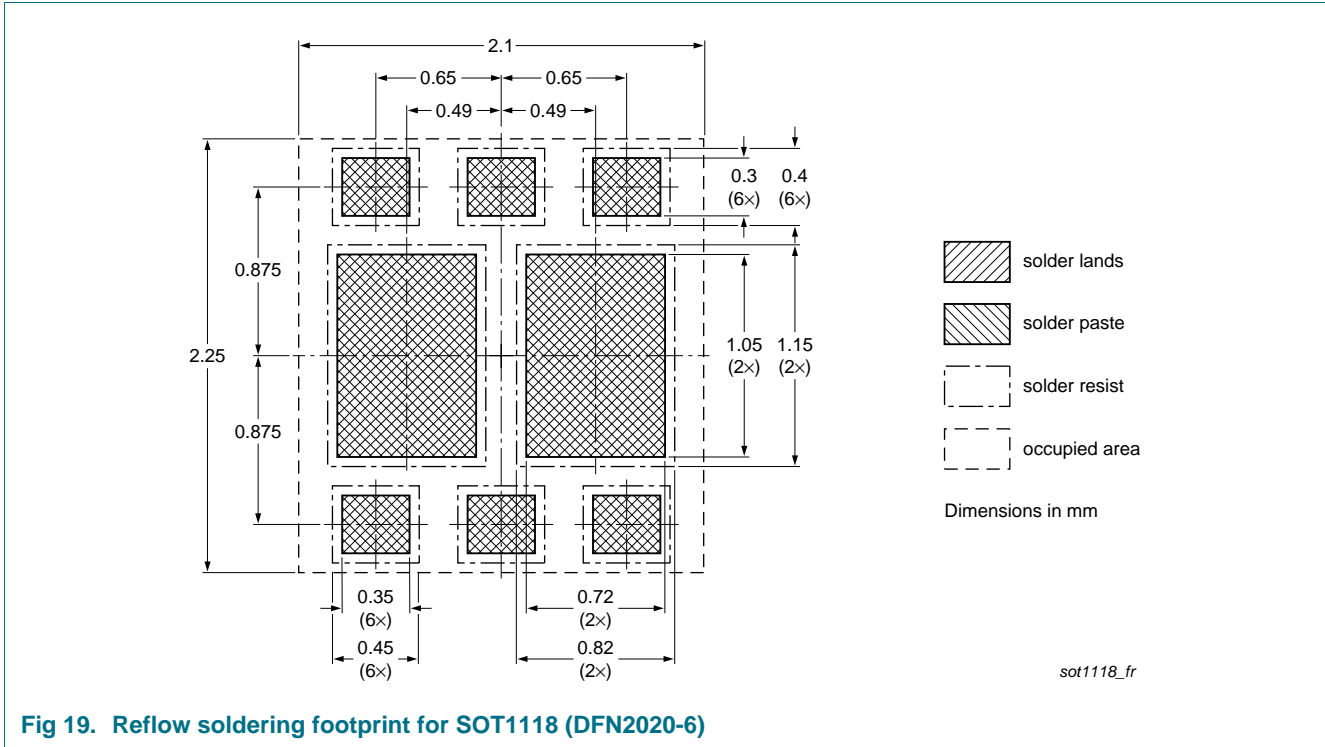


Fig 18. Package outline SOT1118 (DFN2020-6)

**10. Soldering**



**Fig 19. Reflow soldering footprint for SOT1118 (DFN2020-6)**

## 11. Revision history

Table 8. Revision history

Document ID	Release date	Data sheet status	Change notice	Supersedes
PMDPB70EN v.1	20120425	Product data sheet	-	-

## 12. Legal information

### 12.1 Data sheet status

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Objective [short] data sheet	Development	This document contains data from the objective specification for product development.
Preliminary [short] data sheet	Qualification	This document contains data from the preliminary specification.
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