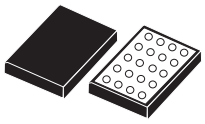
THE DATASHEET OF

STBB2J30-R

STBB2

800 mA 2.5 MHz, high efficiency dual mode buck-boost DC-DC converter

Datasheet - production data



Flip Chip 20 (2.1 x 1.8 mm)

Features

- Operating input voltage range from 2.4 V to 5.5 V
- ± 2% output voltage tolerance over process and temperature variations
- Bypass power save function
- Selectable output voltage with dedicated VSEL pin
- Very fast line and load transients
- 2.5 MHz switching frequency
- Power save mode (PS) at light load
- Typical efficiency higher than 90%
- 50 µA max. quiescent current
- Flip Chip 20 bumps 0.4 mm pitch 2.1 x 1.8 mm

Applications

- Memory card supply
- Cellular phones

Description

The STBB2 is a fixed frequency, high efficiency, buck-boost DC-DC converter which provides output voltages from 1.2 V to 4.5 V starting from input voltage from 2.4 V to 5.5 V. The device can operate with input voltages higher than, equal to, or lower than the output voltage making the product suitable for single Li-Ion, multi-cell alkaline or NiMH applications where the output voltage is within the battery voltage range. The low-$R_{DS(on)}$ N-channel and P-channel MOSFET switches are integrated and help to achieve high efficiency. The MODE pin allows the selection between auto mode and forced PWM mode, taking advantage from either lower power consumption or best dynamic performance. The bypass function allows the battery power saving. In this operating mode, the high-side switches are turned on so that the output voltage is equal to the input voltage; in this condition the current consumption is reduced to a maximum of 5 µA. The device also includes soft-start control, thermal shutdown, and current limit. The STBB2 is packaged in Flip Chip 20 bumps with 0.4 mm pitch.

Table 1. Device summary

Order codes	Markings	Packaging	Output voltages
STBB2JAD-R	BB2	Tape and reel	Adjustable
STBB2J29-R	B229	Tape and reel	2.9 V / 3.4 V
STBB2J30-R	B230	Tape and reel	3.0 V / 3.3 V

Contents

1 Application schematic

Figure 1. Application schematic for fixed version

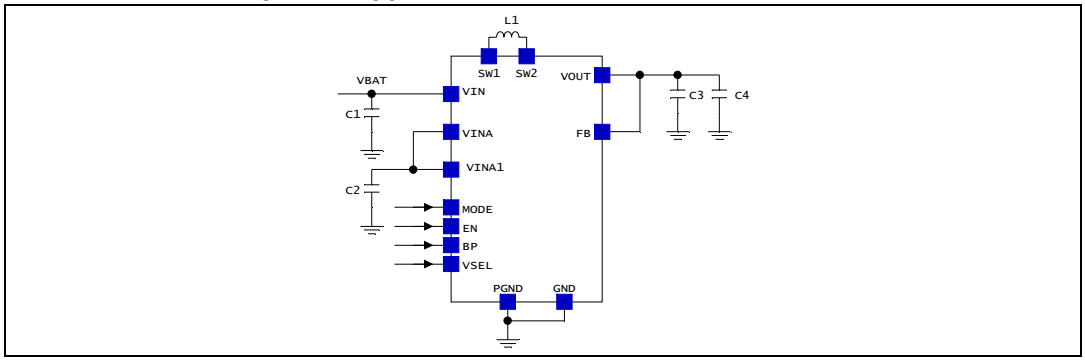


Figure 2. Application schematic for adjustable version

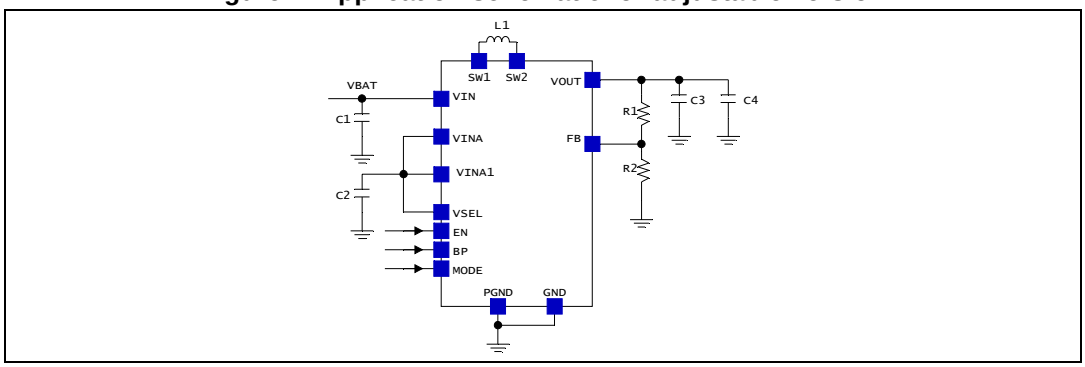


Table 2. Typical external components

Component	Manufacturer	Part number	Value	Size
C1	Murata	GRM188R60J106M	10 µF	0603
	TDK-EPC	C1608X5R0J106M		
C2	Murata	GRM188R61C105K	1 µF	0603
C3, C4	Murata	GRM188R60J106M	10 µF	0603
	TDK-EPC	C1608X5R0J106M		
L(1)	Murata	LQH3NPN1R0NM0	1.0 µH	3 x 3 x 1.4 mm
	Coilcraft	LPS3015-102ML		3.0 x 3.0 x 1.5 mm
	TDK-EPC	VLS252010ET1R0N		2.5 x 2 x 1 mm
R1	Depending on the output voltage, 0 Ω for fixed output version			
R2	Depending on the output voltage, not used for fixed output version			

1. Inductor used for the maximum power capability. Optimized choice can be made according to the application conditions (see *Section 8*).

Note: All the above components refer to a typical application. Operation of the device is not limited to the choice of these external components.

2 Block diagram

Figure 3. Block diagram adjustable

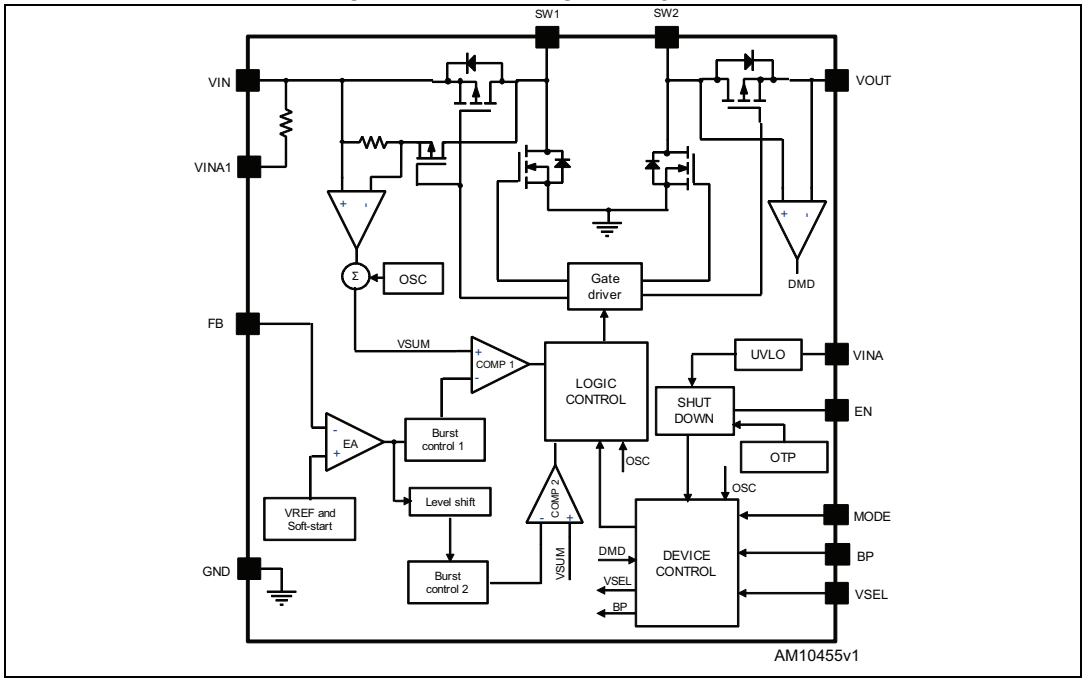
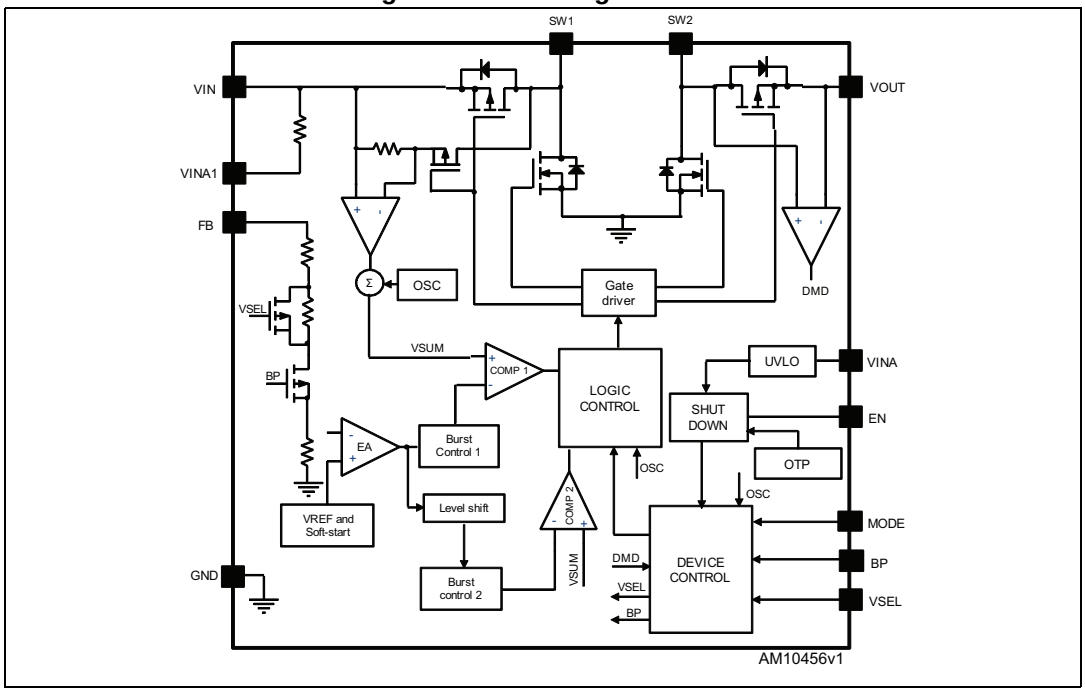


Figure 4. Block diagram fixed



3 Absolute maximum ratings

Table 3. Absolute maximum ratings

Symbol	Parameter	Value	Unit
VIN, VINA, VINA1	Supply voltage	-0.3 to 7.0	V
SW1,SW2	Switching nodes	-0.3 to 7.0	V
VOUT	Output voltage	-0.3 to 7.0	V
MODE, EN, BP, VSEL	Logic pins	-0.3 to 7.0	V
FB	Feedback pin	-0.3 to 6.0	V
ESD	Human body model	± 2000	V
	Charged device model	± 500	
T_{AMB}	Operating ambient temperature	-40 to 85	°C
T_J	Maximum operating junction temperature	150	°C
T_{STG}	Storage temperature	-65 to 150	°C

Note: Absolute maximum ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

Table 4. Thermal data

Symbol	Parameter	Value	Unit
R_{thJA}	Thermal resistance junction-ambient	80 (1)	°C/W

1. PCB condition: JEDEC standard 2s2P(4-layer).

4 Pin configuration

Figure 5. Pin connections (top view)

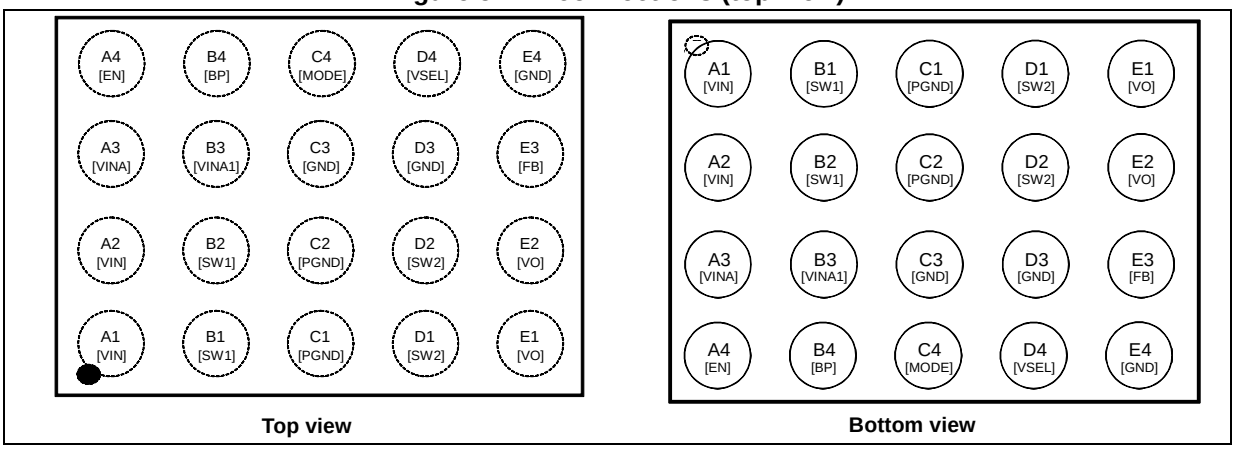


Table 5. Pin description

Pin name	Pin n°	Description
VOUT	E1, E2	Output voltage.
SW2	D1, D2	Switch pin - internal switches C and D are connected to this pin. Connect inductor between SW1 to SW2.
PGND	C1, C2	Power ground.
SW1	B1, B2	Switch pin - internal switches A and B are connected to this pin. Connect inductor between SW1 and SW2.
EN	A4	Enable pin. Connect this pin to GND or a voltage lower than 0.4 V to shut down the IC. A voltage higher than 1.2 V is required to enable the IC. Do not leave this pin floating.
MODE	C4	When in normal operation, the MODE pin selects between auto mode and forced PWM mode. If the MODE pin is low, the STBB2 automatically switches between pulse-skipping and standard PWM according to the load level. If the MODE pin is pulled high, the STBB2 always works in PWM mode. Do not leave this pin floating.
VINA	A3	Supply voltage for control stage.
VINA1	B3	A 100 Ω resistor is internally connected between VIN and VINA1. Connecting a 1 µF capacitor between VINA1 and GND.
VIN	A1, A2	Power input voltage. Connect a ceramic bypass capacitor (10 µF min.) between this pin and PGND.
GND	C3, D3, E4	Signal ground.
FB	E3	Feedback voltage. For the fixed version this pin must be connected to V_{OUT}.

Table 5. Pin description (continued)

Pin name	Pin n°	Description
BP	B4	Bypass mode selection. When EN is high, connecting this pin to a voltage higher than 1.2 V, the device works in bypass mode. A voltage lower than 0.4 V is required to disable bypass mode. In bypass mode VIN is shorted to V_{OUT} through internal switches. Do not leave this pin floating.
VSEL	D4	Selection of output voltage for fixed versions (0 V_{OUT} = 2.9 V / 1 V_{OUT} = 3.4 V), (0 V_{OUT} = 3.0 V / 1 V_{OUT} = 3.3 V). This feature is not present in the adjustable version where the VSEL pin must be connected to VINA. Do not leave this pin floating.

5 Electrical characteristics

- 40 °C < T_A < 85 °C, V_{IN} = 3.6 V; V_{OUT} = 3.4 V, V_{EN} = V_{IN}, V_{BP} = 0 V; typical values are at T_A = 25 °C, unless otherwise specified.

Table 6. Electrical characteristics

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
General section						
V_{IN}	Operating power input voltage range		2.4		5.5	V
I_q	Shutdown mode	V_{EN} = 0 V		0.5	2	µA
	Pulse-skipping	I_{OUT} = 0 A, V_{MODE} = 0		35	50	µA
	PWM mode	I_{OUT} = 0 A, V_{MODE} = V_{IN}		8	10	mA
	Bypass mode	V_{BP} = V_{IN}; I_{OUT} = 0 A; V_{MODE} = 0, V_{IN} = 2.4 to 5.5 V		5	10	µA
V_{UVLO}	Undervoltage lockout threshold	V_{IN} rising; V_{MODE} = V_{IN}; I_{OUT} = 100 mA		2.1	2.35	V
		V_{IN} falling; V_{MODE} = V_{IN}; I_{OUT} = 100 mA		1.8	2.1	
f_{SW}	Switching frequency		2	2.5	3	MHz
I_{OUT}	Continuous output current (1)	2.5 V ≤ V_{IN} ≤ 5.5 V	800			mA
I_{PK}	Switch current limitation		2.4	2.5	2.7	A
I_{PS-PWM}	PS to PWM transition			300		mA
	PWM to PS transition			280		
h	Efficiency (V_{IN} = 3.6 V; V_{OUT} = 3.4 V)	I_{OUT} =1 0 mA (PS mode)		85		%
		I_{OUT} = 50 mA (PS mode)		90		
		I_{OUT} = 150 mA (PWM)		90		
		I_{OUT} = 250 mA (PWM)		91		
		I_{OUT} = 500 mA (PWM)		92		
		I_{OUT} = 800 mA (PWM)		92		
T_{ON}	Turn-on time (2)	V_{EN} from low to high; I_{OUT} = 10 mA		260	300	µs
T_{SHDN}	Thermal shutdown			150		°C
	Hysteresis			20		°C
Output voltage						
V_{OUT}	Output voltage range		1.2		4.5	V

Table 6. Electrical characteristics (continued)

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$\%V_{OUT}$	Output voltage accuracy in PWM mode	V_{IN} = 2.5 to 5.5 V, V_{MODE} = V_{IN} V_{SEL}= GND/V_{IN}	-1.5		+1.5	%
	Output voltage accuracy in power save mode	V_{IN} = 2.5 to 5.5 V, V_{MODE} = GND V_{SEL} = GND/V_{IN} suitable output current to keep PS operation	-3		+3	%
V_{FB}	Feedback voltage accuracy	Adjustable version	493	500	507	mV
$\%V_{OUT}$	Maximum load regulation	I_{LOAD} = from 10 mA to 800 mA		±0.5		%
V_{OPP-PS}	Peak-to-peak ripple in PS mode	I_{OUT} = 100 mA		130		mV
I_{LKFB}	FB pin leakage current	V_{FB} = 5.5 V			9	µA
Logic inputs						
V_{IL}	Low-level input voltage (EN, MODE, BP, VSEL pins)				0.4	V
V_{IH}	High-level input voltage (EN, MODE, BP, VSEL pins)		1.2			V
I_{LK-I}	Input leakage current (EN, MODE, BP, VSEL pins)	V_{EN}=V_{MODE}=V_{BP}=V_{SEL}= 5.5 V		0.01	1	µA
Power switches						
$R_{DS(on)}$	P-channel on-resistance			130	350	mΩ
	N-channel on-resistance			130	350	mΩ
I_{LKG-P}	P-channel leakage current	V_{IN} = V_{OUT} = 5.5 V; V_{EN} = 0			1	µA
I_{LKG-N}	N-channel leakage current	V_{SW1} = V_{SW2} = 5.5 V; V_{EN} = 0			1	µA

1. Not tested in production. This value is guaranteed by correlation with $R_{DS(on)}$, peak current limit and operating input voltage.
2. Not tested in production.

6 Typical performance characteristics

Table 7. Table of graphs

Maximum output current	vs. input voltage	*Figure 5*
Efficiency	vs. output current (power save enabled, V_{IN} = 2.5 V, 3.6 V, 4.5 V/V_{OUT} = 3.4 V)	*Figure 6*
	vs. output current (power save disabled, V_{OUT} = 2.5 V, 3.6 V, 4.5 V/ V_{OUT} = 3.4 V)	*Figure 7*
	vs. output current (power save enabled, V_{IN} = 2.5 V, 3.6 V, 4.5 V/V_{OUT} = 2.9 V)	*Figure 8*
	vs. output current (power save disabled, V_{OUT} = 2.5 V, 3.6 V, 4.5 V/ V_{OUT} = 2.9 V)	*Figure 9*
	vs. input voltage power save enabled, V_{OUT} = 3.4 V, I_{OUT} = (10; 50; 150; 500; 800 mA)	*Figure 10*
	vs. input voltage power save disabled, V_{OUT} = 3.4 V, I_{OUT} = (10; 500; 1000; 2000 mA)	*Figure 12*
	vs. output current (PWM/Auto mode)	*Figure 13*
Waveforms	Load transient response $V_{IN} < V_{OUT}$	*Figure 14*
	Load transient response $V_{IN} > V_{OUT}$	*Figure 15*
	Line transient response (V_{OUT} = 3.3 V, I_{OUT} = 1500 mA)	*Figure 16*
	Startup after enable (V_{OUT} = 3.3 V, V_{IN} = 2.4 V, I_{OUT} = 300 mA)	*Figure 17*
	Startup after enable (V_{OUT} = 3.3 V, V_{IN} = 4.2 V, I_{OUT} = 300 mA)	*Figure 18*

Figure 6. Maximum output current vs. input voltage

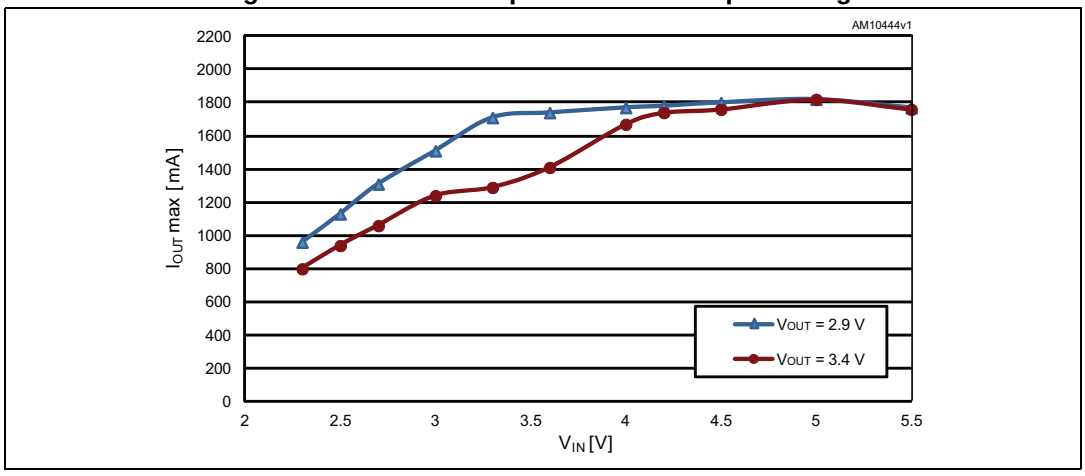


Figure 7. Efficiency vs. output current (power save mode enabled V_{OUT} = 3.4 V)

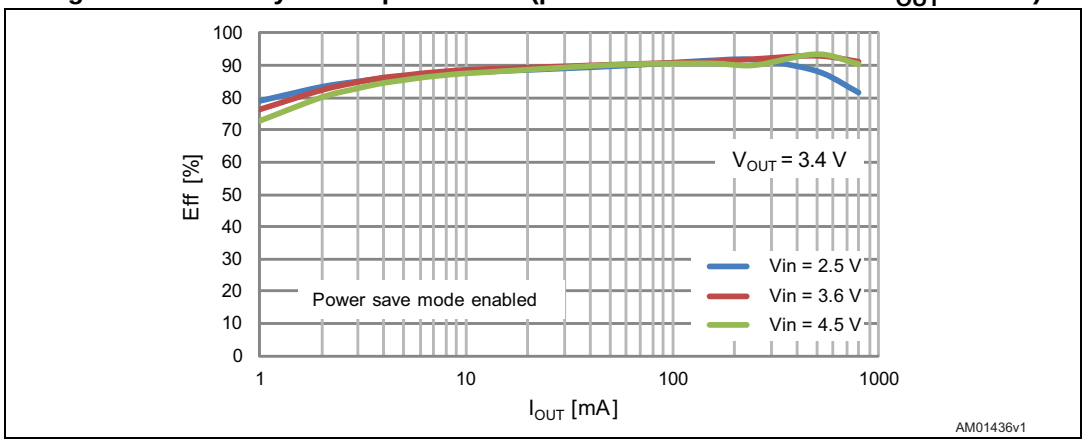


Figure 8. Efficiency vs. output current (power save mode disabled V_{OUT} = 3.4 V)

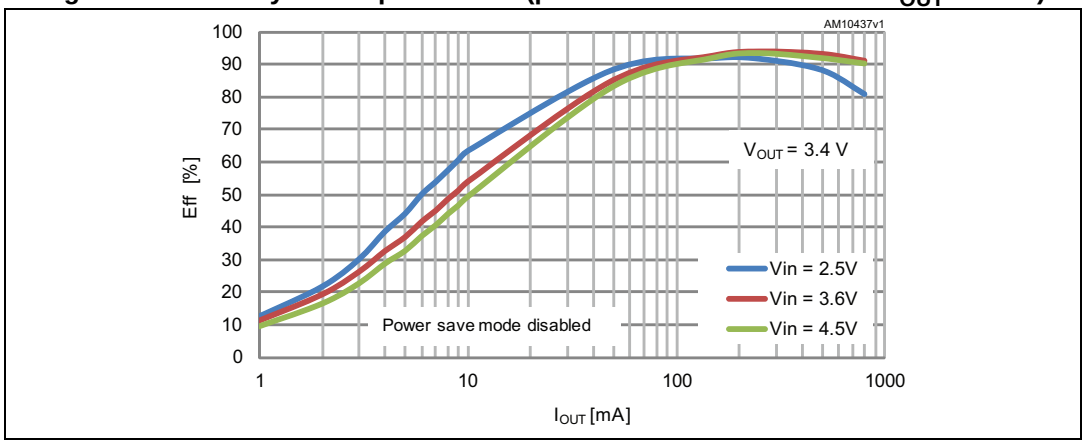


Figure 9. Efficiency vs. output current (power save mode enabled V_{OUT} = 2.9 V)

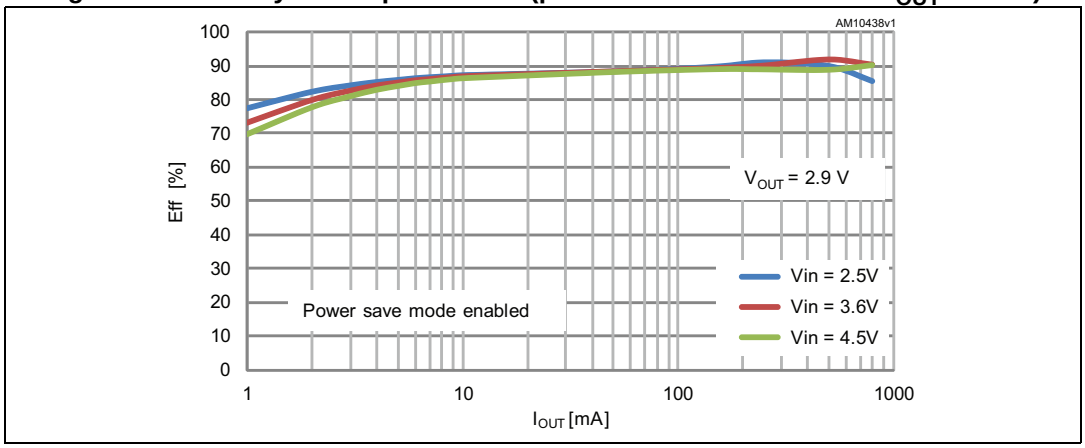


Figure 10. Efficiency vs. output current (power save mode disabled V_{OUT} = 2.9 V)

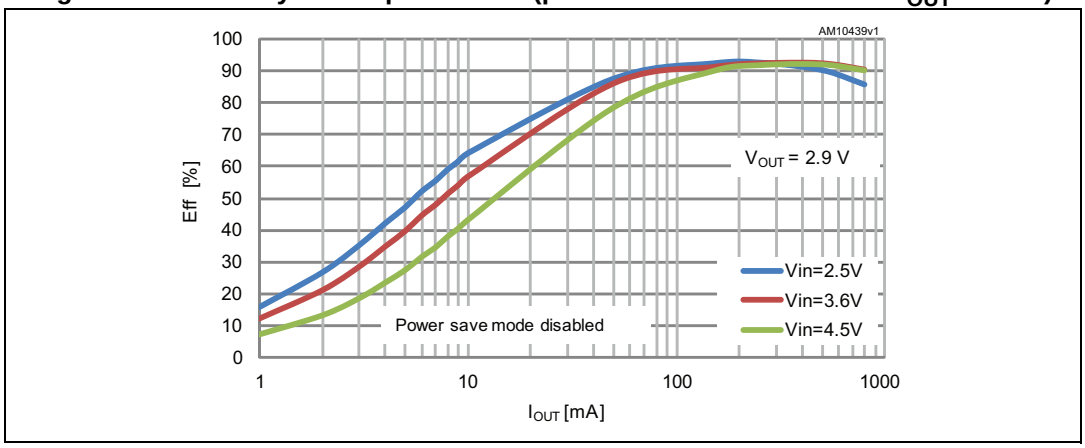


Figure 11. Efficiency vs. input voltage (power save enabled, V_{OUT} = 3.4 V)

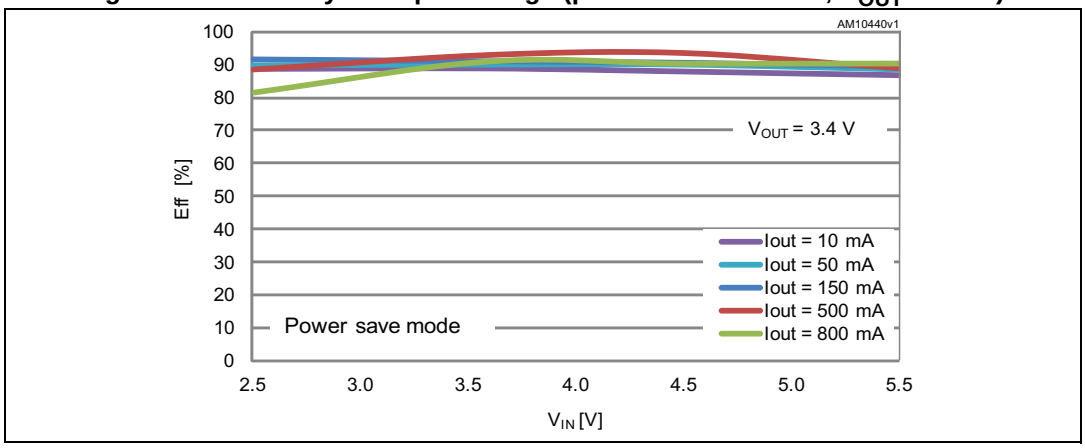


Figure 12. Efficiency vs. input voltage (power save disabled, V_{OUT} = 3.4 V)

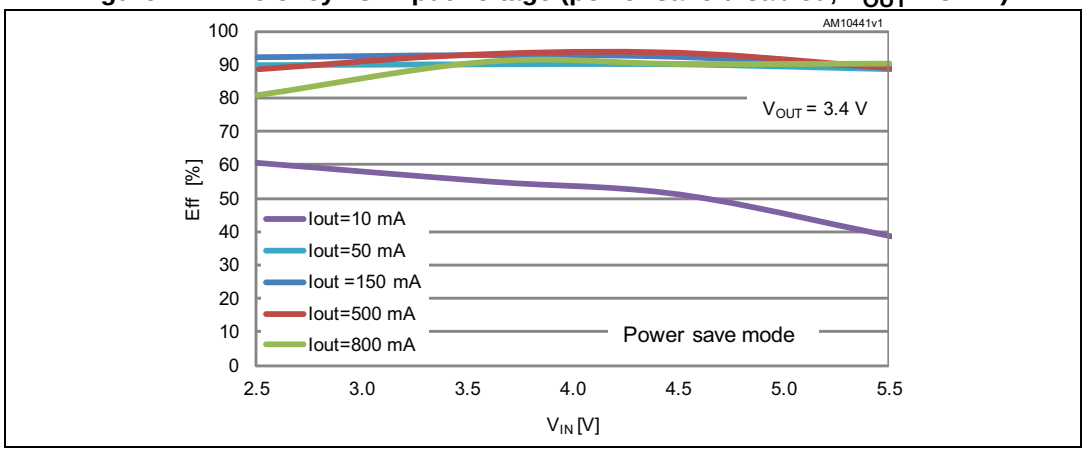


Figure 13. Efficiency vs. output current (PWM / auto mode)

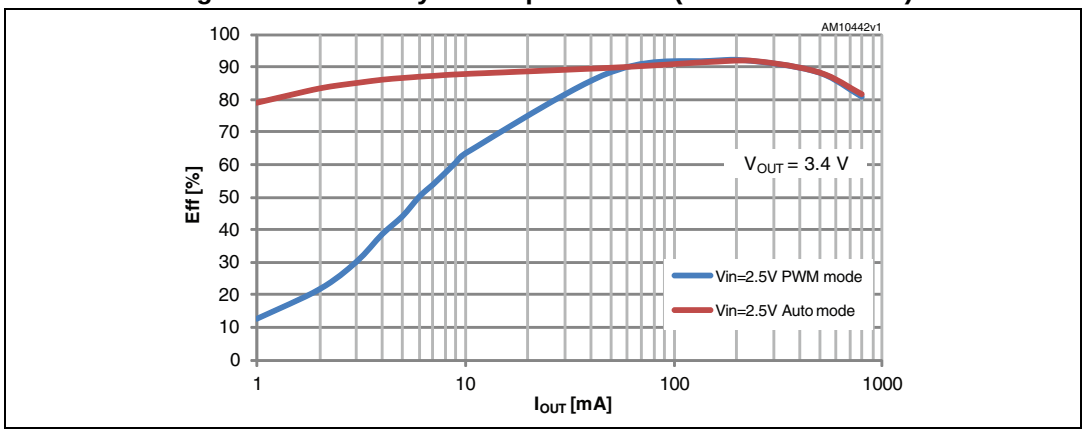


Figure 14. V_{IN} = 2.4 V, V_{OUT} = 3.4 V, I_{OUT} = from 80 mA to 630 mA

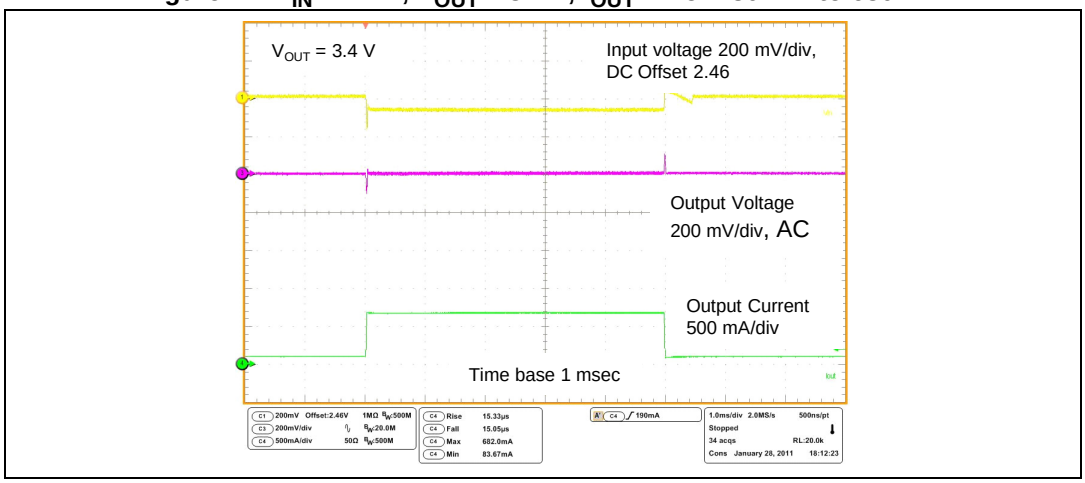


Figure 15. V_{IN} = 4.2 V, V_{OUT} = 3.4 V, I_{OUT} = from 80 mA to 1100 mA

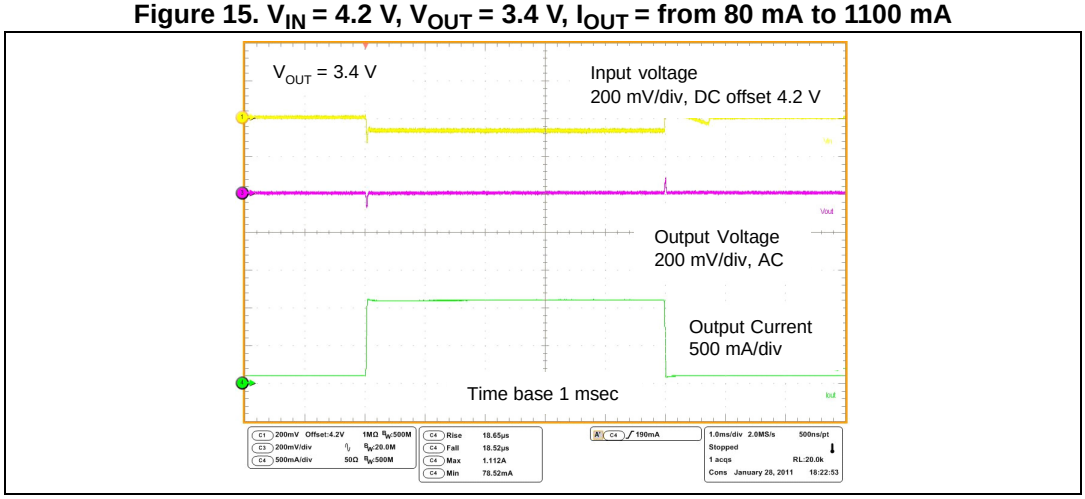


Figure 16. V_{IN} = from 3.6 V to 4 V, V_{OUT} = 3.4 V, I_{OUT} = 300 mA

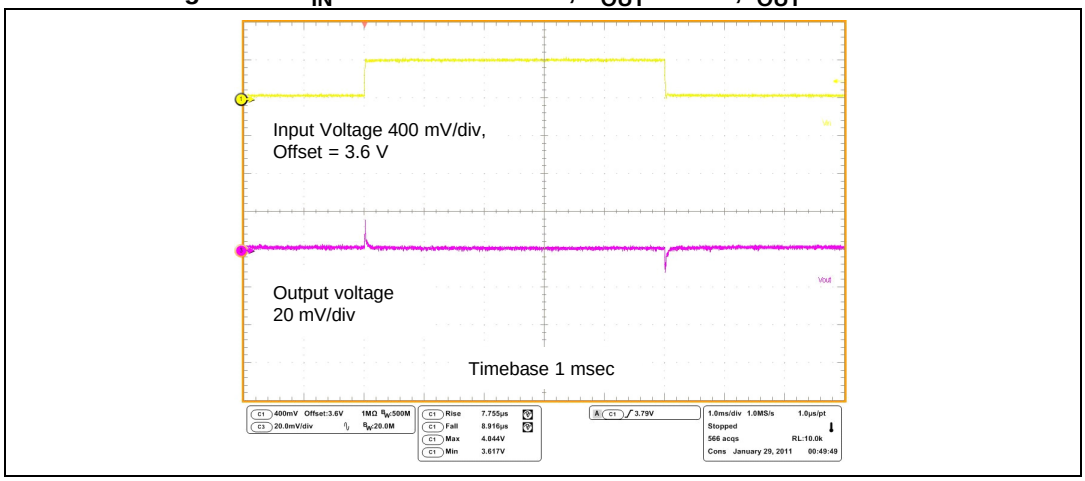


Figure 17. Startup after enable (V_{OUT} = 3.3 V, V_{IN} = 2.4 V, I_{OUT} = 300 mA)

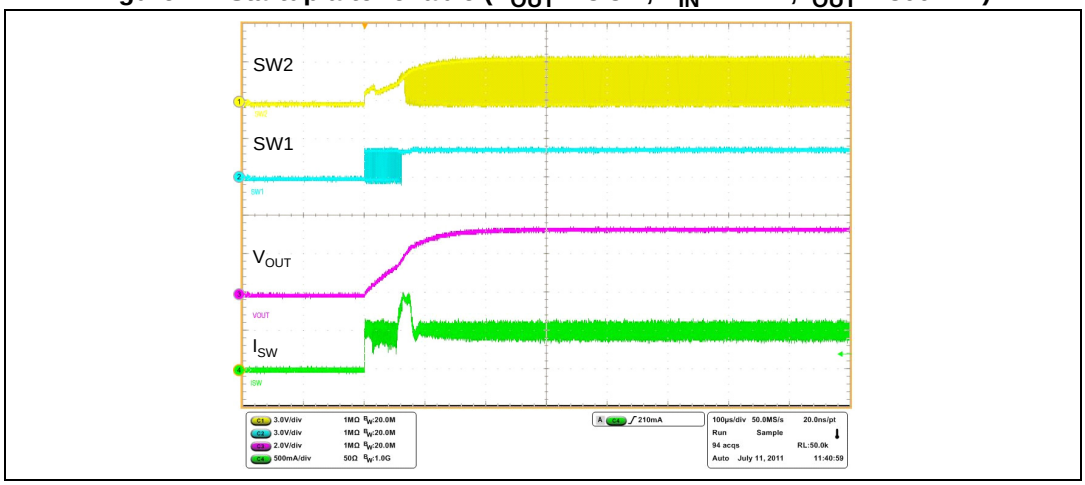
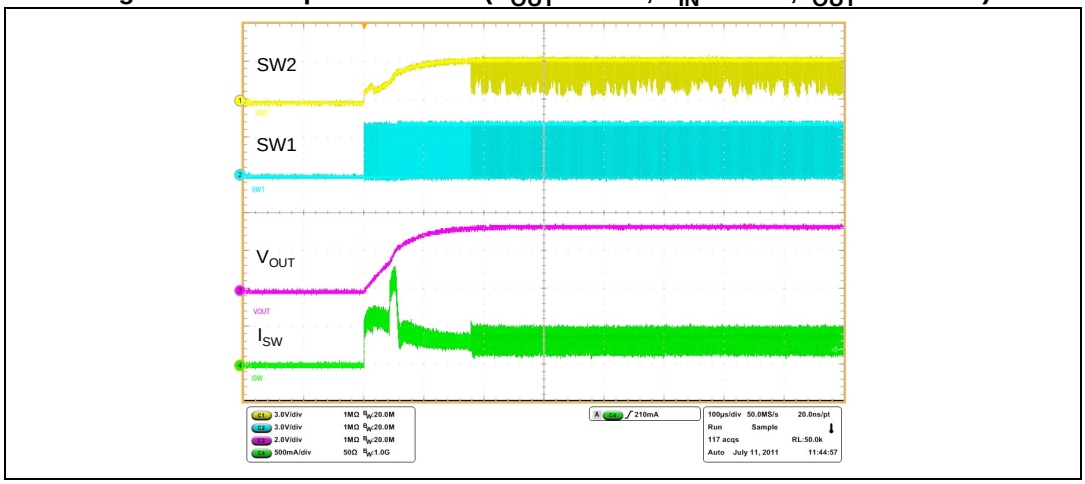


Figure 18. Startup after enable (V_{OUT} = 3.3 V, V_{IN} = 4.2 V, I_{OUT} = 300 mA)



7 General description

The STBB2 is a high efficiency dual mode buck-boost switch mode converter. Thanks to the 4 internal switches, 2 P-channels and 2 N-channels, it is able to deliver a well-regulated output voltage using a variable input voltage which can be higher than, equal to, or lower than the desired output voltage. This solves most of the power supply problems that circuit designers face when dealing with battery powered equipment.

The controller uses an average current mode technique in order to obtain good stability in all possible conditions of input voltage, output voltage and output current. In addition, the peak inductor current is monitored to avoid saturation of the coil.

The STBB2 can work in two different modes: PWM mode or power save mode. In the first case, the device operates with a fixed oscillator frequency in all line/load conditions. This is the suitable condition to obtain the maximum dynamic performance. In the second case the device operates in burst mode allowing a drastic reduction of the power consumption.

Top-class line and load transients are achieved thanks to a feed-forward technique and due to the innovative control method specifically designed to optimize the performance in the buck-boost region where input voltage is very close to the output voltage.

The STBB2 is self-protected from short-circuit and overtemperature. Undervoltage lockout and soft-start guarantee proper operation during startup.

Input voltage and ground connections are split into power and signal pins. This allows reduction of internal disturbances when the 4 internal switches are working. The switch bridge is connected between the V_{IN} and PGND pins while all logic blocks are connected between V_{INA} and GND.

7.1 Dual mode operation

The STBB2 works at fixed frequency pulse width modulation (PWM) or in power save mode (PS) according to the different operating conditions. If the MODE pin is pulled high the device works at fixed frequency pulse width modulation (PWM) even at light or no load. In this condition, the STBB2 provides the best dynamic performance. If the MODE pin is logic low, the STBB2 operation changes according to the average input current handled by the device. At low average current the STBB2 is in PS mode allowing very low power consumption and therefore obtaining very good efficiency event at light load. When the average current increases, the device automatically switches to fixed switching frequency mode in order to deliver the power needed by the load. In PS mode the STBB2 implements a burst mode operation: if the output voltage increases above its nominal value the device stops switching; as soon the V_{OUT} falls below the nominal value the device restarts switching.

7.2 Enable pin

The device turns on when the EN pin is pulled high. If the EN pin is low the device goes to shutdown mode and all internal blocks are turned off. In shutdown mode the load is electrically disconnected from the input to avoid unwanted current leakage from the input to the load and the current drawn from the battery is lower than 1 µA in the whole temperature range.

7.3 Bypass operation

In bypass mode the output is connected directly to the battery by two P-channels and the inductor. The bypass function has been implemented in order to save energy when the application is in idle mode. At light load condition, the device can be in bypass mode to reduce the current drained from the battery. In bypass mode the quiescent current is around 5 µA. Without bypass function, the buck-boost works in pulse-skipping mode with around 50 µA of current consumption. The device can be placed in bypass mode by the BYP pin.

Table 8. Bypass and enable matrix

EN	BP	MODE	Status
0	0	0	Shutdown
0	0	1	Shutdown
0	1	0	Shutdown
0	1	1	Shutdown
1	0	0	Auto mode
1	0	1	PWM mode
1	1	0	Bypass
1	1	1	Bypass

7.4 VSEL pin operation

For the fixed output voltage version, the FB pin must be connected to the V_{OUT} pin. Fixed output voltage versions have two different output voltages programmed internally which are selected by programming high or low at VSEL. The higher output voltage is selected by programming VSEL high and the lower output voltage is selected by programming VSEL low. This feature is not present in the adjustable version, where the VSEL pin must be connected to V_{INA}.

Table 9. Output selection

P/N	V_{SEL}	V_{OUT}
STBB2J-29	Low	2.9 V
	High	3.4 V
STBB2J-30	Low	3.0 V
	High	3.3 V

7.5 Protection features

7.5.1 Soft-start and short-circuit

After the EN pin is pulled high, the device initiates the start-up phase. The average current limit is set to 400 mA at the beginning and is gradually increased while the output voltage increases. As soon as the output voltage reaches 1.0 V, the average current limit is set to its nominal value.

This method allows a current limit proportional to the output voltage. If there is a short in the V_{OUT} pin, the output current does not exceed 400 mA. This process is not handled by a timer so the device is also able to start up even with large capacitive loads.

7.5.2 Undervoltage lockout

The undervoltage lockout function prevents improper operation of the STBB2 when the input voltage is not high enough. When the input voltage is below the VUVLO threshold, the device is in shutdown mode. The hysteresis of 100 mV prevents unstable operation when the input voltage is close to the UVLO threshold.

7.5.3 Overtemperature protection

An internal temperature sensor continuously monitors the IC junction temperature. If the IC temperature exceeds 150 °C (typ.), the device stops operating. As soon as the temperature falls below 130 °C (typ.), normal operation is restored.

8 Application information

8.1 Programming the output voltage

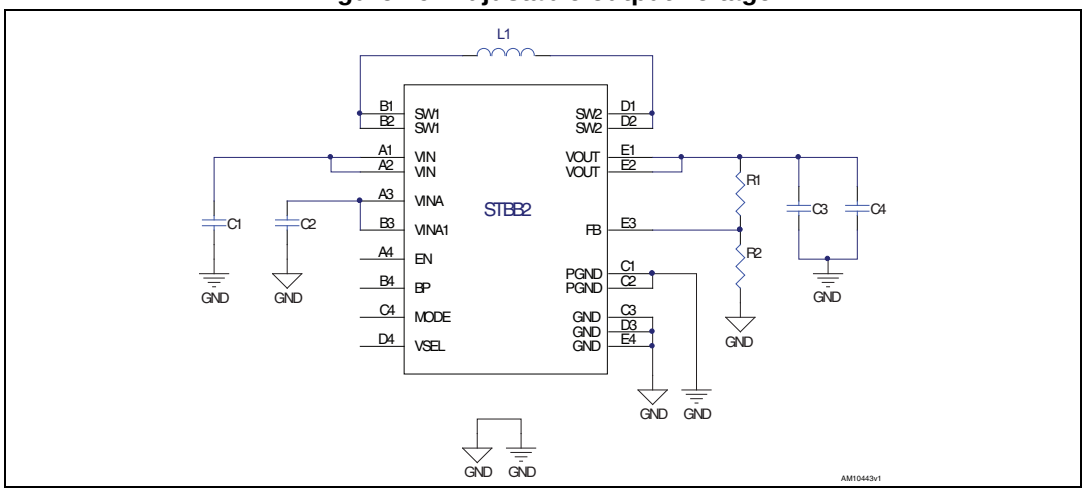
The STBB2 is available in two versions: fixed output voltage and adjustable output voltage.

In the first case the device integrates the resistor divider needed to set the correct output voltage and the FB pin must be connected directly to V_{OUT}. For the fixed version, two different output voltages, programmed internally by the VSEL pin, can be selected. For the adjustable version, the VSEL pin must be connected to V_{IN}. The resistor divider must be connected between V_{OUT} and GND and the middle point of the divider must be connected to FB as shown in *Figure 19*.

Equation 1

$$R1 = R2 \times \left(\frac{V_{OUT}}{V_{FB}} - 1 \right)$$

Figure 19. Adjustable output voltage



A suggested value for R2 is 100 kΩ. To reduce the power consumption a maximum value of 500 kΩ can be used.

8.2 Inductor selection

The inductor is the key passive component for switching converters. With a buck-boost device, the inductor selection must take into consideration the following two conditions in which the converter works:

- as buck at the maximum operative input voltage of the application
- as a boost at the minimum operative input voltage of the application

Two critical inductance values are then obtained according to the following formulas:

Equation 2

$$L_{MIN-BUCK} = \frac{VOUT \times (VIN_{MAX} - VOUT)}{VIN_{MAX} \times fs \times \Delta I_L}$$

Equation 3

$$L_{MIN-BOOST} = \frac{VIN_{MIN} \times (VOUT - VIN_{MIN})}{VOUT \times fs \times \Delta I_L}$$

where fs is the minimum value of the switching frequency and ΔI_L is the peak-to-peak inductor ripple current. The peak-to-peak ripple can be set at 10% or 20% of the output current.

The minimum inductor value for the application is the highest between *Equation 2* and *Equation 3*. In addition to the inductance value, the maximum current, which the inductor can handle, must be calculated in order to avoid saturation.

Equation 4

$$I_{PEAK-BUCK} = (I_{OUT} / \eta) + \frac{VOUT \times (VIN_{MAX} - VOUT)}{2 \times VIN_{MAX} \times fs \times L}$$

Equation 5

$$I_{PEAK-BOOST} = \frac{VOUT \times I_{OUT}}{\eta \times VIN_{MIN}} + \frac{VIN_{MIN} \times (VOUT - VIN_{MIN})}{2 \times VOUT \times fs \times L}$$

where η is the estimated efficiency. The maximum of the two above values must be considered when the inductor is selected.

8.3 Input and output capacitor selection

It is recommended ceramic capacitors to be used with low ESR as input and output capacitors in order to filter any disturbance present in the input line and to obtain stable operation.

Minimum values of 10 µF for both capacitors are needed to achieve good behavior of the device. The input capacitor must be placed as closer as possible to the device.

8.4 Layout guidelines

Due to the high switching frequency and peak current, the layout is an important design step for all switching power supplies. If the layout is not fulfilled carefully, important parameters such as efficiency and output voltage ripple may be compromised.

Short and wide traces must be implemented for main current and for power ground paths. The input capacitor must be placed as closer as possible to the device pins as well as the inductor and output capacitor.

The feedback pin (FB) is a high impedance node, so the interference can be minimized by placing the routing of the feedback node as far as possible from the high current paths. A common ground node minimizes ground noise.

8.5 Product evaluation board

Figure 20. Assembly layer

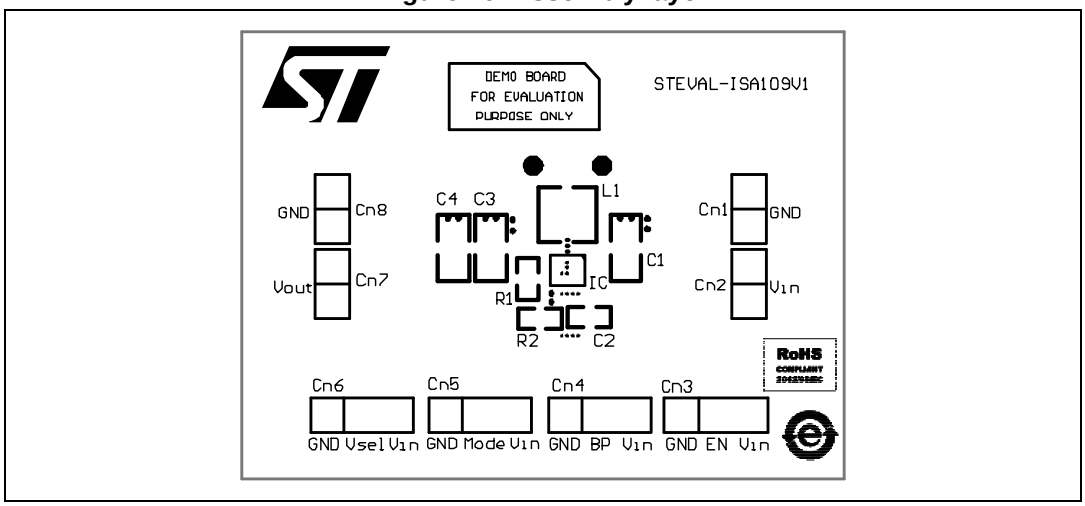


Figure 21. Top layer

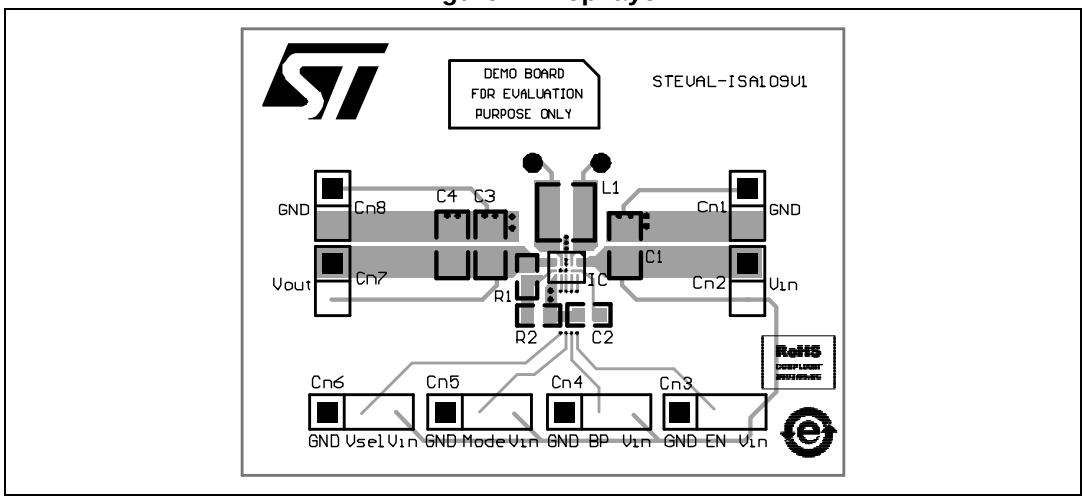
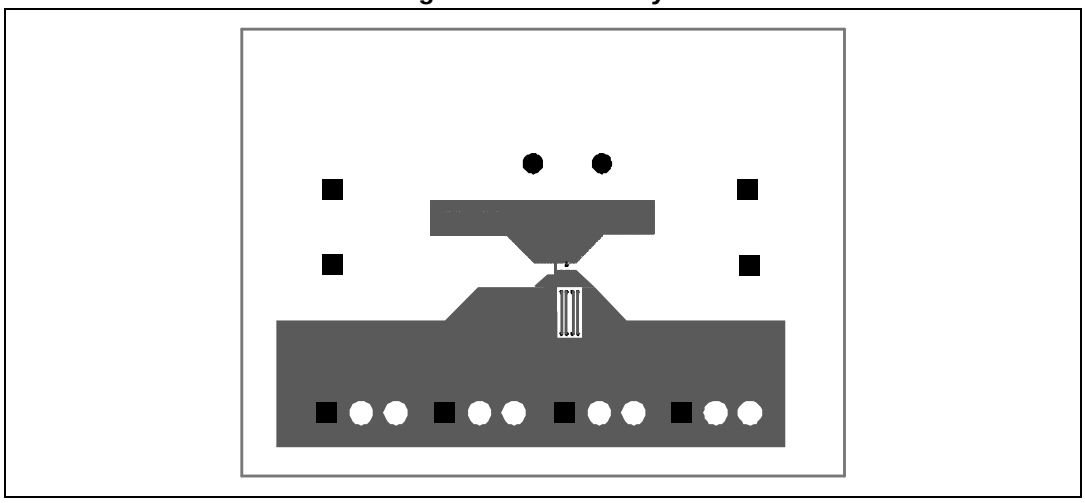


Figure 22. Bottom layer



8.6 Thermal consideration

To enhance the thermal performance, the power dissipation capability of the PCB design can be improved by traces as wider as possible. The maximum recommended junction temperature (T_J) of the devices is 125 °C. The junction ambient thermal resistance of this 20-pin Flip Chip package is 80 °C/W, if all pins are soldered.

To the maximum ambient temperature T_A = 85 °C the maximum power dissipated inside the package is given by:

Equation 6

$P_{DISS\_MAX} = (T_{JMAX} - T_{AMAX}) / R_{JA} = (125 - 85) / 80 = 500$ mW

9 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK® packages, depending on their level of environmental compliance. ECOPACK specifications, grade definitions and product status are available at: www.st.com. ECOPACK is an ST trademark.

Figure 23. Flip Chip 20 (2.1 x 1.8 mm) package dimensions

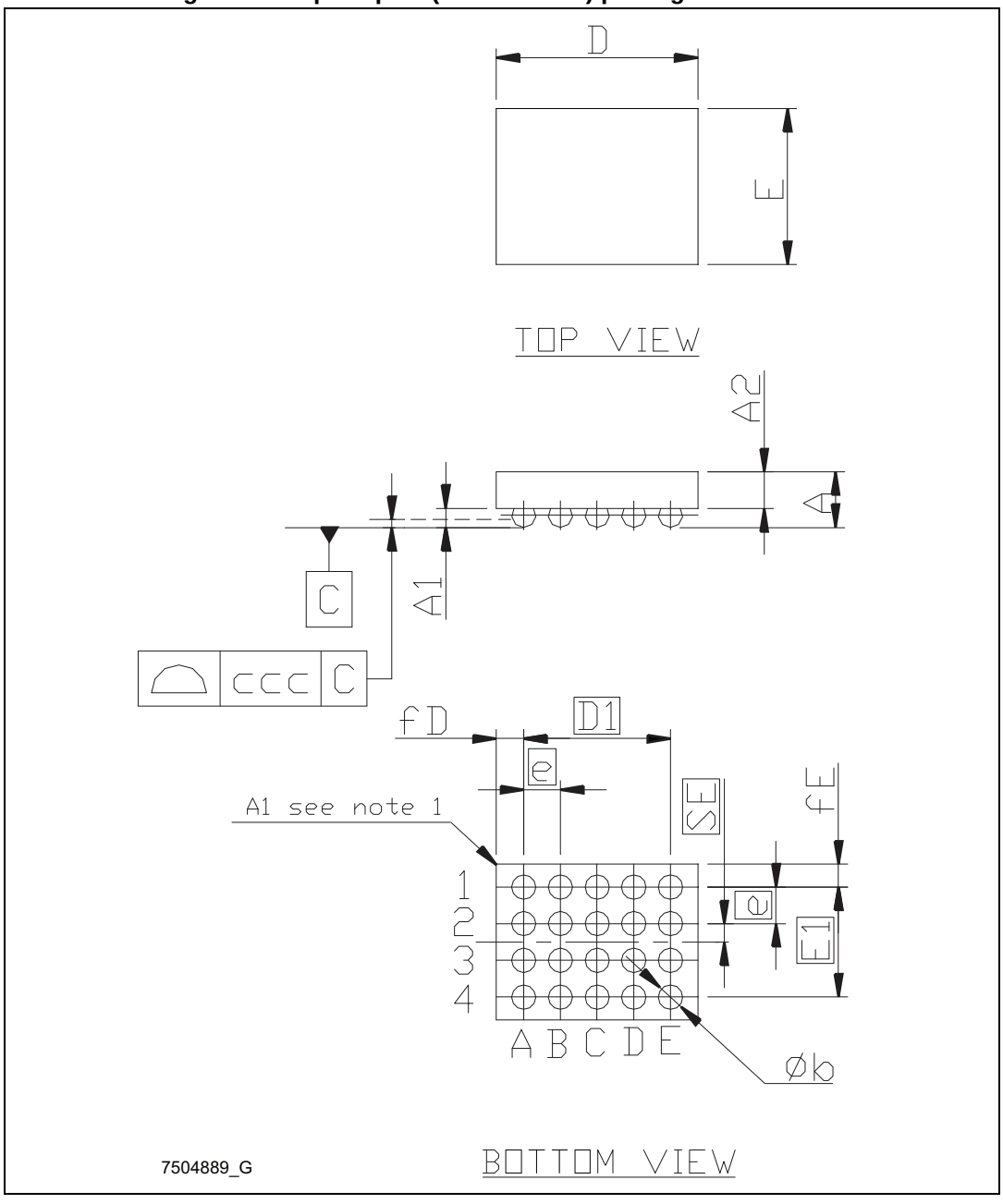


Table 10. Flip Chip 20 (2.1 x 1.8 mm) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	0.52	0.56	0.60
A1	0.17		0.23
A2	0.35	0.36	0.37
b	0.23	0.25	0.29
D	2.03	2.06	2.09
D1		1.6	
E	1.71	1.74	1.77
E1		1.2	
e		0.40	
SE		0.20	
fD		0.23	
fE		0.27	
ccc		0.075	

10 Revision history

Table 11. Document revision history

Date	Revision	Changes
27-Jan-2012	1	First release.
27-Mar-2012	2	Datasheet promoted from preliminary data to production data. Removed: order code STBB2J28-R *Table 1 on page 1*.
09-May-2012	3	Modified: marking BB2 *Table 1 on page 1*, description pin B4 and D4 *Table 5 on page 6*.
26-Jul-2012	4	Modified: C2 value *Table 2 on page 3*. Updated: *Figure 20*, *Figure 21* and *Figure 22 on page 21*.
19-Sep-2012	5	Modified: *Figure 2 on page 3*.
06-Mar-2013	6	Added: new order code STBB2J33-R *Table 1 on page 1*.
17-Dec-2013	7	Changed order code from the STBB2J33-R to the STBB2J30-R in *Table 1: Device summary* and in *Table 9: Output selection*. Changed V_{OPP-PS} typ. value from 100 to 130 in *Table 6: Electrical characteristics*. Minor text changes.
20-Jan-2014	8	Updated mechanical data.
12-Feb-2014	9	Updated *Features* and *Description* in cover page. Changed typ. and max. values of V_{UVLO} parameter in *Table 6*. Changed V_{IN} min. value in *Table 6*. Changed V_{IN} test conditions of I_q parameter in *Table 6*. Changed I_{PK} min. value in *Table 6*. Updated *Table 7*.

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