THE DATASHEET OF

LM3310SQX/NOPB

LM3310 Step-Up PWM DC/DC Converter with Integrated Op-Amp and Gate Pulse Modulation Switch

Check for Samples: LM3310

FEATURES

- **Boost Converter with a 2A, 0.18Ω Switch**
- **Boost Output Voltage Adjustable up to 20V**
- **Operating Voltage Range of 2.5V to 7V**
- **660kHz/1.28MHz Pin Selectable Switching Frequency**
- **Adjustable Soft-Start Function**
- **Input Undervoltage Protection**
- **Over Temperature Protection**
- **Integrated Op-Amp**
- **Integrated Gate Pulse Modulation (GPM) Switch**
- **24-Lead WQFN Package**

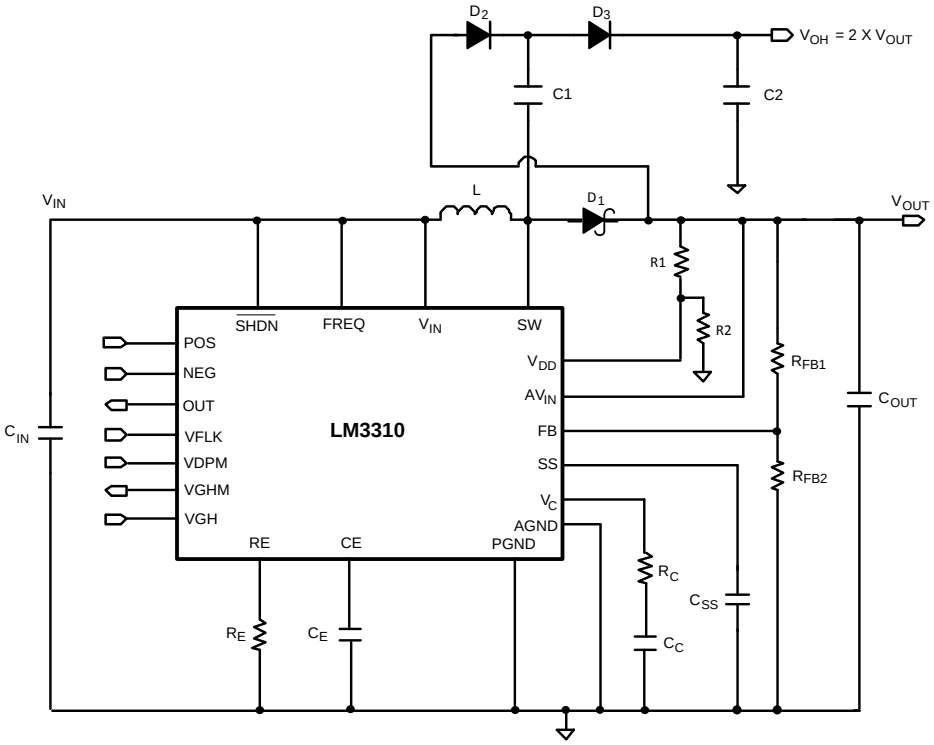
APPLICATIONS

- **TFT Bias Supplies**
- **Portable Applications**

DESCRIPTION

The LM3310 is a step-up DC/DC converter integrated with an Operational Amplifier and a gate pulse modulation switch. The boost (step-up) converter is used to generate an adjustable output voltage and features a low R_{DSON} internal switch for maximum efficiency. The operating frequency is selectable between 660kHz and 1.28MHz allowing for the use of small external components. An external soft-start pin enables the user to tailor the soft-start time to a specific application and limit the inrush current. The Op-Amp is capable of sourcing/sinking 135mA of current (typical). The gate pulse modulation switch can operate with a VGH voltage of 5V to 30V. The LM3310 is available in a low profile 24-lead WQFN package.

Typical Application Circuit



Connection Diagram

Top View

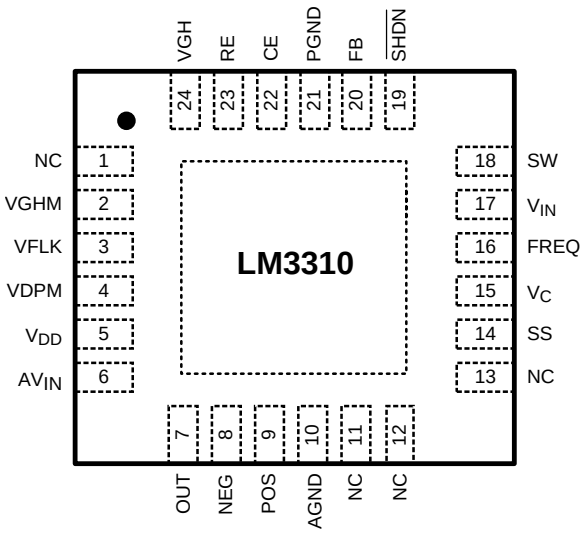


Figure 1. WQFN-24 Package
See Package Number RTW0024A
θ_{JA}=37°C/W

Pin Descriptions

Pin	Name	Function
1	NC	Not internally connected. Leave pin open.
2	VGHM	Output of GPM circuit. This output directly drives the supply for the gate driver circuits.
3	VFLK	Determines when the TFT LCD is on or off. This is controlled by the timing controller in the LCD module.
4	VDPM	VDPM pin is the enable signal for the GPM block. Pulling this pin high enables the GPM while pulling this pin low disables it. VDPM is used for timing sequence control.
5	V_{DD}	Reference input for gate pulse modulation (GPM) circuit. The voltage at V_{DD} is used to set the lower VGHM voltage. If the GPM function is not used connect V_{DD} to V_{IN}.
6	AV_{IN}	Op-Amp analog power input.
7	OUT	Output of the Op-Amp.
8	NEG	Negative input terminal of the Op-Amp.
9	POS	Positive input terminal of the Op-Amp.
10	AGND	Analog ground for the step-up regulator, LDO, and Op-Amp. Connect directly to DAP and PGND beneath the device.
11	NC	Not internally connected. Leave pin open.
12	NC	Not internally connected. Leave pin open.
13	NC	Not internally connected. Leave pin open.
14	SS	Boost converter soft start pin.
15	V_C	Boost compensation network connection. Connected to the output of the voltage error amplifier.
16	FREQ	Switching frequency select input. Connect this pin to V_{IN} for 1.28MHz operation and AGND for 660kHz operation.
17	V_{IN}	Boost converter and GPM power input.
18	SW	Boost power switch input. Switch connected between SW pin and PGND pin.
19	$\overline{SHDN}$	Shutdown pin. Active low, pulling this pin low disable the LM3310.
20	FB	Boost output voltage feedback input.
21	PGND	Power Ground. Source connection of the step-up regulator NMOS switch and ground for the GPM circuit. Connect AGND and PGND directly to the DAP beneath the device.

Pin Descriptions (continued)

Pin	Name	Function
22	CE	Connect capacitor from this pin to AGND.
23	RE	Connect a resistor between RE and PGND.
24	VGH	GPM power supply input. VGH range is 5V to 30V.
DAP		Die Attach Pad. Internally connected to GND. Connect AGND and PGND pins directly to this pad beneath the device.

Block Diagrams

Boost Converter

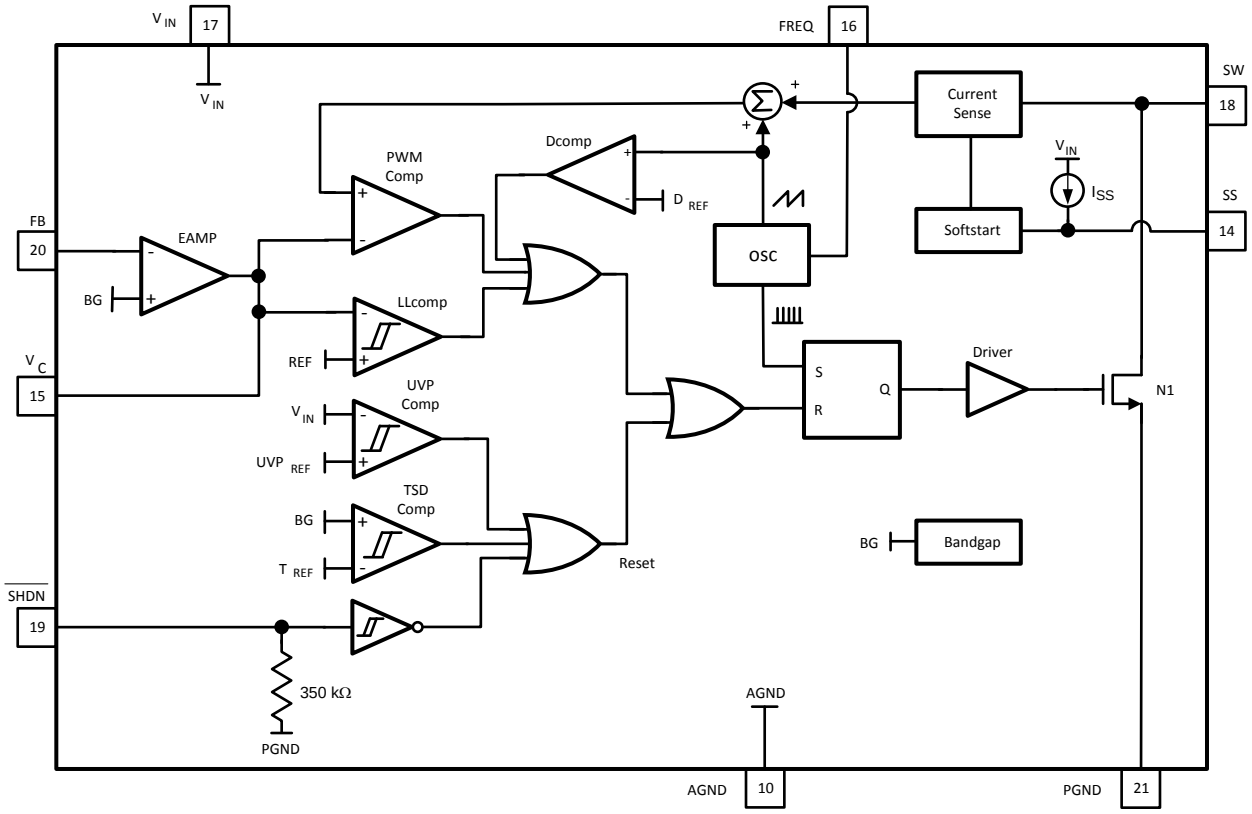


Figure 2.

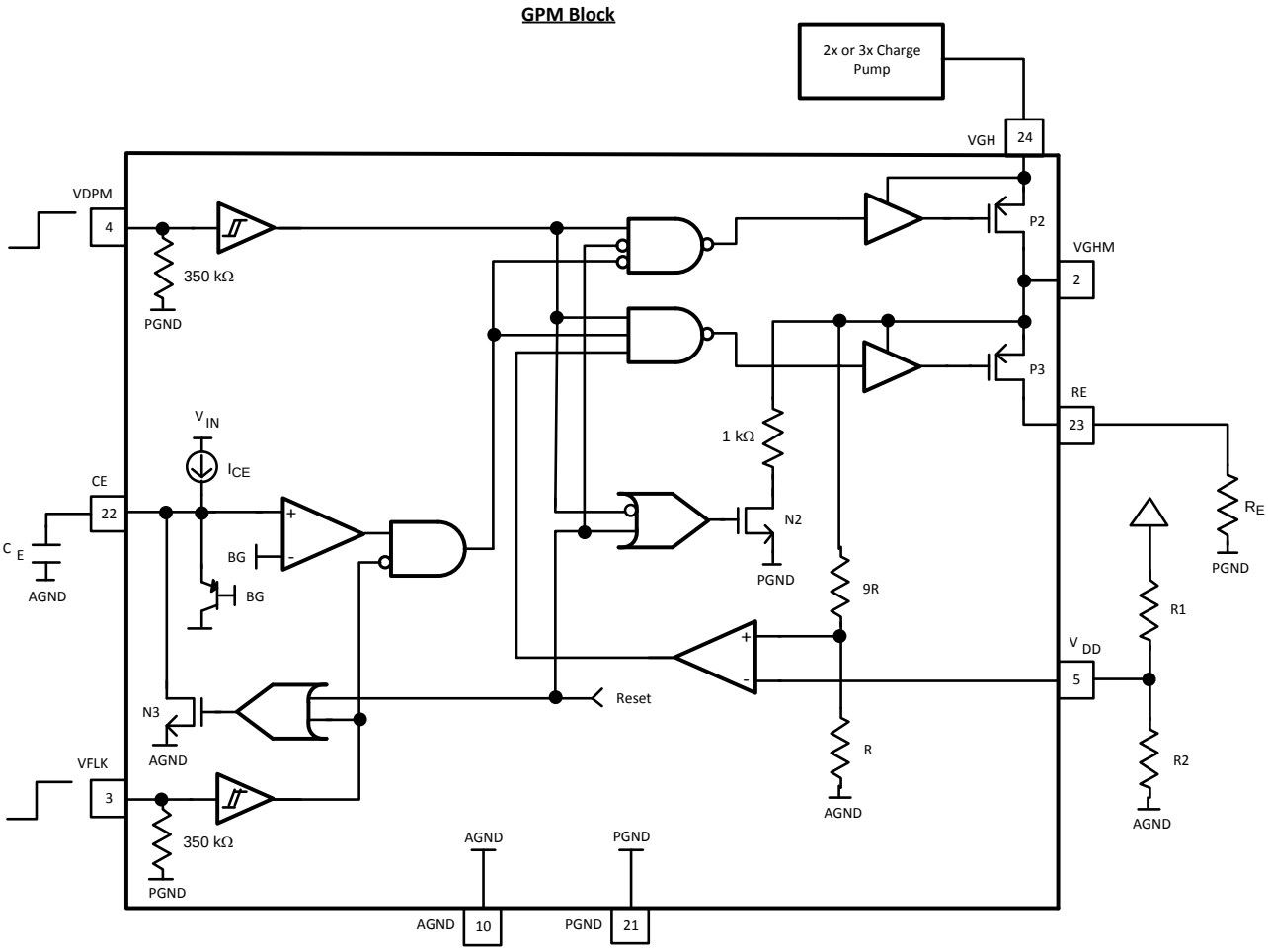


Figure 3.

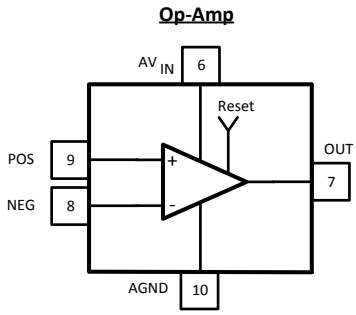


Figure 4.

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

Absolute Maximum Ratings (1)(2)

V_{IN}	7.5V
SW Voltage	21V
FB Voltage	V_{IN}
V_C Voltage (3)	1.265V ± 0.3V
$\overline{SHDN}$ Voltage	7.5V
FREQ	V_{IN}
AV_{IN}	14.5V
Amplifier Inputs/Output	Rail-to-Rail
VGH Voltage	31V
VGHM Voltage	VGH
VFLK, VDPM, V_{DD} Voltage	7.5V
CE Voltage (3)	1.265 + 0.3V
RE Voltage	VGH
Maximum Junction Temperature	150°C
Power Dissipation(4)	Internally Limited
Lead Temperature	300°C
Vapor Phase (60 sec.)	215°C
Infrared (15 sec.)	220°C
ESD Susceptibility (5)	
Human Body Model	2kV

(1) Absolute maximum ratings are limits beyond which damage to the device may occur. Operating Ratings are conditions for which the device is intended to be functional, but device parameter specifications may not be ensured. For specifications and test conditions, see the Electrical Characteristics.
(2) If Military/Aerospace specified devices are required, please contact the Texas Instruments Sales Office/ Distributors for availability and specifications.
(3) Under normal operation the V_C and CE pins may go to voltages above this value. The maximum rating is for the possibility of a voltage being applied to the pin, however the V_C and CE pins should never have a voltage directly applied to them.
(4) The maximum allowable power dissipation is a function of the maximum junction temperature, $T_J(MAX)$, the junction-to-ambient thermal resistance, θ_{JA}, and the ambient temperature, T_A. See the Electrical Characteristics table for the thermal resistance of various layouts. The maximum allowable power dissipation at any ambient temperature is calculated using: $P_D (MAX) = (T_{J(MAX)} - T_A)/\theta_{JA}$. Exceeding the maximum allowable power dissipation will cause excessive die temperature, and the regulator will go into thermal shutdown.
(5) The human body model is a 100pF capacitor discharged through a 1.5kΩ resistor into each pin per JEDEC standard JESD22-A114.

Operating Conditions

Operating Junction Temperature Range (1)	−40°C to +125°C
Storage Temperature	−65°C to +150°C
Supply Voltage	2.5V to 7V
Maximum SW Voltage	20V
VGH Voltage Range	5V to 30V
Op-Amp Supply, AV_{IN}	4V to 14V

(1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).

Electrical Characteristics

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Unless otherwise specified, V_{IN} =2.5V and I_L = 0A.

Parameter		Test Conditions	Min(1)	Typ(2)	Max(1)	Units
I_Q	Quiescent Current	FB = 2V (Not Switching)		690	**1100**	µA
		$V_{\overline{SHDN}}$ = 0V		0.04	0.5 **8.5**	
		660kHz Switching		2.1	**2.8**	mA
		1.28MHz Switching		3.1	**4.0**	
V_{FB}	Feedback Voltage		**1.231**	1.263	**1.287**	V
$\%V_{FB}/\Delta V_{IN}$	Feedback Voltage Line Regulation	2.5V ≤ V_{IN} ≤ 7V	**-0.26**	0.089	**0.42**	%/V
I_{CL}	Switch Current Limit (3)	(4)	**2.0**	2.6		A
I_B	FB Pin Bias Current (5)			27	**160**	nA
I_{SS}	SS Pin Current		**8.5**	11	**13.5**	µA
V_{SS}	SS Pin Voltage		**1.20**	1.24	**1.28**	V
V_{IN}	Input Voltage Range		**2.5**		**7**	V
g_m	Error Amp Transconductance	ΔI = 5µA	**26**	74	**133**	µmho
A_V	Error Amp Voltage Gain			69		V/V
D_{MAX}	Maximum Duty Cycle	f_S = 660kHz	**80**	91		%
		f_S = 1.28MHz	**80**	89		
f_S	Switching Frequency	FREQ = Ground	**440**	660	**760**	kHz
		FREQ = V_{IN}	**1.0**	1.28	**1.5**	MHz
$I_{\overline{SHDN}}$	Shutdown Pin Current	$V_{\overline{SHDN}}$ = 2.5V		8	**13.5**	µA
		$V_{\overline{SHDN}}$ = 0.3V		1	**2**	
I_L	Switch Leakage Current	V_{SW} = 20V		0.03	**5**	µA
R_{DSON}	Switch R_{DSON}	I_{SW} = 500mA		0.18	**0.35**	Ω
Th_{SHDN}	$\overline{SHDN}$ Threshold	Output High, V_{IN} = 2.5V to 7V	**1.4**			V
		Output Low, V_{IN} = 2.5V to 7V			**0.4**	
UVP	Undervoltage Protection Threshold	On Threshold (Switch On)	**2.5**	2.4		V
		Off Threshold (Switch Off)		2.3	**2.1**	
I_{FREQ}	FREQ Pin Current	FREQ = V_{IN} = 2.5V		2.7	**13.5**	µA
Operational Amplifier						
V_{OS}	Input Offset Voltage	Buffer configuration, V_O = AV_{IN}/2, no load		5.7	**15**	mV
I_B	Input Bias Current (POS Pin)	Buffer configuration, V_O = AV_{IN}/2, no load (5)		200	**550**	nA
V_{OUT} Swing		Buffer, R_L=2kΩ, V_O min.		0.001	**0.03**	V
		Buffer, R_L=2kΩ, V_O max.	**7.9**	7.97		
AV_{IN}	Supply Voltage		**4**		**14**	V
Is+	Supply Current	Buffer, V_O = AV_{IN}/2, No Load		1.5	**7.8**	mA
I_{OUT}	Output Current	Source	**90**	138	**195**	mA
		Sink	**105**	135	**175**	
Gate Pulse Modulation						
VFLK	VFLK Voltage Levels	Rising edge threshold			**1.4**	V
		Falling edge threshold	**0.4**			

(1) All limits specified at room temperature (standard typeface) and at temperature extremes (bold typeface). All room temperature limits are 100% production tested. All limits at temperature extremes are specified via correlation using standard Statistical Quality Control (SQC) methods. All limits are used to calculate Average Outgoing Quality Level (AOQL).
(2) Typical numbers are at 25°C and represent the most likely norm.
(3) Duty cycle affects current limit due to ramp generator.
(4) Current limit at 0% duty cycle. See Typical Performance Characteristics section for Switch Current Limit vs. V_{IN}
(5) Bias current flows into pin.

Electrical Characteristics (continued)

Specifications in standard type face are for T_J = 25°C and those with **boldface type** apply over the full **Operating Temperature Range** (T_J = −40°C to +125°C). Unless otherwise specified, V_{IN} =2.5V and I_L = 0A.

Parameter		Test Conditions	Min(1)	Typ(2)	Max(1)	Units
VDPM	VDPM Voltage Levels	Rising edge threshold			**1.4**	V
		Falling edge threshold	**0.4**			
$V_{DD(TH)}$	V_{DD} Threshold	VGHM = 30V	**2.8**	3	**3.3**	V
		VGHM = 5V	**0.4**	0.5	**0.7**	
I_{VFLK}	VFLK Current	VFLK = 1.5V		4.8	**11**	µA
		VFLK = 0.3V		1.1	**2.5**	
I_{VDPM}	VDPM Current	VDPM = 1.5V		4.8	**11**	µA
		VDPM = 0.3V		1.1	**2.5**	
I_{VGH}	VGH Bias Current	VGH = 30V, VFLK High		59	**300**	µA
		VGH = 30V, VFLK Low		11	**35.5**	
$R_{VGH-VGHM}$	VGH to VGHM Resistance	20mA Current, VGH = 30V		14	**28.5**	Ω
$R_{VGHM-RE}$	VGHM to RE Resistance	20mA Current, VGH = VGHM = 30V		27	**55**	
$R_{VGHM(OFF)}$	VGH Resistance	VDPM is Low, VGHM = 2V		1.2	**1.7**	kΩ
I_{CE}	CE Current	CE = 0V	**7**	11	**16**	µA
$V_{CE(TH)}$	CE Voltage Threshold		**1.16**	1.22	**1.34**	V

Typical Performance Characteristics

$\overline{\text{SHDN}}$ Pin Current vs. $\overline{\text{SHDN}}$ Pin Voltage

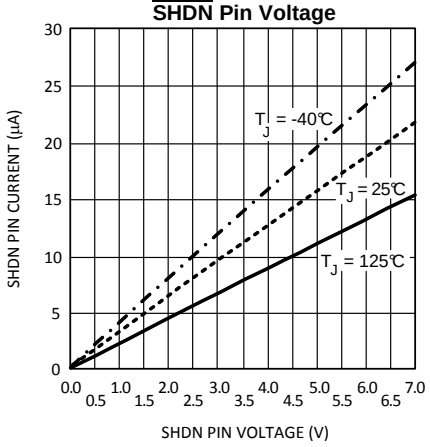


Figure 5.

SS Pin Current vs. Input Voltage

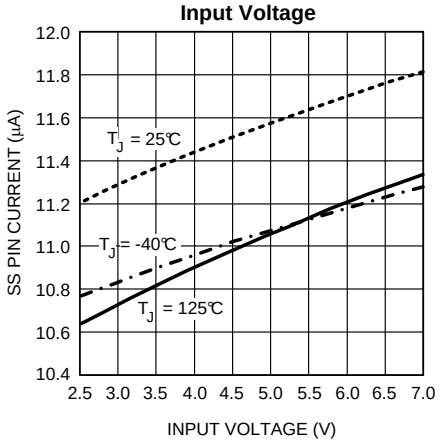


Figure 6.

FREQ Pin Current vs. Input Voltage

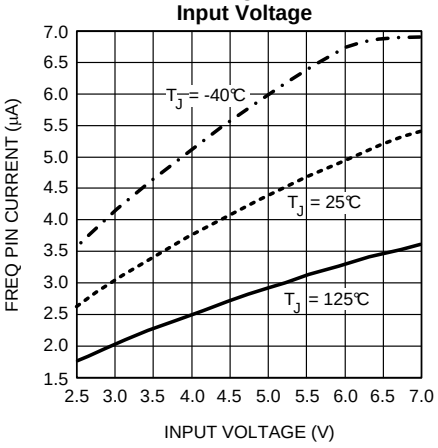


Figure 7.

FB Pin Current vs. Temperature

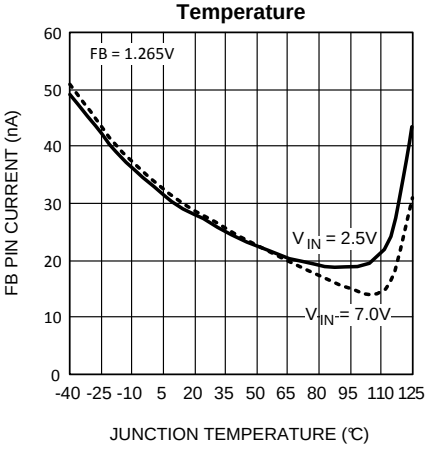


Figure 8.

CE Pin Current vs. Input Voltage

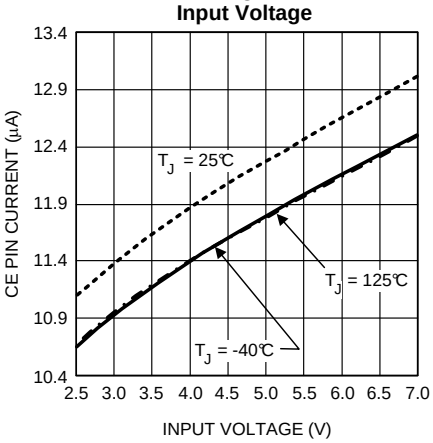


Figure 9.

VDPM Pin Current vs. VDPM Pin Voltage

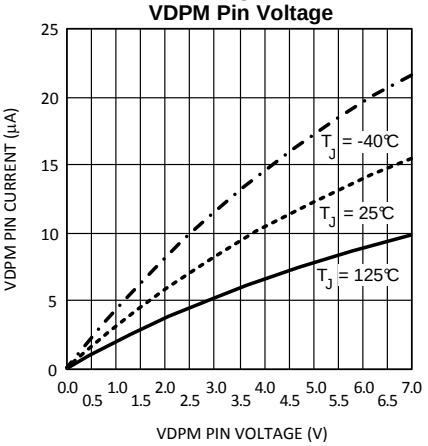


Figure 10.

Typical Performance Characteristics (continued)

VFLK Pin Current vs. VFLK Pin Voltage

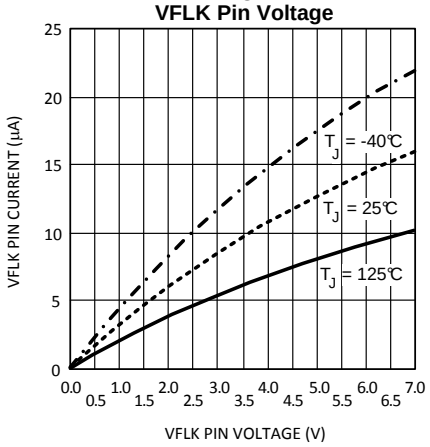


Figure 11.

660kHz Switching Quiescent Current vs. Input Voltage

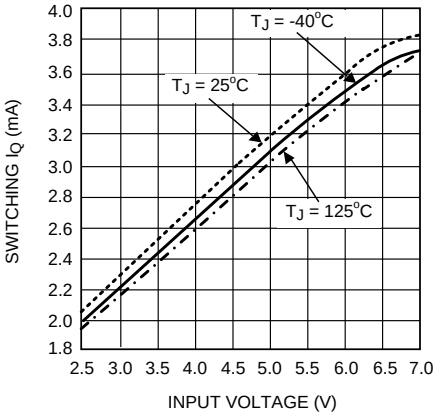


Figure 12.

1.28MHz Switching Quiescent Current vs. Input Voltage

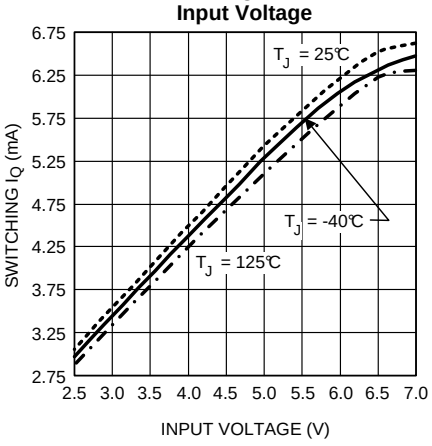


Figure 13.

660kHz Switching Quiescent Current vs. Temperature

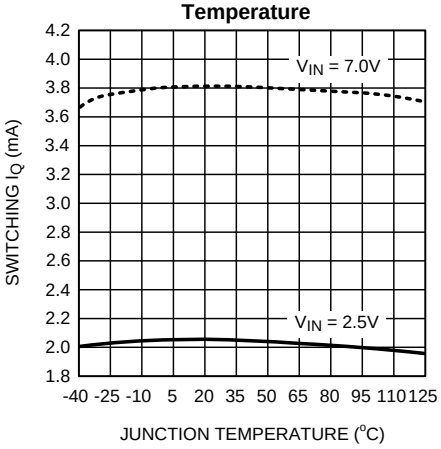


Figure 14.

1.28MHz Switching Quiescent Current vs. Temperature

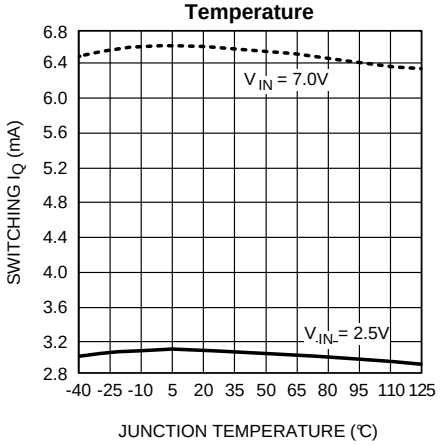


Figure 15.

660kHz Switching Frequency vs. Temperature

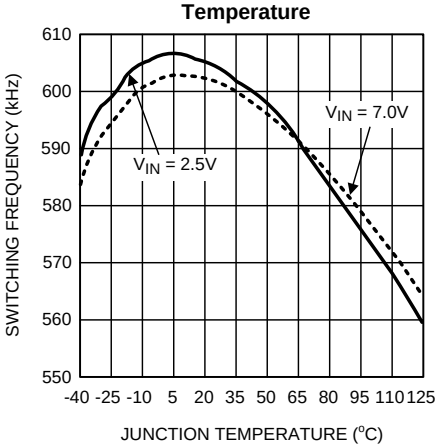


Figure 16.

Typical Performance Characteristics (continued)

1.28MHz Switching Frequency vs. Temperature

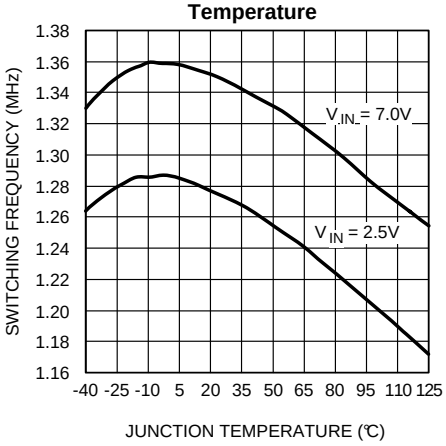


Figure 17.

Switch Current Limit vs. Input Voltage

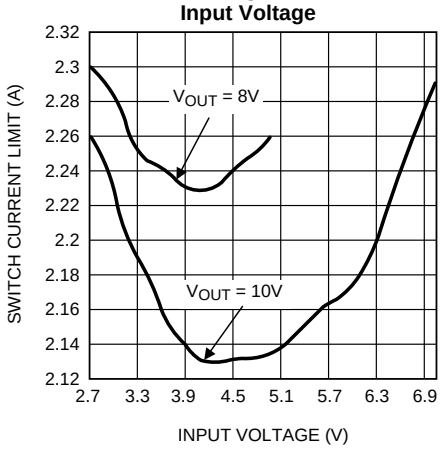


Figure 18.

Non-Switching Quiescent Current vs. Input Voltage GPM Disabled

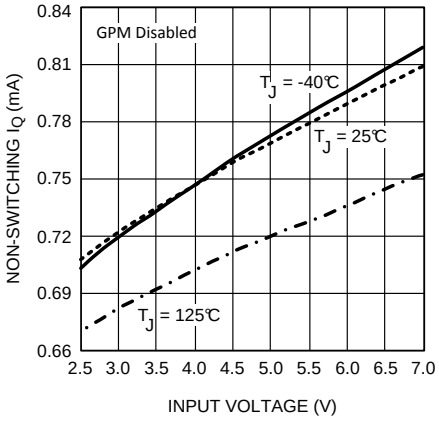


Figure 19.

Non-Switching Quiescent Current vs. Input Voltage GPM Enabled

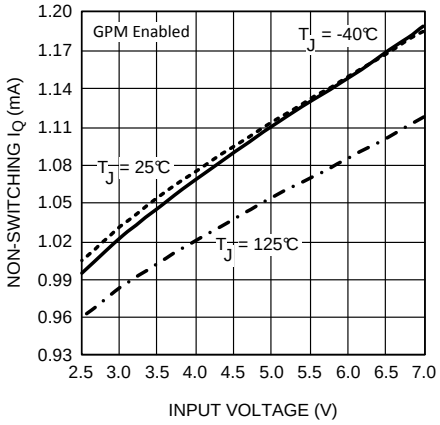


Figure 20.

Non-Switching Quiescent Current vs. Temperature GPM Disabled

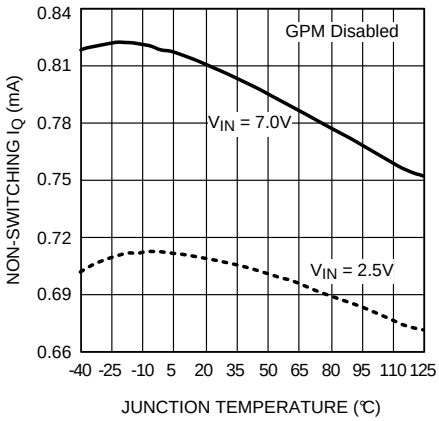


Figure 21.

Non-Switching Quiescent Current vs. Temperature GPM Enabled

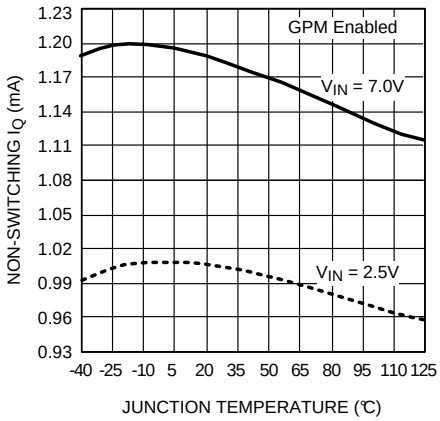


Figure 22.

Typical Performance Characteristics (continued)

Power NMOS R_{DSON} vs. Input Voltage

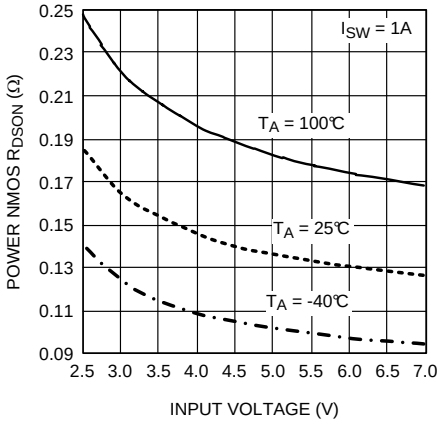


Figure 23.

660kHz Max. Duty Cycle vs. Input Voltage

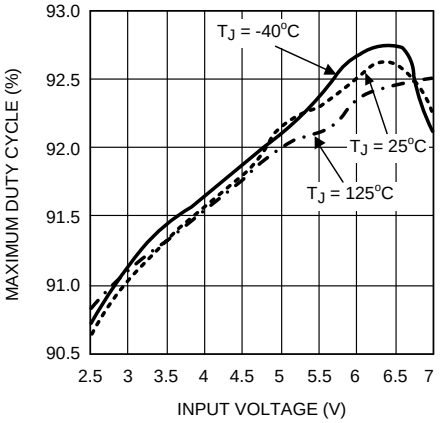


Figure 24.

1.28MHz Max. Duty Cycle vs. Input Voltage

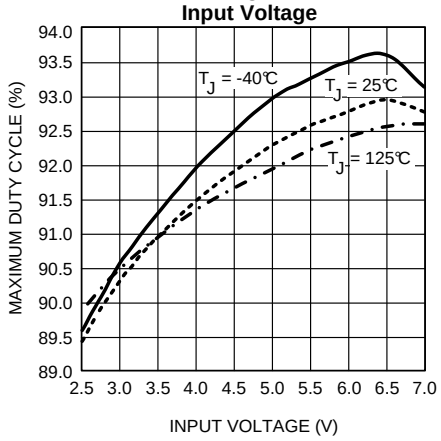


Figure 25.

660kHz Max. Duty Cycle vs. Temperature

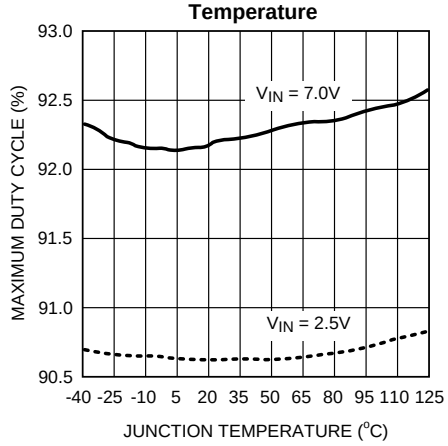


Figure 26.

1.28MHz Max. Duty Cycle vs. Temperature

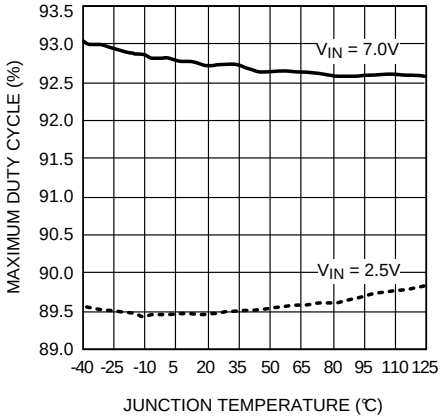


Figure 27.

1.28MHz Application Efficiency

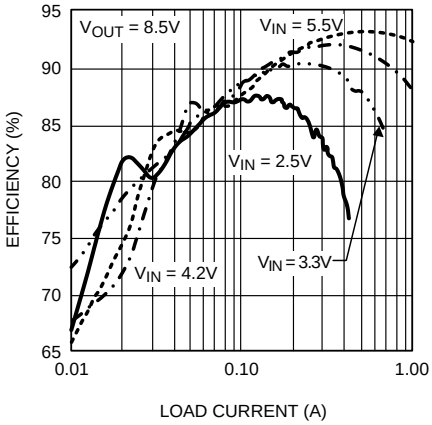


Figure 28.

Typical Performance Characteristics (continued)

1.28MHz Application Efficiency

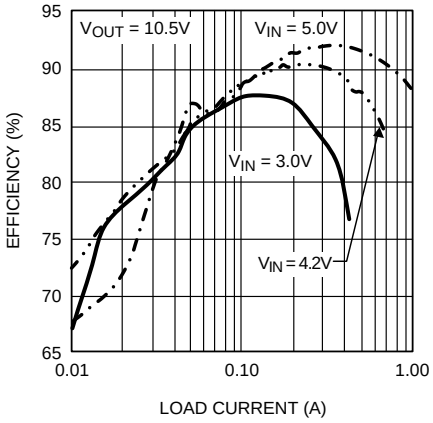


Figure 29.

VGH Pin Bias Current vs. VGH Pin Voltage

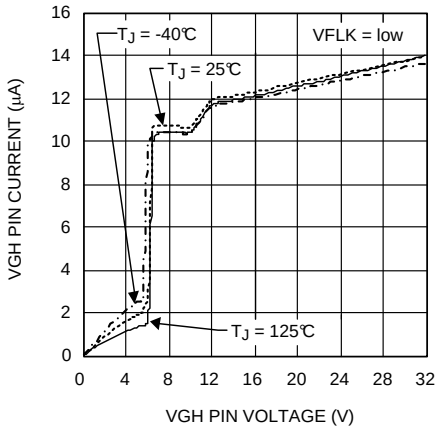


Figure 30.

VGH Pin Bias Current vs. VGH Pin Voltage

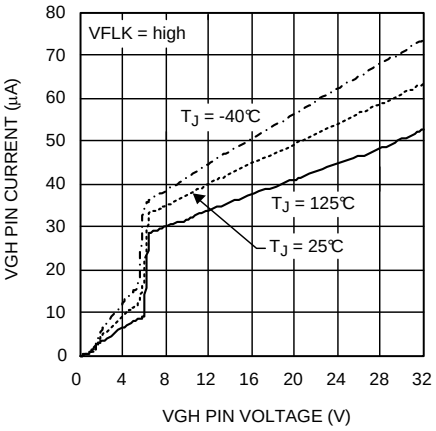


Figure 31.

VGH-VGHM PMOS R_{DSON} vs. VGH Pin Voltage

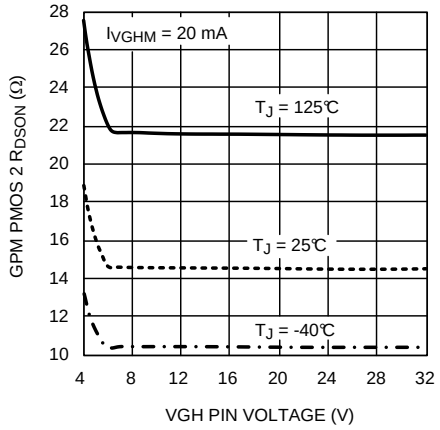


Figure 32.

VGHM-RE PMOS R_{DSON} vs. VGHM Pin Voltage

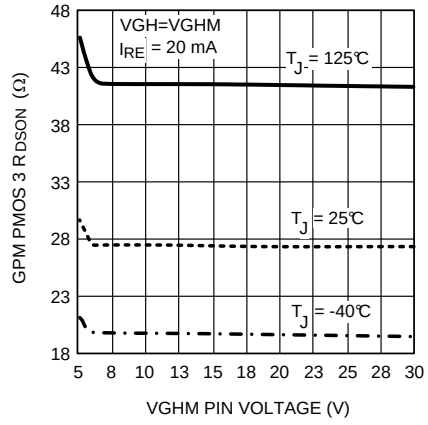


Figure 33.

VGHM OFF Resistance vs. Temperature

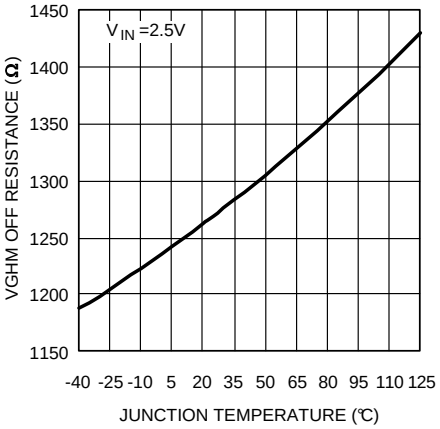


Figure 34.

Typical Performance Characteristics (continued)

Op-Amp Source Current vs. AV_{IN}

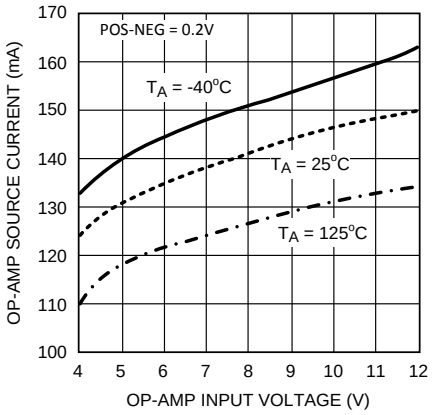


Figure 35.

Op-Amp Sink Current vs. AV_{IN}

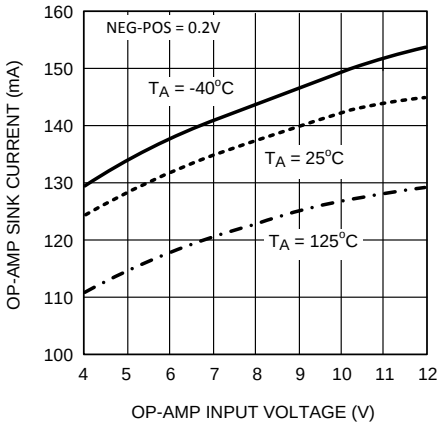


Figure 36.

Op-Amp Quiescent Current vs. AV_{IN}

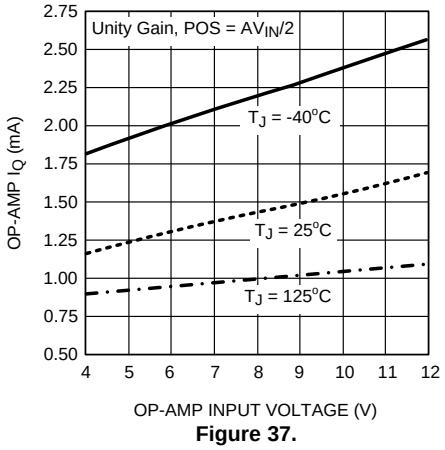


Figure 37.

Op-Amp Offset Voltage vs. AV_{IN} (No Load)

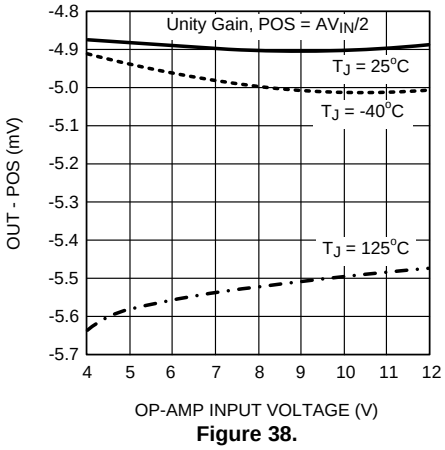


Figure 38.

Op-Amp Offset Voltage vs. Load Current

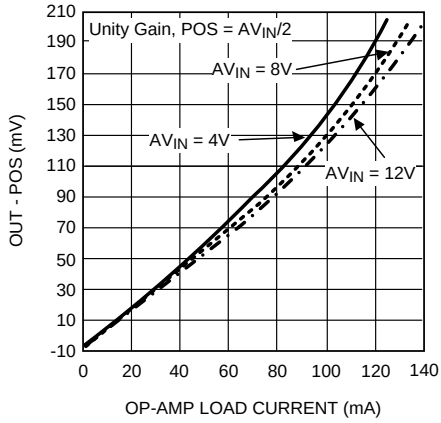
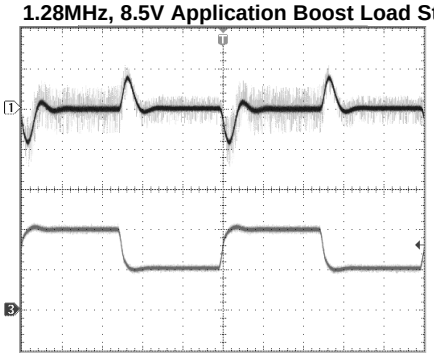


Figure 39.

1.28MHz, 8.5V Application Boost Load Step

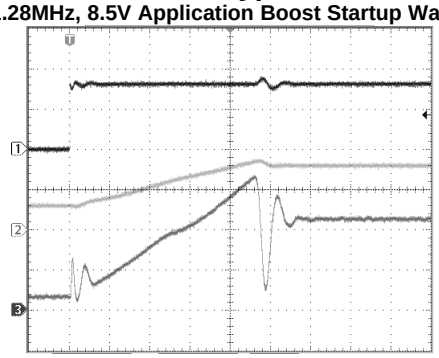


V_{OUT} = 8.5V, V_{IN} = 3.3V, C_{OUT} = 20µF
1) V_{OUT}, 200mV/div, AC
3) I_{LOAD}, 200mA/div, DC
T = 200µs/div

Figure 40.

Typical Performance Characteristics (continued)

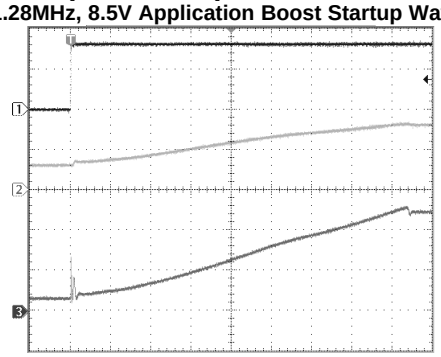
1.28MHz, 8.5V Application Boost Startup Waveform



V_{OUT} = 8.5V, V_{IN} = 3.3V, C_{OUT} = 20µF, R_{LOAD} = 20Ω, C_{SS} = 10nF
1) V_{SHDN}, 2V/div, DC
2) V_{OUT}, 5V/div, DC
3) I_{IN}, 500mA/div, DC
T = 200µs/div

Figure 41.

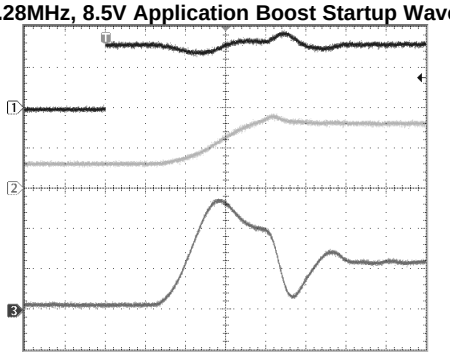
1.28MHz, 8.5V Application Boost Startup Waveform



V_{OUT} = 8.5V, V_{IN} = 3.3V, C_{OUT} = 20µF, R_{LOAD} = 20Ω, C_{SS} = 100nF
1) V_{SHDN}, 2V/div, DC
2) V_{OUT}, 5V/div, DC
3) I_{IN}, 500mA/div, DC
T = 1ms/div

Figure 42.

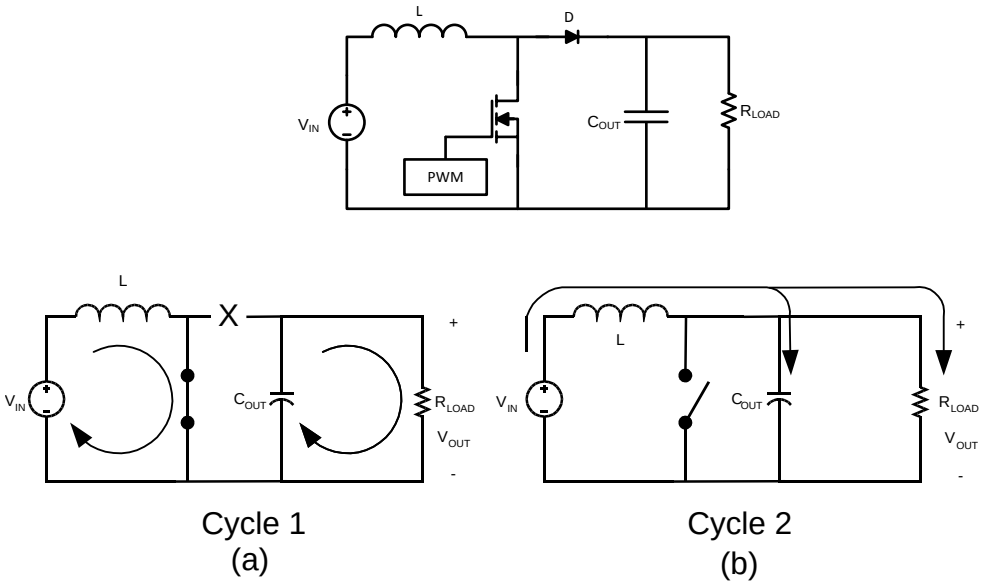
1.28MHz, 8.5V Application Boost Startup Waveform



V_{OUT} = 8.5V, V_{IN} = 3.3V, C_{OUT} = 20µF, R_{LOAD} = 20Ω, C_{SS} = open
1) V_{SHDN}, 2V/div, DC
2) V_{OUT}, 5V/div, DC
3) I_{IN}, 1A/div, DC
T = 40µs/div

Figure 43.

Operation



(a) First Cycle of Operation
(b) Second Cycle Of Operation

Figure 44. Simplified Boost Converter Diagram

CONTINUOUS CONDUCTION MODE

The LM3310 contains a current-mode, PWM boost regulator. A boost regulator steps the input voltage up to a higher output voltage. In continuous conduction mode (when the inductor current never reaches zero at steady state), the boost regulator operates in two cycles.

In the first cycle of operation, shown in Figure 44 (a), the transistor is closed and the diode is reverse biased. Energy is collected in the inductor and the load current is supplied by C_{OUT}.

The second cycle is shown in Figure 44 (b). During this cycle, the transistor is open and the diode is forward biased. The energy stored in the inductor is transferred to the load and output capacitor.

The ratio of these two cycles determines the output voltage. The output voltage is defined approximately as:

$$V_{OUT} = \frac{V_{IN}}{1-D}, \; D' = (1-D) = \frac{V_{IN}}{V_{OUT}} \tag{1}$$

where

- D is the duty cycle of the switch
- D and D′ will be required for design calculations

SETTING THE OUTPUT VOLTAGE (BOOST CONVERTER)

The output voltage is set using the feedback pin and a resistor divider connected to the output as shown in the Typical Application Circuit. The feedback pin voltage is 1.263V, so the ratio of the feedback resistors sets the output voltage according to the following equation:

$$R_{FB1} = R_{FB2} \times \frac{V_{OUT} - 1.263}{1.263} \; \Omega \tag{2}$$

SOFT-START CAPACITOR

The LM3310 has a soft-start pin that can be used to limit the inductor inrush current on start-up. The external SS pin is used to tailor the soft-start for a specific application but is not required for all applications and can be left open when not needed. When used a current source charges the external soft-start capacitor C_{SS} until it reaches its typical clamp voltage, V_{SS}. The soft-start time can be estimated as:

$$T_{SS} = C_{SS} * V_{SS} / I_{SS} \quad (3)$$

THERMAL SHUTDOWN

The LM3310 includes thermal shutdown. If the die temperature reaches 145°C the device will shut down until it cools to a safe temperature at which point the device will resume operation. If the adverse condition that is heating the device is not removed (ambient temperature too high, short circuit conditions, etc...) the device will continue to cycle on and off to keep the die temperature below 145°C. The thermal shutdown has approximately 20°C of hysteresis. When in thermal shutdown the boost regulator, Op-Amp, and GPM blocks will all be disabled.

INPUT UNDER-VOLTAGE PROTECTION

The LM3310 includes input under-voltage protection (UVP). The purpose of the UVP is to protect the device both during start-up and during normal operation from trying to operate with insufficient input voltage. During start-up using a ramping input voltage the UVP circuitry ensures that the device does not begin switching until the input voltage reaches the UVP On threshold. If the input voltage is present and the shutdown pin is pulled high the UVP circuitry will prevent the device from switching if the input voltage present is lower than the UVP On threshold. During normal operation the UVP circuitry will disable the device if the input voltage falls below the UVP Off threshold for any reason. In this case the device will not turn back on until the UVP On threshold voltage is exceeded.

OPERATIONAL AMPLIFIER

Compensation:

The architecture used for the amplifier in the LM3310 requires external compensation on the output. Depending on the equivalent resistive and capacitive distributed load of the TFT-LCD panel, external components at the amplifier outputs may or may not be necessary. If the capacitance presented by the load is equal to or greater than an equivalent distibutive load of 50Ω in series with 4.7nF no external components are needed as the TFT-LCD panel will act as compensation itself. Distributed resistive and capacitive loads enhance stability and increase performance of the amplifiers. If the capacitance and resistance presented by the load is less than 50Ω in series with 4.7nF, external components will be required as the load itself will not ensure stability. No external compensation in this case will lead to oscillation of the amplifier and an increase in power consumption. A good choice for compensation in this case is to add a 50Ω in series with a 4.7nF capacitor from the output of the amplifier to ground. This allows for driving zero to infinite capacitance loads with no oscillations, minimal overshoot, and a higher slew rate than using a single large capacitor. The high phase margin created by the external compensation will ensure stability and good performance for all conditions.

Layout and Filtering considerations:

When the power supply for the amplifiers (AV_{IN}) is connected to the output of the switching regulator, the output ripple of the regulator will produce ripple at the output of the amplifiers. This can be minimized by directly bypassing the AV_{IN} pin to ground with a low ESR ceramic capacitor. For best noise reduction a resistor on the order of 5Ω to 20Ω from the supply being used to the AV_{IN} pin will create and RC filter and give you a cleaner supply to the amplifier. The bypass capacitor should be placed as close to the AV_{IN} pin as possible and connected directly to the AGND plane.

For best noise immunity all bias and feedback resistors should be in the low kΩ range due to the high input impedance of the amplifier. It is good practice to use a small capacitance at the high impedance input terminals as well to reduce noise susceptibility. All resistors and capacitors should be placed as close to the input pins as possible.

Special care should also be taken in routing of the PCB traces. All traces should be as short and direct as possible. The output pin trace must never be routed near any trace going to the positive input. If this happens cross talk from the output trace to the positive input trace will cause the circuit to oscillate.

The op-amp is not a three terminal device it has 5 terminals: positive voltage power pin, AGND, positive input, negative input, and the output. The op-amp "routes" current from the power input pin and AGND to the output pin. So in effect an opamp has not two inputs but four, all of which must be kept noise free relative to the external circuits which are being driven by the op-amp. The current from the power pins goes through the output pin and into the load and feedback loop. The current exiting the load and feedback loops then must have a return path back to the op-amp power supply pins. Ideally this return path must follow the same path as the output pin trace to the load. Any deviation that makes the loop area larger between the output current path and the return current path adds to the probability of noise pick up.

GATE PULSE MODULATION

The Gate Pulse Modulation (GPM) block is designed to provide a modulated voltage to the gate driver circuitry of a TFT LCD display. Operation is best understood by referring to the GPM block diagram in the Block Diagrams section, the drawing in Figure 45 and the transient waveforms in Figure 46 and Figure 47.

There are two control signals in the GPM block, VDPM and VFLK. VDPM is the enable pin for the GPM block. If VDPM is high, the GPM block is active and will respond to the VFLK drive signal from the timing controller. However, if VDPM is low, the GPM block will be disabled and both PMOS switches P2 and P3 will be turned off. The VGHM node will be discharged through a 1kΩ resistor and the NMOS switch N2.

When VDPM is high, typical waveforms for the GPM block can be seen in Figure 45. The pin VGH is typically driven by a 2x or 3x charge pump. In most cases, the 2x or 3x charge pump is a discrete solution driven from the SW pin and the output of the boost switching regulator. When VFLK is high, the PMOS switch P2 is turned on and the PMOS switch P3 is turned off. With P2 on, the VGHM pin is pulled to the same voltage applied to the VGH pin. This provides a high gate drive voltage, $VGHM_{MAX}$, and can source current to the gate drive circuitry. When VFLK is high, NMOS switch N3 is on which discharges the capacitor CE.

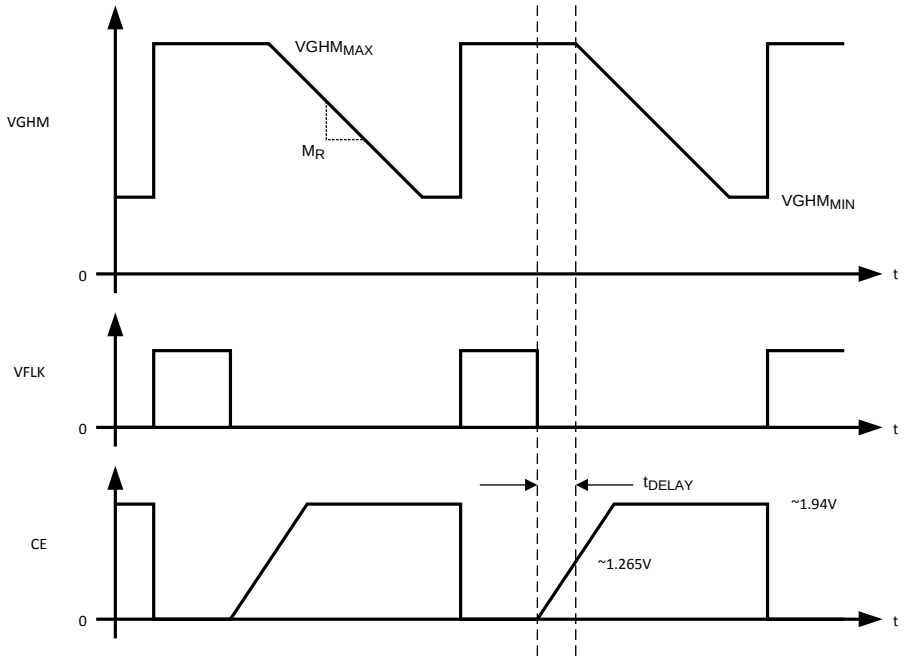


Figure 45.

When VFLK is low, the NMOS switch N3 is turned off which allows current to charge the C_E capacitor. This creates a delay, t_{DELAY}, given by the following equations:

$$t_{DELAY} \cong 1.265V(C_E + 7pF)/I_{CE} \quad (4)$$

When the voltage on CE reaches about 1.265V and the VFLK signal is low, the PMOS switch P2 will turn off and the PMOS switch P3 will turn on connecting resistor R3 to the VGHM pin through P3. This will discharge the voltage at VGHM at some rate determined by R3 creating a slope, M_R, as shown in Figure 45. The VGHM pin is no longer a current source, it is now sinking current from the gate drive circuitry.

As VGHM is discharged through R3, the comparator connected to the pin V_{DD} monitors the VGHM voltage. PMOS switch P3 will turn off when the following is true:

$$VGHM_{MIN} \cong 10V_X R2/(R1 + R2) \quad (5)$$

where

- V_X is some voltage connected to the resistor divider on pin V_{DD}

V_X is typically connected to the output of the boost switching regulator. When PMOS switch P3 turns off, VGHM will be high impedance until the VFLK pin is high again.

Figure 46 and Figure 47 give typical transient waveforms for the GPM block. Waveform (1) is the VGHM pin, (2) is the VFLK and (3) is the VDPM. The output of the boost switching regulator is operating at 8.5V and there is a 3x discrete charge pump (~23.5V) supplying the VGH pin. In Figure 46 and Figure 47, the VGHM pin is driving a purely capacitive load, 4.7nF. The value of resistor R1 is 15kohm, R2 is 1.1kΩ and R3 is 750Ω. In both transient plots, there is no C_E delay capacitor.

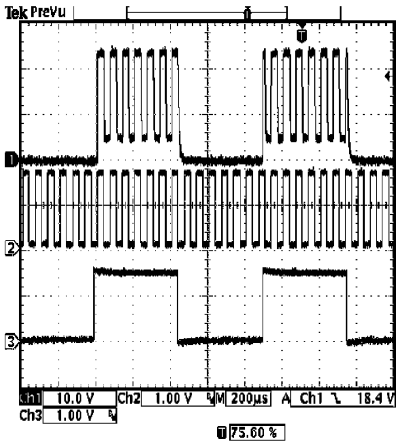


Figure 46. Waveform

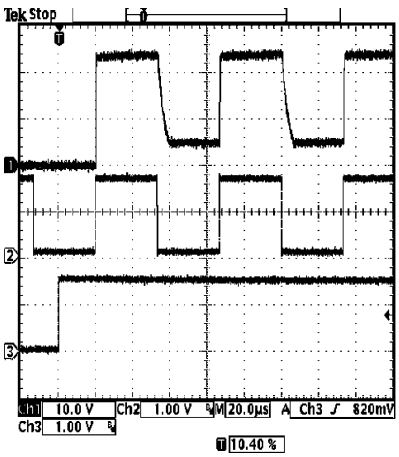
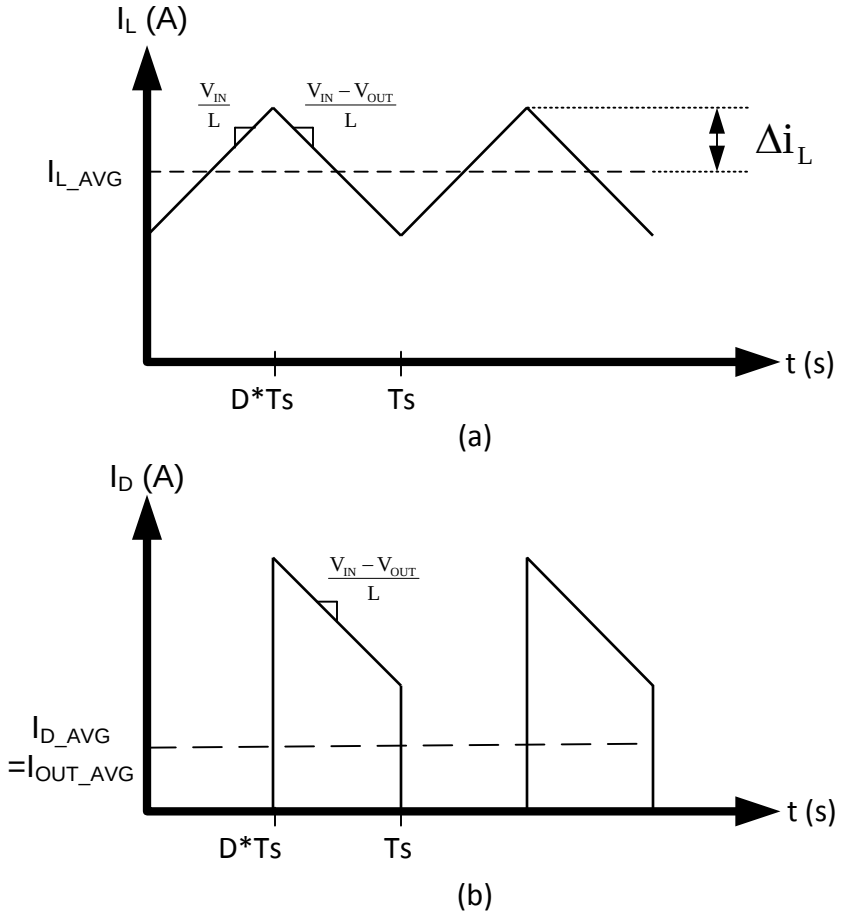


Figure 47. Waveform

In the GPM block diagram, a signal called “Reset” is shown. This signal is generated from the V_{IN} under-voltage lockout, thermal shutdown, or the $\overline{SHDN}$ pin. If the V_{IN} supply voltage drops below 2.3V, typically, then the GPM block will be disabled and the VGHM pin will discharge through NMOS switch N2 and the 1kΩ resistor. This applies also if the junction temperature of the device exceeds 145°C or if the $\overline{SHDN}$ signal is low. As shown in the Block Diagrams, both VDPM and VFLK have internal 350kΩ pull down resistors. This puts both VDPM and VFLK in normally “off” states. Typical VDPM and VFLK pin currents can be found in the Typical Performance Characteristics section.

INTRODUCTION TO COMPENSATION (BOOST CONVERTER)



(a) Inductor current
(b) Diode current

Figure 48.

The LM3310 is a current mode PWM boost converter. The signal flow of this control scheme has two feedback loops, one that senses switch current and one that senses output voltage.

To keep a current programmed control converter stable above duty cycles of 50%, the inductor must meet certain criteria. The inductor, along with input and output voltage, will determine the slope of the current through the inductor (see Figure 48 (a)). If the slope of the inductor current is too great, the circuit will be unstable above duty cycles of 50%. A 10µH inductor is recommended for most 660 kHz applications, while a 4.7µH inductor may be used for most 1.28 MHz applications. If the duty cycle is approaching the maximum of 85%, it may be necessary to increase the inductance by as much as 2X. See INDUCTOR AND DIODE SELECTION for more detailed inductor sizing.

The LM3310 provides a compensation pin (V_C) to customize the voltage loop feedback. It is recommended that a series combination of R_C and C_C be used for the compensation network, as shown in the Typical Application Circuit. For any given application, there exists a unique combination of R_C and C_C that will optimize the performance of the LM3310 circuit in terms of its transient response. The series combination of R_C and C_C introduces a pole-zero pair according to the following equations:

$$f_{ZC} = \frac{1}{2\pi R_C C_C} \text{ Hz}$$

$$f_{PC} = \frac{1}{2\pi (R_C + R_O) C_C} \text{ Hz} \quad (6)$$

where

- R_O is the output impedance of the error amplifier, approximately 900kΩ (7)

For most applications, performance can be optimized by choosing values within the range 5kΩ ≤ R_C ≤ 100kΩ (R_C can be up to 200kΩ if C_{C2} is used, see HIGH OUTPUT CAPACITOR ESR COMPENSATION) and 68pF ≤ C_C ≤ 4.7nF. Refer to the Application Information section for recommended values for specific circuits and conditions. Refer to the COMPENSATION section for other design requirement.

COMPENSATION

This section will present a general design procedure to help insure a stable and operational circuit. The designs in this datasheet are optimized for particular requirements. If different conversions are required, some of the components may need to be changed to ensure stability. Below is a set of general guidelines in designing a stable circuit for continuous conduction operation, in most all cases this will provide for stability during discontinuous operation as well. The power components and their effects will be determined first, then the compensation components will be chosen to produce stability.

INDUCTOR AND DIODE SELECTION

Although the inductor sizes mentioned earlier are fine for most applications, a more exact value can be calculated. To ensure stability at duty cycles above 50%, the inductor must have some minimum value determined by the minimum input voltage and the maximum output voltage. This equation is:

$$L > \frac{V_{IN} R_{DSON}}{0.144\ fs} \left[\frac{D}{D'} - 1 \right] \text{ (in H)}$$

where

- fs is the switching frequency
- D is the duty cycle
- R_{DSON} is the ON resistance of the internal switch taken from the graph "R_{DSON} vs. V_{IN}" in the Typical Performance Characteristics section (8)

This equation is only good for duty cycles greater than 50% (D>0.5), for duty cycles less than 50% the recommended values may be used. The value given by this equation is the inductance necessary to supress sub-harmonic oscillations. In some cases the value given by this equation may be too small for a given application. In this case the average inductor current and the inductor current ripple must be considered.

The corresponding inductor current ripple, average inductor current, and peak inductor current as shown in Figure 48 (a) is given by:

$$\Delta i_L = \frac{V_{IN} D}{2Lfs} \text{ (in Amps)} \quad (9)$$

$$i_{L(AVE)} \approx \frac{I_{OUT}}{\eta D'} \quad (10)$$

$$i_{L(PEAK)} \approx i_{L(AVE)} + \Delta i_L \quad (11)$$

Continuous conduction mode occurs when Δi_L is less than the average inductor current and discontinuous conduction mode occurs when Δi_L is greater than the average inductor current. Care must be taken to make sure that the switch will not reach its current limit during normal operation. The inductor must also be sized accordingly. It should have a saturation current rating higher than the peak inductor current expected. The output voltage ripple is also affected by the total ripple current.

The output diode for a boost regulator must be chosen correctly depending on the output voltage and the output current. The typical current waveform for the diode in continuous conduction mode is shown in Figure 48 (b). The diode must be rated for a reverse voltage equal to or greater than the output voltage used. The average current rating must be greater than the maximum load current expected, and the peak current rating must be greater than the peak inductor current. During short circuit testing, or if short circuit conditions are possible in the application, the diode current rating must exceed the switch current limit. Using Schottky diodes with lower forward voltage drop will decrease power dissipation and increase efficiency.

DC GAIN AND OPEN-LOOP GAIN

Since the control stage of the converter forms a complete feedback loop with the power components, it forms a closed-loop system that must be stabilized to avoid positive feedback and instability. A value for open-loop DC gain will be required, from which you can calculate, or place, poles and zeros to determine the crossover frequency and the phase margin. A high phase margin (greater than 45°) is desired for the best stability and transient response. For the purpose of stabilizing the LM3310, choosing a crossover point well below where the right half plane zero is located will ensure sufficient phase margin.

To ensure a bandwidth of ½ or less of the frequency of the RHP zero, calculate the open-loop DC gain, A_{DC}. After this value is known, you can calculate the crossover visually by placing a −20dB/decade slope at each pole, and a +20dB/decade slope for each zero. The point at which the gain plot crosses unity gain, or 0dB, is the crossover frequency. If the crossover frequency is less than ½ the RHP zero, the phase margin should be high enough for stability. The phase margin can also be improved by adding C_{C2} as discussed later in this section. The equation for A_{DC} is given below with additional equations required for the calculation:

$$A_{DC(DB)} = 20\log_{10}\left\langle\left(\frac{R_{FB2}}{R_{FB1} + R_{FB2}}\right)\frac{g_m R_O D'}{R_{DSON}}\{[(\omega cLeff)// R_L]//R_L\}\right\rangle \text{ (in dB)}$$

where

- R_L is the minimum load resistance
- g_m is the error amplifier transconductance found in the Electrical Characteristics table

(12)

$$\omega c \cong \frac{2fs}{nD'} \text{ (in rad/s)} \quad (13)$$

$$Leff = \frac{L}{(D')^2} \quad (14)$$

$$n = 1 + \frac{2mc}{m1} \text{ (no unit)} \quad (15)$$

$$mc \cong 0.072fs \text{ (in V/s)} \quad (16)$$

$$m1 \cong \frac{V_{IN}R_{DSON}}{L} \text{ (in V/s)}$$

where

- V_{IN} is the minimum input voltage
- R_{DSON} is the value chosen from the graph "NMOS R_{DSON} vs. Input Voltage" in the Typical Performance Characteristics section

(17)

INPUT AND OUTPUT CAPACITOR SELECTION

The switching action of a boost regulator causes a triangular voltage waveform at the input. A capacitor is required to reduce the input ripple and noise for proper operation of the regulator. The size used is dependant on the application and board layout. If the regulator will be loaded uniformly, with very little load changes, and at lower current outputs, the input capacitor size can often be reduced. The size can also be reduced if the input of the regulator is very close to the source output. The size will generally need to be larger for applications where the regulator is supplying nearly the maximum rated output or if large load steps are expected. A minimum value of 10µF should be used for the less stressful condtions while a 22µF to 47µF capacitor may be required for higher power and dynamic loads. Larger values and/or lower ESR may be needed if the application requires very low ripple on the input source voltage.

The choice of output capacitors is also somewhat arbitrary and depends on the design requirements for output voltage ripple. It is recommended that low ESR (Equivalent Series Resistance, denoted R_{ESR}) capacitors be used such as ceramic, polymer electrolytic, or low ESR tantalum. Higher ESR capacitors may be used but will require more compensation which will be explained later on in the section. The ESR is also important because it determines the peak to peak output voltage ripple according to the approximate equation:

$$\Delta V_{OUT} \cong 2\Delta i_L R_{ESR} \text{ (in Volts)} \quad (18)$$

A minimum value of 10µF is recommended and may be increased to a larger value. After choosing the output capacitor you can determine a pole-zero pair introduced into the control loop by the following equations:

$$f_{P1} = \frac{1}{2\pi(R_{ESR} + R_L)C_{OUT}} \text{ (in Hz)}$$

where

- R_L is the minimum load resistance corresponding to the maximum load current (19)

$$f_{Z1} = \frac{1}{2\pi R_{ESR} C_{OUT}} \text{ (in Hz)} \quad (20)$$

The zero created by the ESR of the output capacitor is generally very high frequency if the ESR is small. If low ESR capacitors are used it can be neglected. If higher ESR capacitors are used see the HIGH OUTPUT CAPACITOR ESR COMPENSATION section. Some suitable capacitor vendors include Vishay, Taiyo-Yuden, and TDK.

RIGHT HALF PLANE ZERO

A current mode control boost regulator has an inherent right half plane zero (RHP zero). This zero has the effect of a zero in the gain plot, causing an imposed +20dB/decade on the rolloff, but has the effect of a pole in the phase, subtracting another 90° in the phase plot. This can cause undesirable effects if the control loop is influenced by this zero. To ensure the RHP zero does not cause instability issues, the control loop should be designed to have a bandwidth of less than ½ the frequency of the RHP zero. This zero occurs at a frequency of:

$$\text{RHPzero} = \frac{V_{OUT}(D')^2}{2\pi I_{LOAD} L} \text{ (in Hz)}$$

where

- I_{LOAD} is the maximum load current (21)

SELECTING THE COMPENSATION COMPONENTS

The first step in selecting the compensation components R_C and C_C is to set a dominant low frequency pole in the control loop. Simply choose values for R_C and C_C within the ranges given in the Introduction to Compensation section to set this pole in the area of 10Hz to 500Hz. The frequency of the pole created is determined by the equation:

$$f_{PC} = \frac{1}{2\pi (R_C + R_O) C_C} \text{ (in Hz)}$$

where

- R_O is the output impedance of the error amplifier, approximately 900kΩ (22)

Since R_C is generally much less than R_O, it does not have much effect on the above equation and can be neglected until a value is chosen to set the zero f_{ZC}. f_{ZC} is created to cancel out the pole created by the output capacitor, f_{P1}. The output capacitor pole will shift with different load currents as shown by the equation, so setting the zero is not exact. Determine the range of f_{P1} over the expected loads and then set the zero f_{ZC} to a point approximately in the middle. The frequency of this zero is determined by:

$$f_{ZC} = \frac{1}{2\pi C_C R_C} \text{ (in Hz)} \quad (23)$$

Now R_C can be chosen with the selected value for C_C. Check to make sure that the pole f_{PC} is still in the 10Hz to 500Hz range, change each value slightly if needed to ensure both component values are in the recommended range.

HIGH OUTPUT CAPACITOR ESR COMPENSATION

When using an output capacitor with a high ESR value, or just to improve the overall phase margin of the control loop, another pole may be introduced to cancel the zero created by the ESR. This is accomplished by adding another capacitor, C_{C2}, directly from the compensation pin V_C to ground, in parallel with the series combination of R_C and C_C. The pole should be placed at the same frequency as f_{Z1}, the ESR zero. The equation for this pole follows:

$$f_{PC2} = \frac{1}{2\pi C_{C2} (R_C // R_O)} \text{ (in Hz)} \quad (24)$$

To ensure this equation is valid, and that C_{C2} can be used without negatively impacting the effects of R_C and C_C, f_{PC2} must be greater than $10 f_{ZC}$.

CHECKING THE DESIGN

With all the poles and zeros calculated the crossover frequency can be checked as described in the section DC GAIN AND OPEN-LOOP GAIN. The compensation values can be changed a little more to optimize performance if desired. This is best done in the lab on a bench, checking the load step response with different values until the ringing and overshoot on the output voltage at the edge of the load steps is minimal. This should produce a stable, high performance circuit. For improved transient response, higher values of R_C should be chosen. This will improve the overall bandwidth which makes the regulator respond more quickly to transients. If more detail is required, or the most optimum performance is desired, refer to a more in depth discussion of compensating current mode DC/DC switching regulators.

POWER DISSIPATION

The output power of the LM3310 is limited by its maximum power dissipation. The maximum power dissipation is determined by the formula

$$P_D = (T_{jmax} - T_A)/\theta_{JA} \quad (25)$$

where

- T_{jmax} is the maximum specified junction temperature (125°C)
- T_A is the ambient temperature
- θ_{JA} is the thermal resistance of the package

LAYOUT CONSIDERATIONS

The input bypass capacitor C_{IN}, as shown in the Typical Application Circuit, must be placed close to the IC. This will reduce copper trace resistance which effects input voltage ripple of the IC. For additional input voltage filtering, a 100nF bypass capacitor can be placed in parallel with C_{IN}, close to the V_{IN} pin, to shunt any high frequency noise to ground. The output capacitor, C_{OUT}, should also be placed close to the IC. Any copper trace connections for the C_{OUT} capacitor can increase the series resistance, which directly effects output voltage ripple. The feedback network, resistors R_{FB1} and R_{FB2}, should be kept close to the FB pin, and away from the inductor, to minimize copper trace connections that can inject noise into the system. R_E and C_E should also be close to the RE and CE pins to minimize noise in the GPM circuitry. Trace connections made to the inductor and schottky diode should be minimized to reduce power dissipation and increase overall efficiency. For more detail on switching power supply layout considerations see Application Note AN-1149: *Layout Guidelines for Switching Power Supplies*.

For Op-Amp layout please refer to the OPERATIONAL AMPLIFIER section.

Figure 49, Figure 50, and Figure 51 in the Application Information section following show the schematic and an example of a good layout as used in the LM3310/11 evaluation board.

APPLICATION INFORMATION

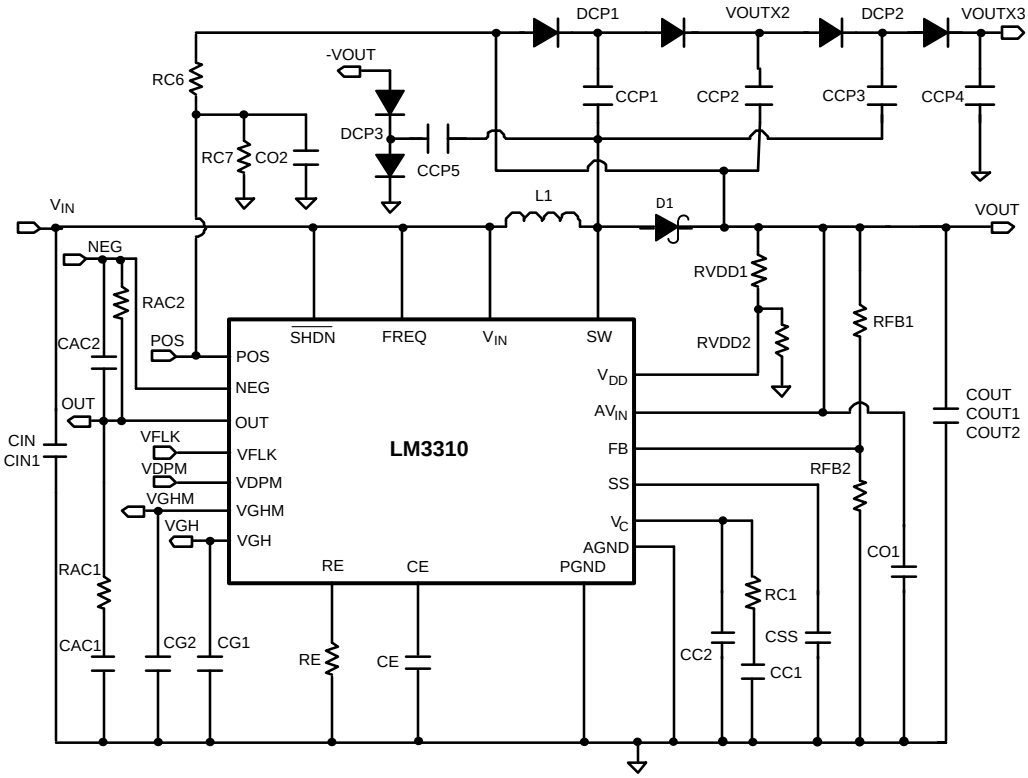


Figure 49. Evaluation Board Schematic

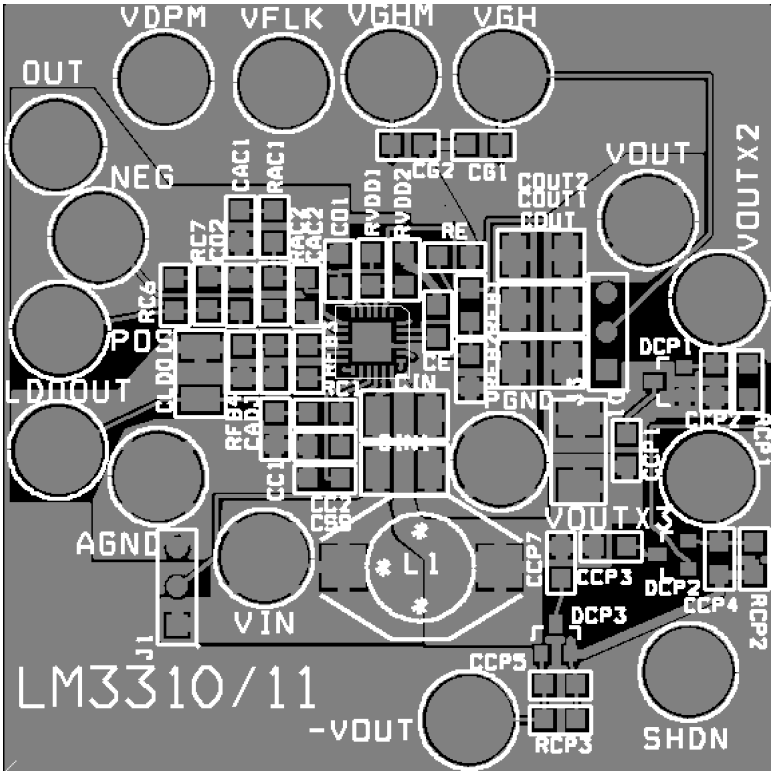


Figure 50. Evaluation Board Layout (top layer)

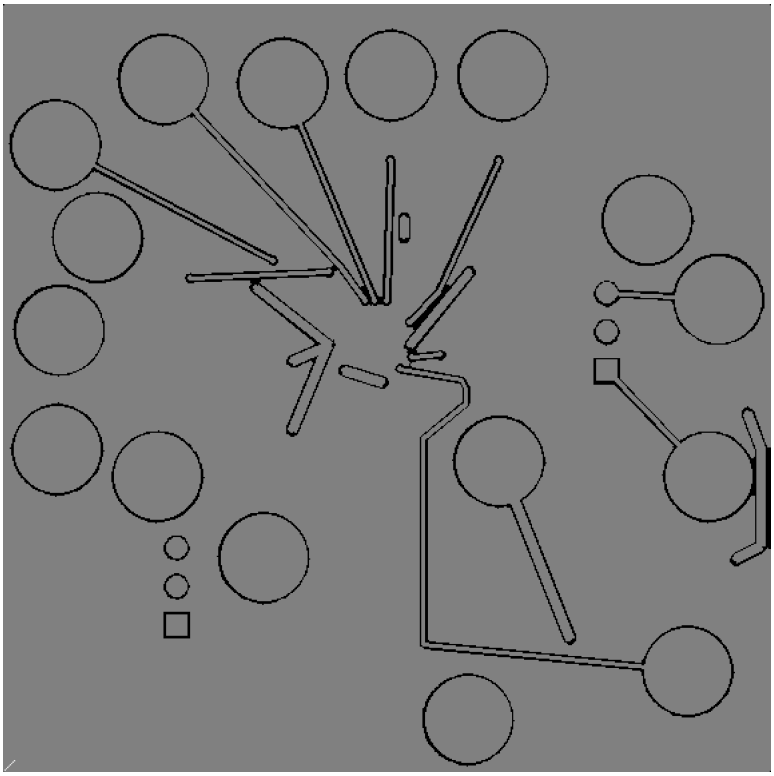


Figure 51. Evaluation Board Layout (bottom layer)

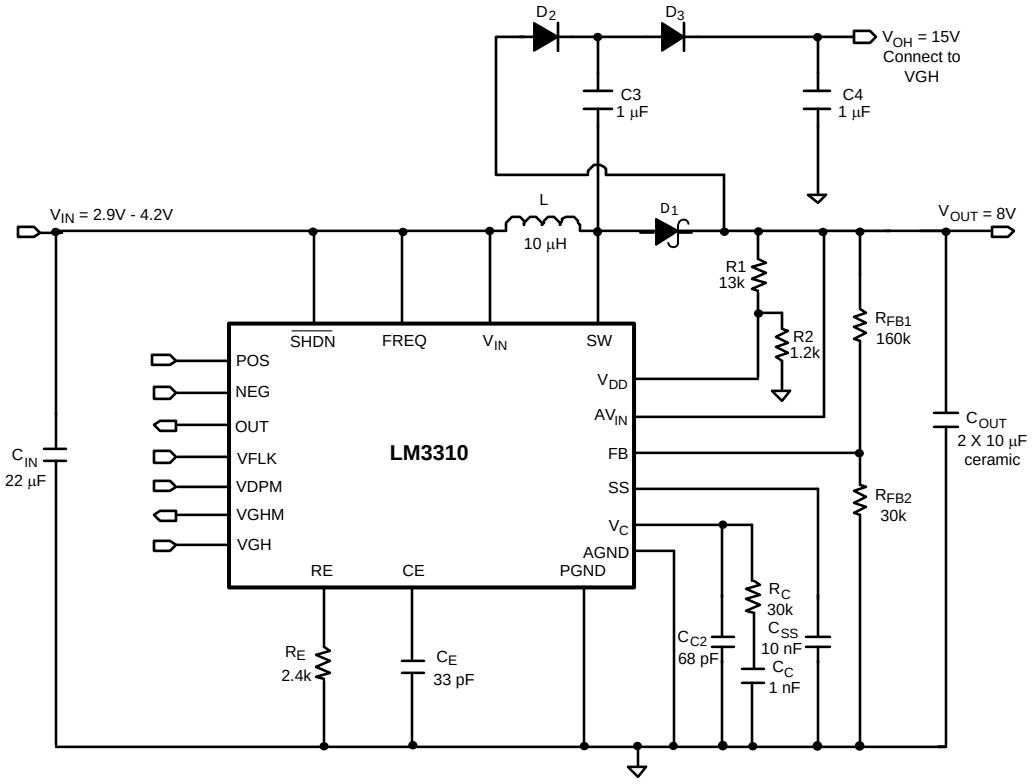


Figure 52. Li-Ion to 8V, 1.28MHz Application

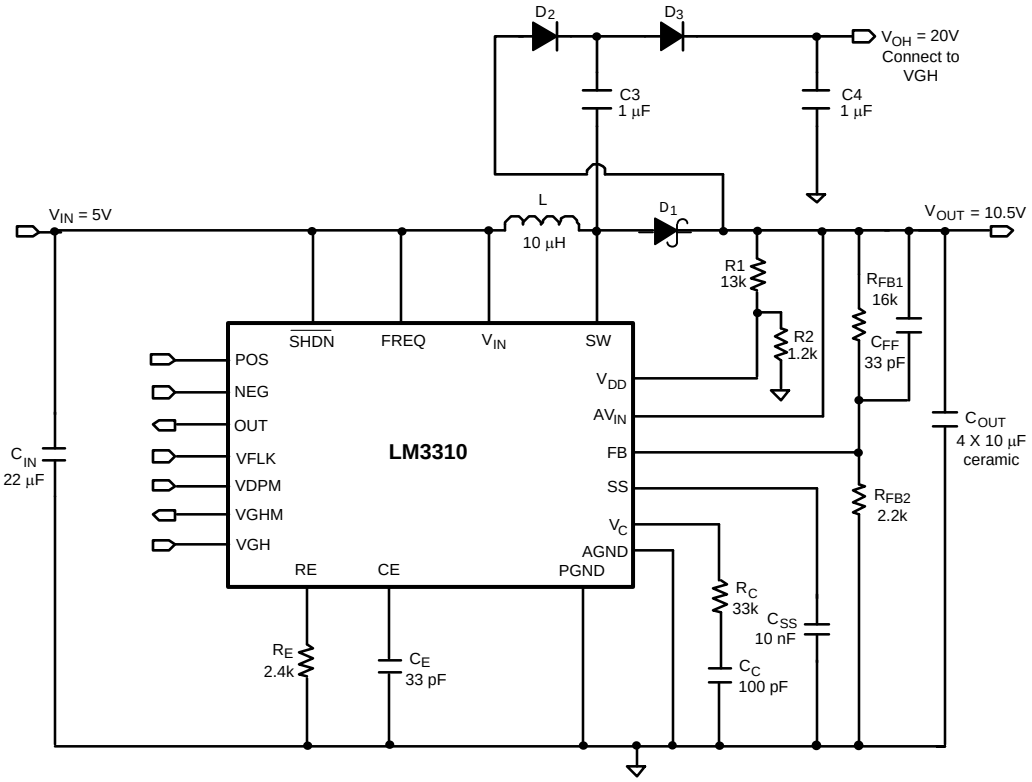


Figure 53. 5V to 10.5V, 1.28MHz Application

Table 1. Some Recommended Inductors (Others May Be Used)

Manufacturer	Inductor	Contact Information
Coilcraft	DO3316 and DT3316 series	www.coilcraft.com 800-3222645
TDK	SLF10145 series	www.component.tdk.com 847-803-6100
Pulse	P0751 and P0762 series	www.pulseeng.com
Sumida	CDRH8D28 and CDRH8D43 series	www.sumida.com

Table 2. Some Recommended Input And Output Capacitors (Others May Be Used)

Manufacturer	Capacitor	Contact Information
Vishay Sprague	293D, 592D, and 595D series tantalum	www.vishay.com 407-324-4140
Taiyo Yuden	High capacitance MLCC ceramic	www.t-yuden.com 408-573-4150
Cornell Dubilier	ESRD seriec Polymer Aluminum Electrolytic SPV and AFK series V-chip series	www.cde.com
Panasonic	High capacitance MLCC ceramic EEJ-L series tantalum	www.panasonic.com

REVISION HISTORY

Changes from Revision D (May 2013) to Revision E **Page**

- Changed layout of National Data Sheet to TI format 26

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
LM3310SQ/NOPB	ACTIVE	WQFN	RTW	24	1000	Green (RoHS & no Sb/Br)	CU SN	Level-1-260C-UNLIM	-40 to 125	L3310SQ	Samples

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

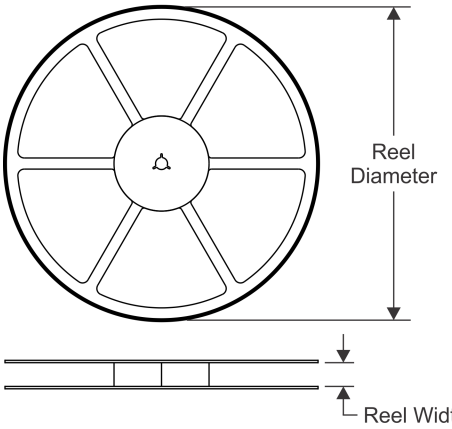
(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

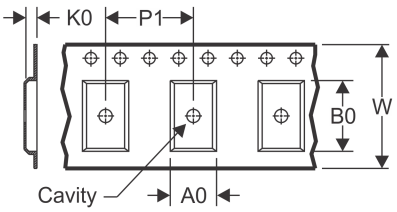
(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

TAPE AND REEL INFORMATION

REEL DIMENSIONS

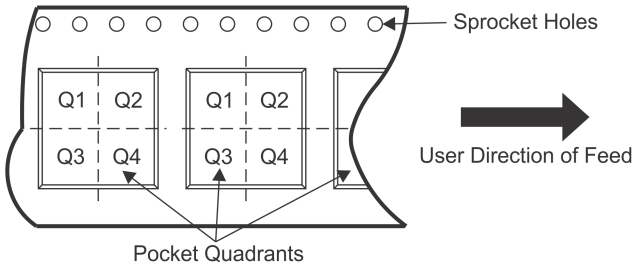


TAPE DIMENSIONS



A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

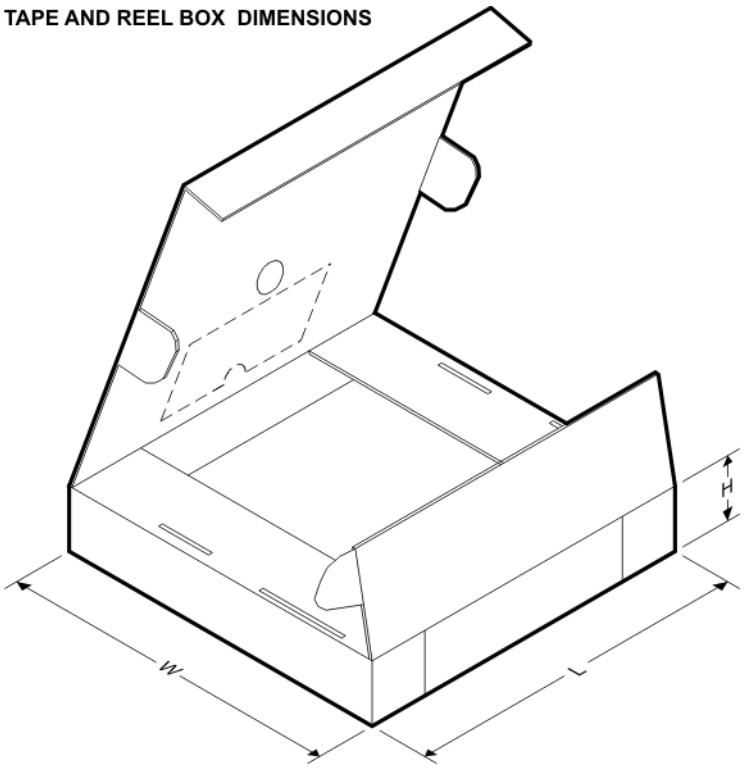
QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE



*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM3310SQ/NOPB	WQFN	RTW	24	1000	178.0	12.4	4.3	4.3	1.3	8.0	12.0	Q1

TAPE AND REEL BOX DIMENSIONS



*All dimensions are nominal

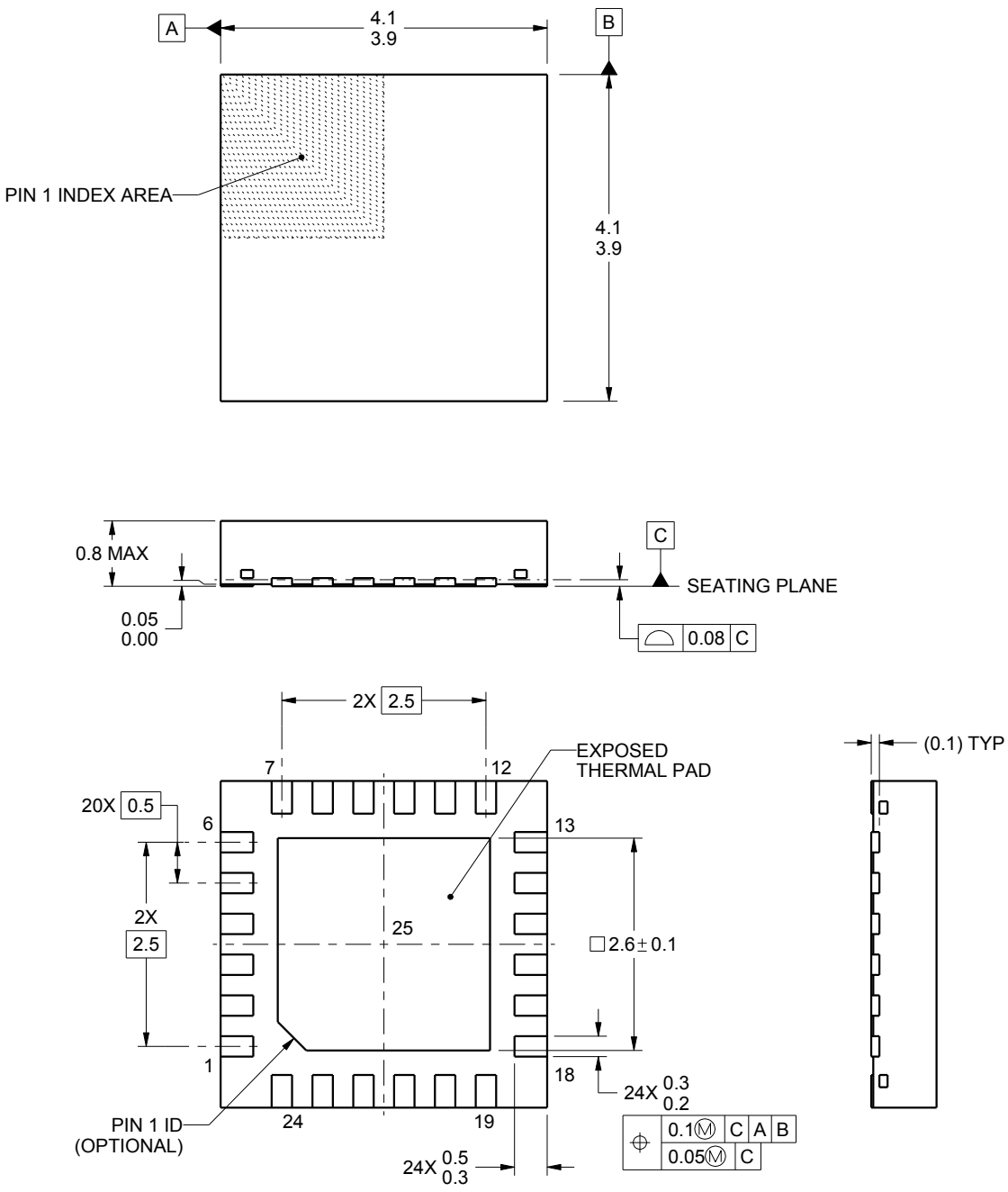
Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
LM3310SQ/NOPB	WQFN	RTW	24	1000	210.0	185.0	35.0

PACKAGE OUTLINE

RTW0024A

WQFN - 0.8 mm max height

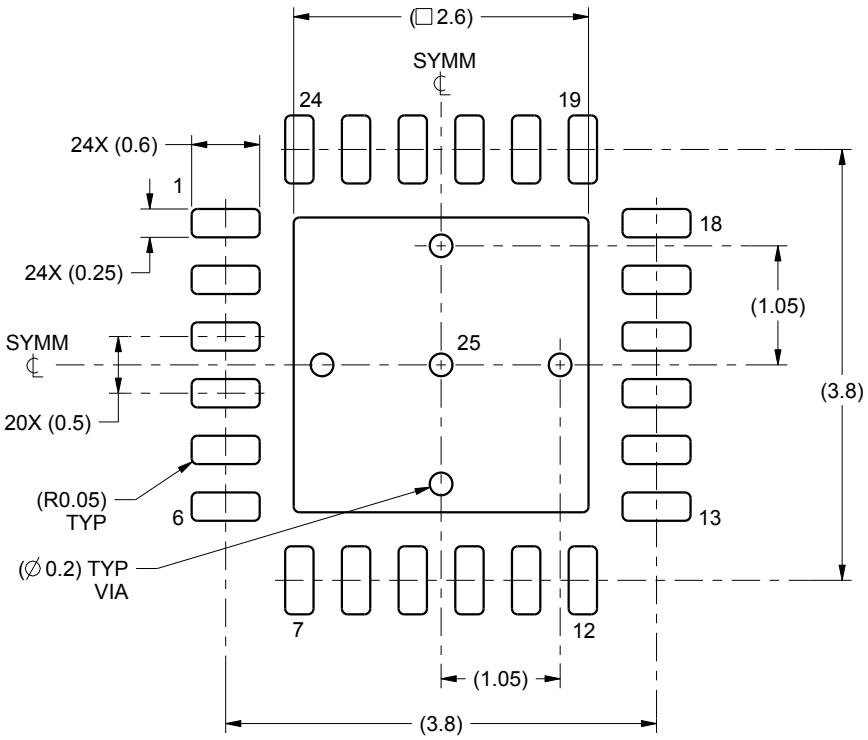
PLASTIC QUAD FLATPACK - NO LEAD



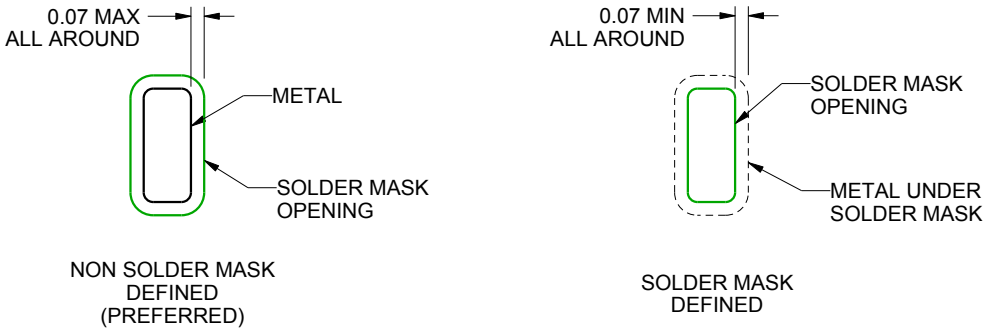
4222815/A 03/2016

NOTES:

1. All linear dimensions are in millimeters. Any dimensions in parenthesis are for reference only. Dimensioning and tolerancing per ASME Y14.5M.
2. This drawing is subject to change without notice.
3. The package thermal pad must be soldered to the printed circuit board for thermal and mechanical performance.



LAND PATTERN EXAMPLE
SCALE:15X

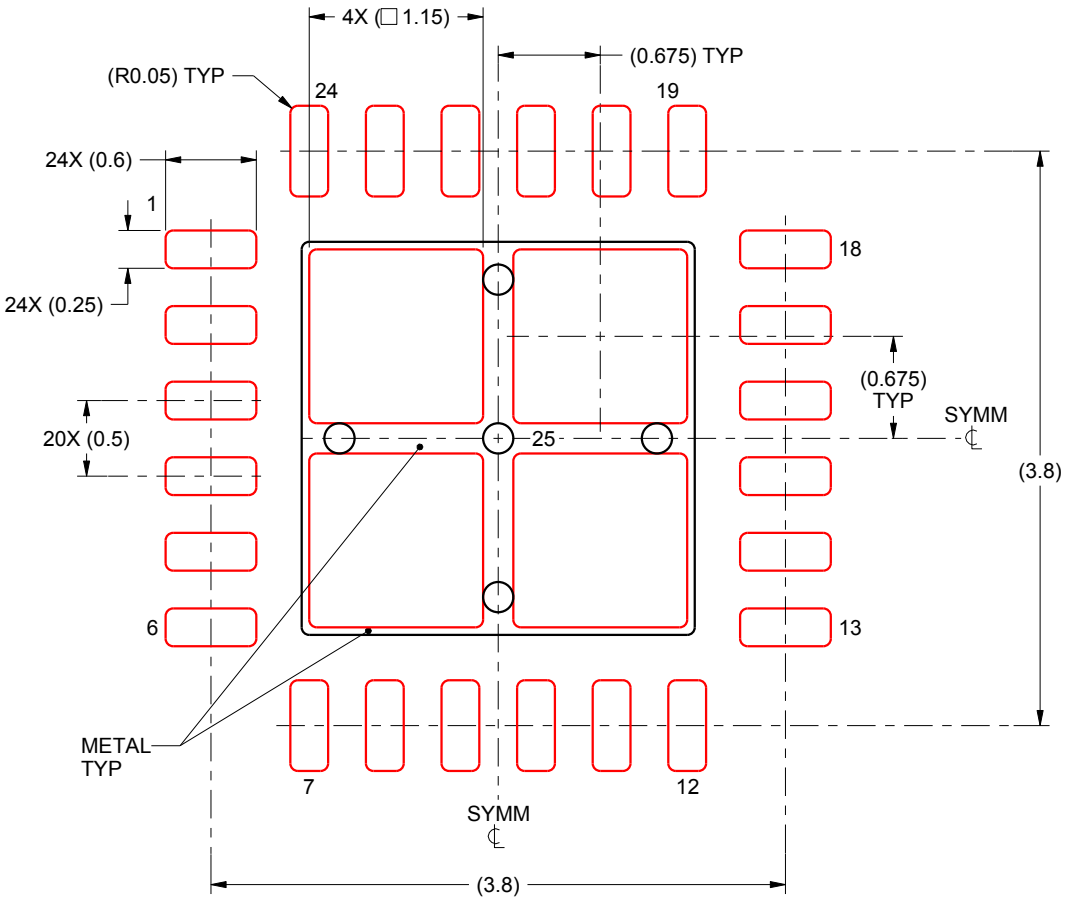


SOLDER MASK DETAILS

4222815/A 03/2016

NOTES: (continued)

4. This package is designed to be soldered to a thermal pad on the board. For more information, see Texas Instruments literature number SLUA271 (www.ti.com/lit/slua271).



SOLDER PASTE EXAMPLE
BASED ON 0.125 mm THICK STENCIL

EXPOSED PAD 25:
78% PRINTED SOLDER COVERAGE BY AREA UNDER PACKAGE
SCALE:20X

4222815/A 03/2016

NOTES: (continued)

5. Laser cutting apertures with trapezoidal walls and rounded corners may offer better paste release. IPC-7525 may have alternate design recommendations.

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