

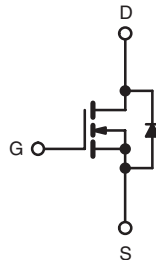
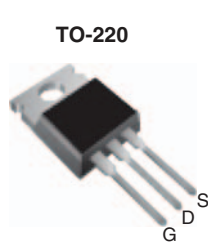


**THE DATASHEET OF  
IRFB17N60KPBF**



## Power MOSFET

PRODUCT SUMMARY		
$V_{DS}$ (V)	600	
$R_{DS(on)}$ ( $\Omega$ )	$V_{GS} = 10\text{ V}$	0.35
$Q_g$ (Max.) (nC)	99	
$Q_{gs}$ (nC)	32	
$Q_{gd}$ (nC)	47	
Configuration	Single	



N-Channel MOSFET

### FEATURES

- Smaller TO-220 Package
- Low Gate Charge  $Q_g$  Results in Simple Drive Requirement
- Improved Gate, Avalanche and Dynamic  $dV/dt$  Ruggedness
- Fully Characterized Capacitance and Avalanche Voltage and Current
- Lead (Pb)-free Available



### APPLICATIONS

- Switch Mode Power Supply (SMPS)
- Uninterruptible Power Supply
- High Speed Power Switching
- Hard Switched and High Frequency Circuits

ORDERING INFORMATION	
Package	TO-220
Lead (Pb)-free	IRFB17N60KPbF
	SiHFB17N60K-E3
SnPb	IRFB17N60K
	SiHFB17N60K


ABSOLUTE MAXIMUM RATINGS $T_C = 25\text{ }^\circ\text{C}$ , unless otherwise noted				
PARAMETER	SYMBOL	LIMIT	UNIT	
Drain-Source Voltage	$V_{DS}$	600	V	
Gate-Source Voltage	$V_{GS}$	$\pm 30$		
Continuous Drain Current	$V_{GS}$ at 10 V	$T_C = 25\text{ }^\circ\text{C}$	17	A
		$T_C = 100\text{ }^\circ\text{C}$	11	
Pulsed Drain Current <sup>a</sup>	$I_{DM}$	68		
Linear Derating Factor		2.7	W/ $^\circ\text{C}$	
Single Pulse Avalanche Energy <sup>b</sup>	$E_{AS}$	330	mJ	
Repetitive Avalanche Current <sup>a</sup>	$I_{AR}$	17	A	
Repetitive Avalanche Energy <sup>a</sup>	$E_{AR}$	34	mJ	
Maximum Power Dissipation	$T_C = 25\text{ }^\circ\text{C}$	$P_D$	340	W
Peak Diode Recovery $dV/dt^c$	$dV/dt$	11	V/ns	
Operating Junction and Storage Temperature Range	$T_J, T_{stg}$	- 55 to + 150	$^\circ\text{C}$	
Soldering Recommendations (Peak Temperature)	for 10 s	300 <sup>d</sup>		
Mounting Torque	6-32 or M3 screw	10	N	

#### Notes

- Repetitive rating; pulse width limited by maximum junction temperature (see fig. 11).
- Starting  $T_J = 25\text{ }^\circ\text{C}$ ,  $L = 2.3\text{ mH}$ ,  $R_G = 25\text{ }\Omega$ ,  $I_{AS} = 17\text{ A}$  (see fig. 12).
- $I_{SD} \leq 17\text{ A}$ ,  $dI/dt \leq 380\text{ A}/\mu\text{s}$ ,  $V_{DD} \leq V_{DS}$ ,  $T_J \leq 150\text{ }^\circ\text{C}$ .
- 1.6 mm from case.

\* Pb containing terminations are not RoHS compliant, exemptions may apply

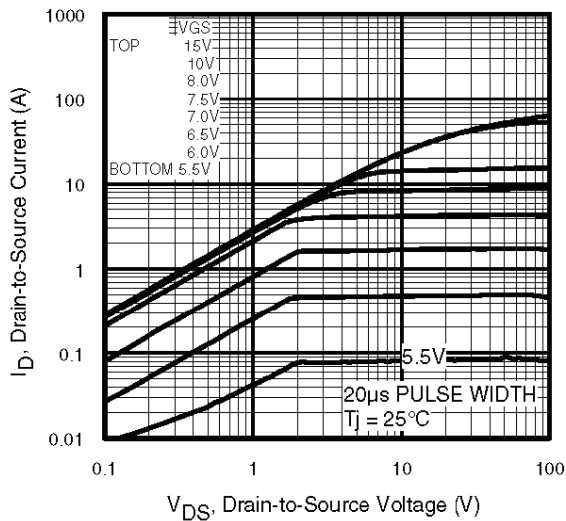
THERMAL RESISTANCE RATINGS				
PARAMETER	SYMBOL	TYP.	MAX.	UNIT
Maximum Junction-to-Ambient	$R_{thJA}$	-	58	°C/W
Case-to-Sink, Flat, Greased Surface	$R_{thCS}$	0.50	-	
Maximum Junction-to-Case (Drain)	$R_{thJC}$	-	0.37	

SPECIFICATIONS $T_J = 25\text{ }^\circ\text{C}$ , unless otherwise noted							
PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
<b>Static</b>							
Drain-Source Breakdown Voltage	$V_{DS}$	$V_{GS} = 0\text{ V}, I_D = 250\text{ }\mu\text{A}$		600	-	-	V
$V_{DS}$ Temperature Coefficient	$\Delta V_{DS}/T_J$	Reference to $25\text{ }^\circ\text{C}$ , $I_D = 1\text{ mA}$		-	600	-	mV/°C
Gate-Source Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$		3.0	-	5.0	V
Gate-Source Leakage	$I_{GSS}$	$V_{GS} = \pm 30\text{ V}$		-	-	$\pm 100$	nA
Zero Gate Voltage Drain Current	$I_{DSS}$	$V_{DS} = 600\text{ V}, V_{GS} = 0\text{ V}$		-	-	50	$\mu\text{A}$
		$V_{DS} = 480\text{ V}, V_{GS} = 0\text{ V}, T_J = 125\text{ }^\circ\text{C}$		-	-	250	
Drain-Source On-State Resistance	$R_{DS(on)}$	$V_{GS} = 10\text{ V}$	$I_D = 10\text{ A}^b$	-	0.35	0.42	$\Omega$
Forward Transconductance	$g_{fs}$	$V_{DS} = 50\text{ V}, I_D = 10\text{ A}$		5.9	-	-	S
<b>Dynamic</b>							
Input Capacitance	$C_{iss}$	$V_{GS} = 0\text{ V},$		-	2700	-	pF
Output Capacitance	$C_{oss}$	$V_{DS} = 25\text{ V},$		-	240	-	
Reverse Transfer Capacitance	$C_{riss}$	$f = 1.0\text{ MHz}$ , see fig. 5		-	21	-	
Output Capacitance	$C_{oss}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 1.0\text{ V}, f = 1.0\text{ MHz}$	-	2950	-	
Effective Output Capacitance	$C_{oss\text{ eff.}}$	$V_{GS} = 0\text{ V}$	$V_{DS} = 0\text{ V to } 480\text{ V}$	-	120	-	
Total Gate Charge	$Q_g$	$V_{GS} = 10\text{ V}$	$I_D = 17\text{ A}, V_{DS} = 480\text{ V}$ see fig. 6 and 13	-	-	99	nC
Gate-Source Charge	$Q_{gs}$			-	-	32	
Gate-Drain Charge	$Q_{gd}$			-	-	47	
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = 300\text{ V}, I_D = 17\text{ A},$ $R_G = 7.5\text{ }\Omega, V_{GS} = 10\text{ V}$ , see fig. 10 <sup>b</sup>		-	25	-	ns
Rise Time	$t_r$			-	82	-	
Turn-Off Delay Time	$t_{d(off)}$			-	38	-	
Fall Time	$t_f$			-	32	-	
<b>Drain-Source Body Diode Characteristics</b>							
Continuous Source-Drain Diode Current	$I_S$	MOSFET symbol showing the integral reverse p - n junction diode 		-	-	17	A
Pulsed Diode Forward Current <sup>a</sup>	$I_{SM}$			-	-	68	
Body Diode Voltage	$V_{SD}$	$T_J = 25\text{ }^\circ\text{C}, I_S = 17\text{ A}, V_{GS} = 0\text{ V}^b$		-	-	1.5	V
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 25\text{ }^\circ\text{C}, I_F = 17\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	520	780	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	5620	8430	nC
Body Diode Reverse Recovery Time	$t_{rr}$	$T_J = 125\text{ }^\circ\text{C}, I_F = 17\text{ A}, dI/dt = 100\text{ A}/\mu\text{s}^b$		-	580	870	ns
Body Diode Reverse Recovery Charge	$Q_{rr}$			-	6470	9700	nC
Forward Turn-On Time	$t_{on}$	Intrinsic turn-on time is negligible (turn-on is dominated by $L_S$ and $L_D$ )					

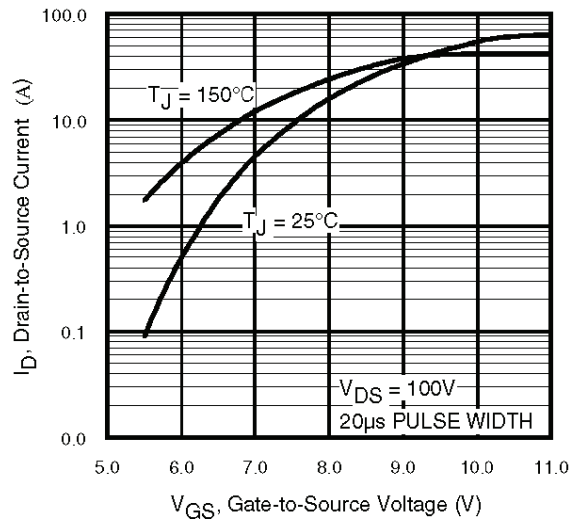
**Notes**

- a. Repetitive rating, pulse width limited by max. junction temperature.
- b. Pulse width  $\leq 300\text{ }\mu\text{s}$ ; duty cycle  $\leq 2\%$ .

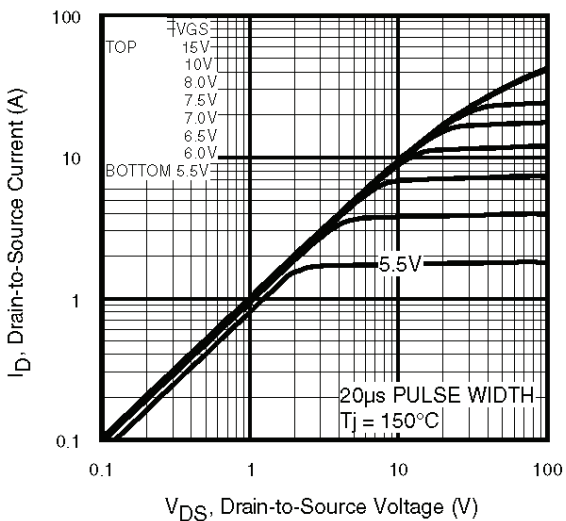
**TYPICAL CHARACTERISTICS** 25 °C, unless otherwise noted



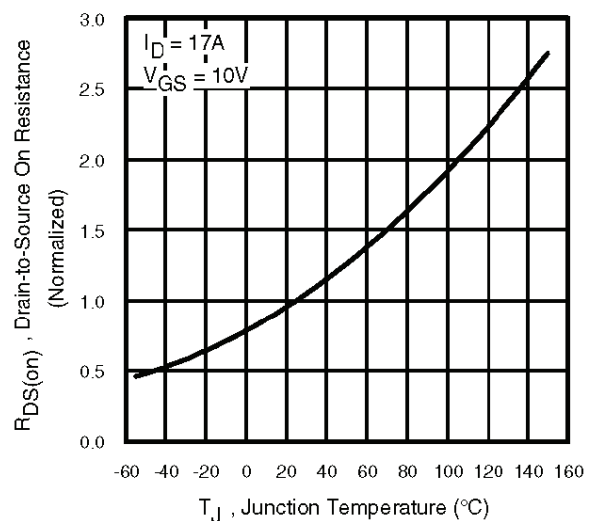
**Fig. 1 - Typical Output Characteristics**



**Fig. 3 - Typical Transfer Characteristics**



**Fig. 2 - Typical Output Characteristics**



**Fig. 4 - Normalized On-Resistance vs. Temperature**

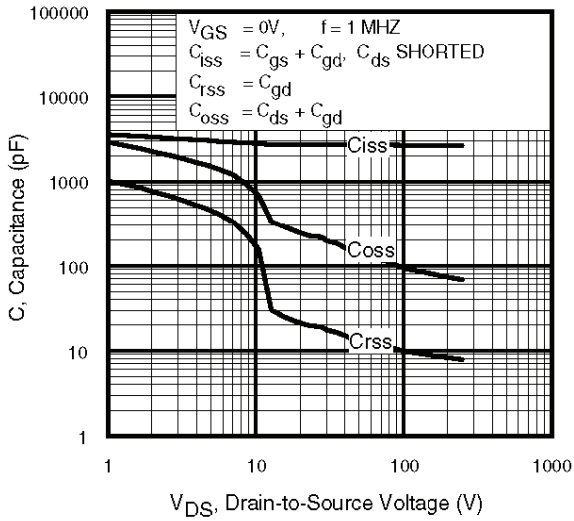


Fig. 5 - Typical Capacitance vs. Drain-to-Source Voltage

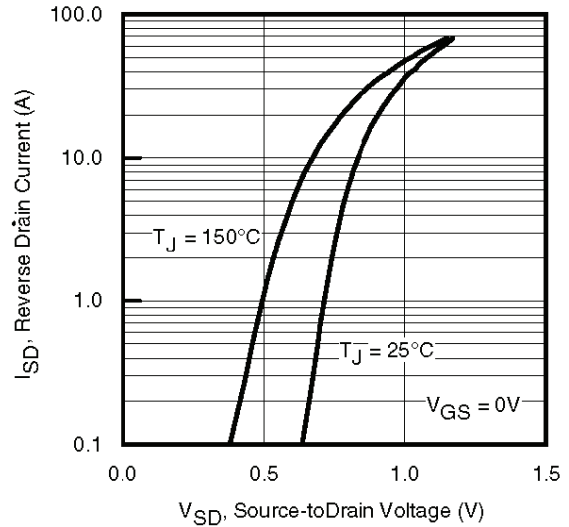


Fig. 7 - Typical Source-Drain Diode Forward Voltage

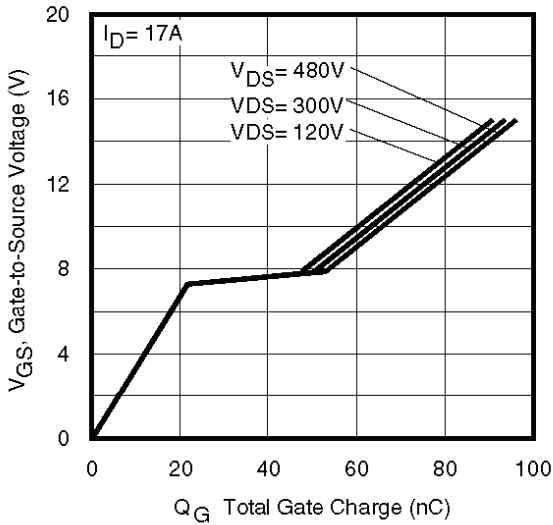


Fig. 6 - Typical Gate Charge vs. Gate-to-Source Voltage

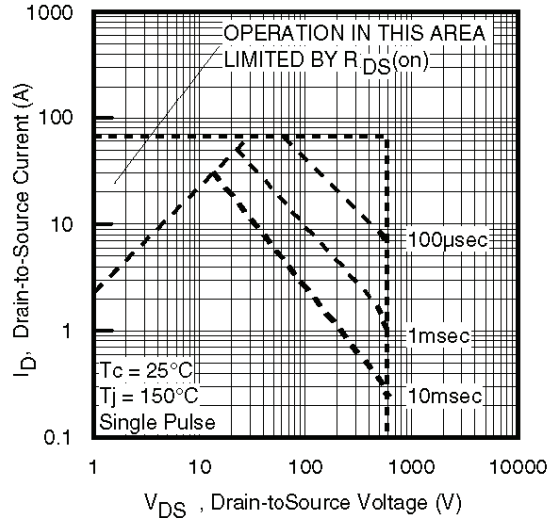


Fig. 8 - Maximum Safe Operating Area

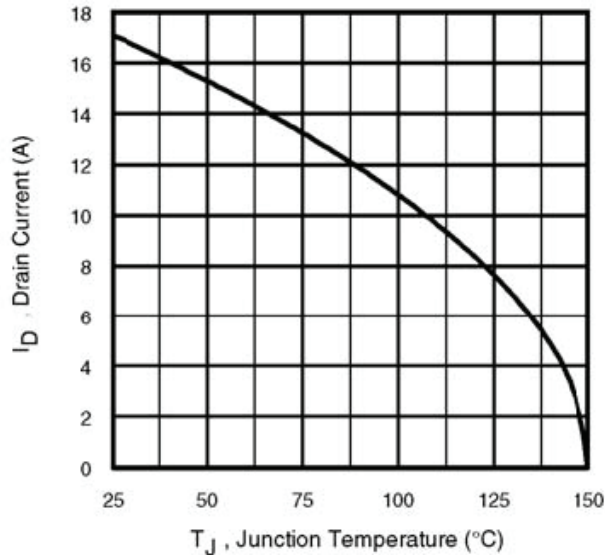


Fig. 9 - Maximum Drain Current vs. Case Temperature

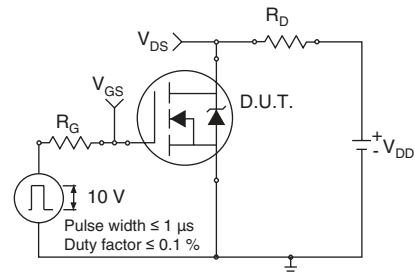


Fig. 10a - Switching Time Test Circuit

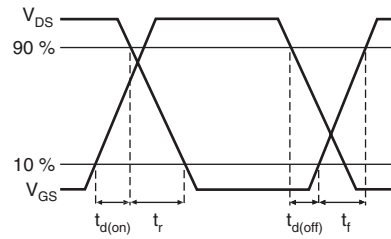


Fig. 10b - Switching Time Waveforms

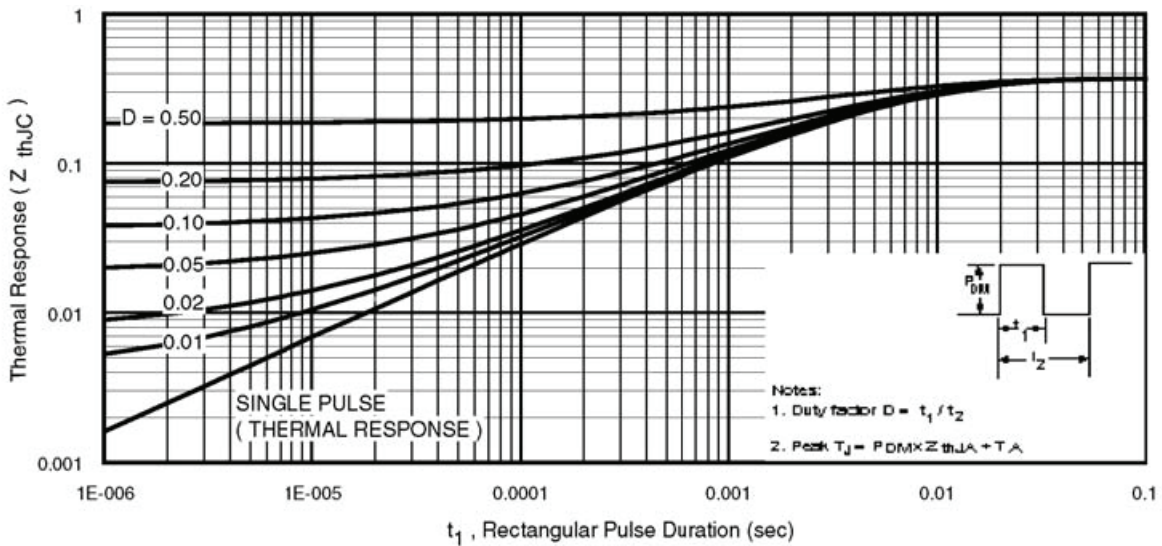


Fig. 11 - Maximum Effective Transient Thermal Impedance, Junction-to-Case

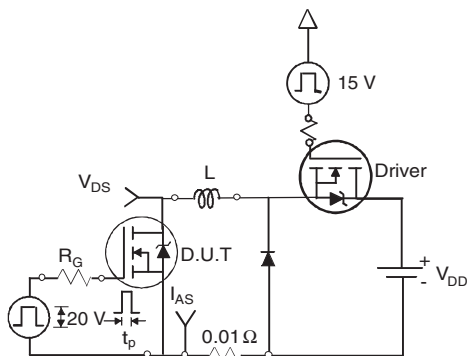


Fig. 12a - Unclamped Inductive Test Circuit

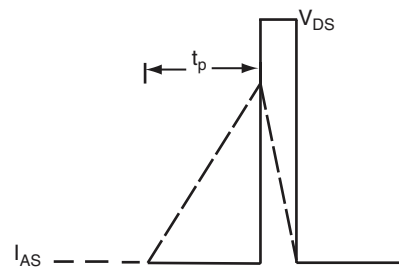


Fig. 12b - Unclamped Inductive Waveforms

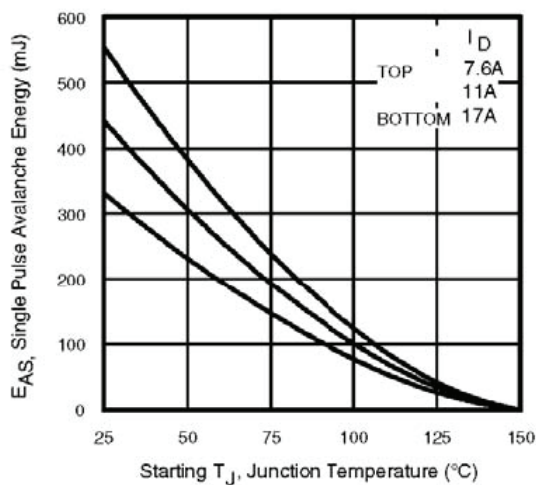


Fig. 12c - Maximum Avalanche Energy vs. Drain Current

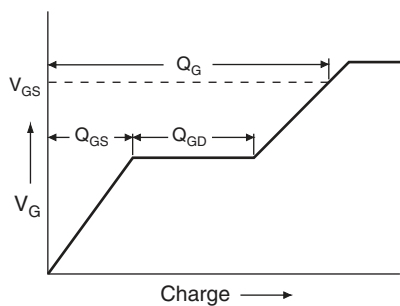


Fig. 13a - Basic Gate Charge Waveform

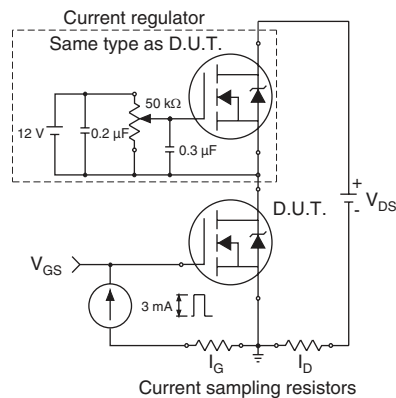
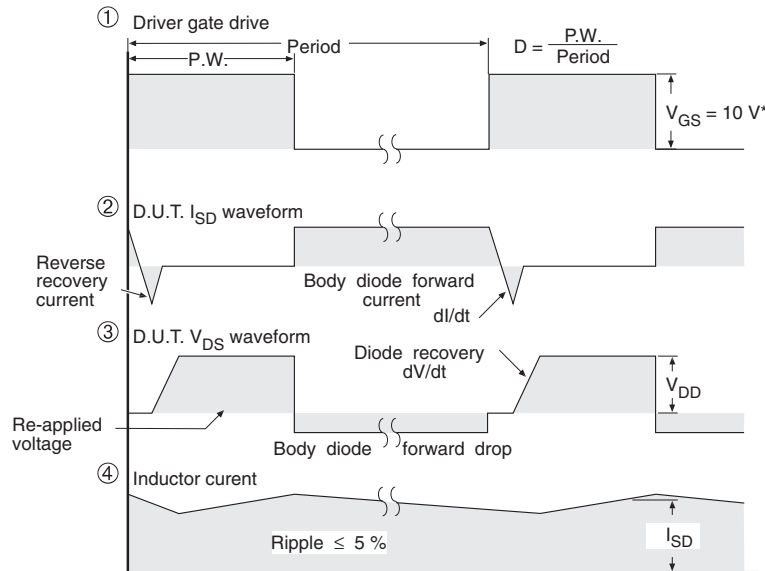
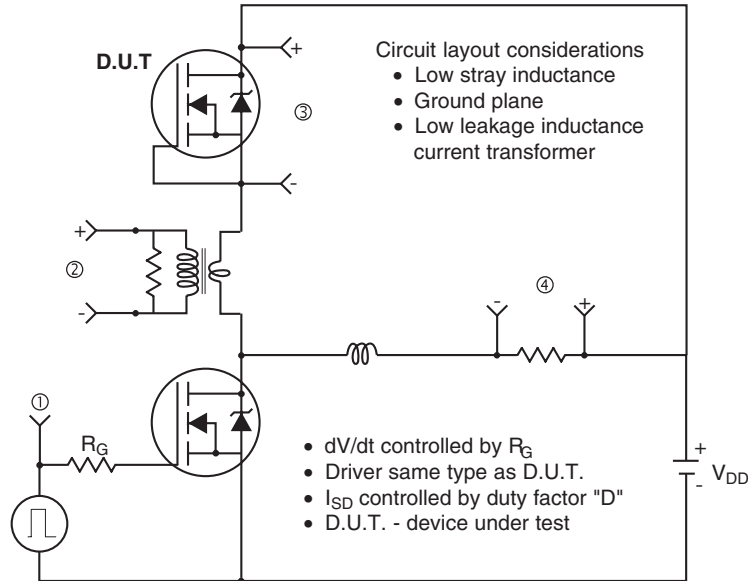


Fig. 13b - Gate Charge Test Circuit

## Peak Diode Recovery dV/dt Test Circuit



\*  $V_{GS} = 5 V$  for logic level devices

Fig. 14 - For N-Channel

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