



# THE DATASHEET OF STD9NM50N





# STD9NM50N

N-channel 500 V, 0.73  $\Omega$ , 5 A MDmesh™II Power MOSFET  
in DPAK

## Features

Order code	V <sub>DSS</sub> @T <sub>JMAX</sub>	R <sub>DS(on)</sub> max.	I <sub>D</sub>
STD9NM50N	550 V	< 0.79 $\Omega$	5 A

- 100% avalanche tested
- Low input capacitances and gate charge
- Low gate input resistance

## Applications

- Switching applications
- Automotive

## Description

These N-channel Power MOSFETs are developed using STMicroelectronics' revolutionary MDmesh™ technology, which associates the multiple drain process with the company's PowerMESH™ horizontal layout. These devices offer extremely low on-resistance, high dv/dt and excellent avalanche characteristics. Utilizing ST's proprietary strip technique, these Power MOSFETs boast an overall dynamic performance which is superior to similar products on the market.

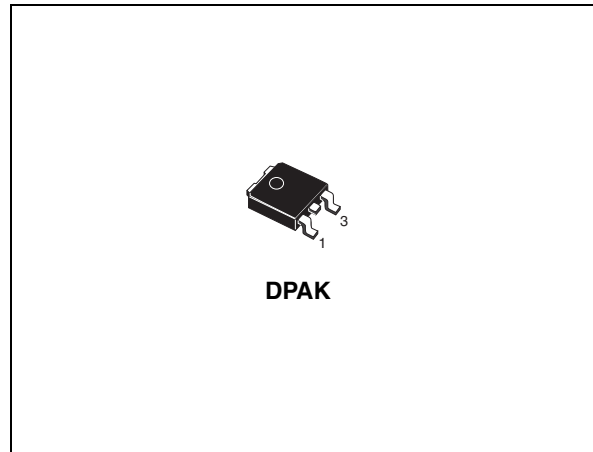


Figure 1. Internal schematic diagram

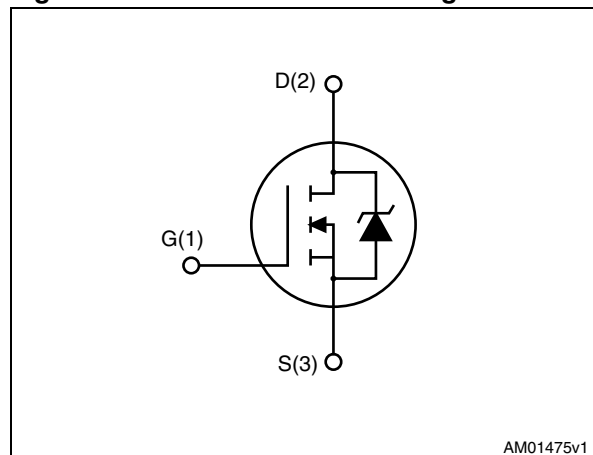


Table 1. Device summary

Order code	Marking	Packages	Packaging
STD9NM50N	9NM50N	DPAK	Tape and reel

# Contents

<b>1</b>	<b>Electrical ratings</b> .....	<b>3</b>
<b>2</b>	<b>Electrical characteristics</b> .....	<b>4</b>
	2.1 Electrical characteristics (curves) .....	6
<b>3</b>	<b>Test circuits</b> .....	<b>8</b>
<b>4</b>	<b>Package mechanical data</b> .....	<b>9</b>
<b>5</b>	<b>Packaging mechanical data</b> .....	<b>12</b>
<b>6</b>	<b>Revision history</b> .....	<b>14</b>

# 1 Electrical ratings

**Table 2. Absolute maximum ratings**

Symbol	Parameter	Value	Unit
$V_{GS}$	Gate-source voltage	$\pm 25$	V
$I_D$	Drain current (continuous) at $T_C = 25\text{ }^\circ\text{C}$	5	A
$I_D$	Drain current (continuous) at $T_C = 100\text{ }^\circ\text{C}$	3	A
$I_{DM}^{(1)}$	Drain current (pulsed)	20	A
$P_{TOT}$	Total dissipation at $T_C = 25\text{ }^\circ\text{C}$	45	W
$dv/dt^{(2)}$	Peak diode recovery voltage slope	15	V/ns
$T_{stg}$	Storage temperature	- 55 to 150	$^\circ\text{C}$
$T_j$	Max. operating junction temperature	150	$^\circ\text{C}$

1. Pulse width limited by safe operating area

2.  $I_{SD} \leq 5\text{ A}$ ,  $di/dt \leq 400\text{ A}/\mu\text{s}$ ,  $V_{Peak} < V_{(BR)DSS}$ ,  $V_{DS}=80\% V_{(BR)DSS}$

**Table 3. Thermal data**

Symbol	Parameter	Value	Unit
$R_{thj-case}$	Thermal resistance junction-case max	2.78	$^\circ\text{C}/\text{W}$
$R_{thj-pcb}$	Thermal resistance junction-pcb max	50	$^\circ\text{C}/\text{W}$

**Table 4. Avalanche characteristics**

Symbol	Parameter	Value	Unit
$I_{AR}$	Avalanche current, repetitive or not-repetitive (pulse width limited by $T_j$ max)	2	A
$E_{AS}$	Single pulse avalanche energy (starting $T_j = 25\text{ }^\circ\text{C}$ , $I_D = I_{AR}$ , $V_{DD} = 50\text{ V}$ )	140	mJ

## 2 Electrical characteristics

( $T_C = 25\text{ °C}$  unless otherwise specified)

**Table 5. On /off states**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$V_{(BR)DSS}$	Drain-source breakdown voltage ( $V_{GS} = 0$ )	$I_D = 1\text{ mA}$	500			V
$I_{DSS}$	Zero gate voltage drain current ( $V_{GS} = 0$ )	$V_{DS} = 500\text{ V}$ $V_{DS} = 500\text{ V}, T_C = 125\text{ °C}$			1 100	$\mu\text{A}$ $\mu\text{A}$
$I_{GSS}$	Gate-body leakage current ( $V_{DS} = 0$ )	$V_{GS} = \pm 25\text{ V}$			100	nA
$V_{GS(th)}$	Gate threshold voltage	$V_{DS} = V_{GS}, I_D = 250\text{ }\mu\text{A}$	2	3	4	V
$R_{DS(on)}$	Static drain-source on resistance	$V_{GS} = 10\text{ V}, I_D = 2.5\text{ A}$		0.73	0.79	$\Omega$

**Table 6. Dynamic**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$C_{iss}$	Input capacitance	$V_{DS} = 50\text{ V}, f = 1\text{ MHz},$ $V_{GS} = 0$	-	364	-	pF
$C_{oss}$	Output capacitance			33		
$C_{rss}$	Reverse transfer capacitance			1.2		
$C_{oss(eq)}^{(1)}$	Equivalent output capacitance time related	$V_{DS} = 0\text{ to }50\text{ V}, V_{GS} = 0$	-	147.5	-	pF
$R_G$	Intrinsic gate resistance	$f = 1\text{ MHz open drain}$	-	5.4	-	$\Omega$
$Q_g$	Total gate charge	$V_{DD} = 400\text{ V}, I_D = 5\text{ A},$ $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 13</a> )	-	14	-	nC
$Q_{gs}$	Gate-source charge			3		nC
$Q_{gd}$	Gate-drain charge			7		nC

1.  $C_{oss\ eq}$  is defined as a constant equivalent capacitance giving the same charging time as  $C_{oss}$  when  $V_{DS}$  increases from 0 to 80%  $V_{DSS}$

**Table 7. Switching times**

Symbol	Parameter	Test conditions	Min.	Typ.	Max	Unit	
$t_{d(on)}$	Turn-on delay time	$V_{DD} = 250\text{ V}$ , $I_D = 5\text{ A}$ , $R_G = 4.7\ \Omega$ , $V_{GS} = 10\text{ V}$ (see <a href="#">Figure 12</a> )		7		ns	
$t_r$	Rise time			4.4		ns	
$t_{d(off)}$	Turn-off-delay time				25		ns
$t_f$	Fall time				8.8		ns

**Table 8. Source drain diode**

Symbol	Parameter	Test conditions	Min.	Typ.	Max.	Unit
$I_{SD}$	Source-drain current				5	A
$I_{SDM}^{(1)}$	Source-drain current (pulsed)				20	A
$V_{SD}^{(2)}$	Forward on voltage	$I_{SD} = 5\text{ A}$ , $V_{GS} = 0$			1.5	V
$t_{rr}$	Reverse recovery time	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ (see <a href="#">Figure 17</a> )		187		ns
$Q_{rr}$	Reverse recovery charge				1.3	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current				14	A
$t_{rr}$	Reverse recovery time	$I_{SD} = 5\text{ A}$ , $di/dt = 100\text{ A}/\mu\text{s}$ $V_{DD} = 60\text{ V}$ , $T_J = 150\text{ }^\circ\text{C}$ (see <a href="#">Figure 17</a> )		224		ns
$Q_{rr}$	Reverse recovery charge				1.5	$\mu\text{C}$
$I_{RRM}$	Reverse recovery current				13	A

1. Pulse width limited by safe operating area.
2. Pulsed: pulse duration = 300  $\mu\text{s}$ , duty cycle 1.5%

## 2.1 Electrical characteristics (curves)

Figure 2. Safe operating area

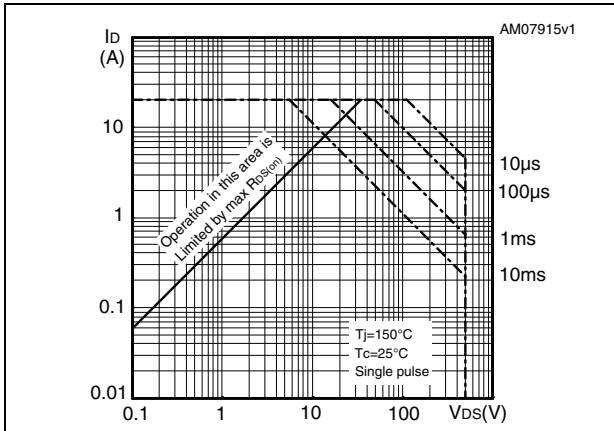


Figure 3. Thermal impedance

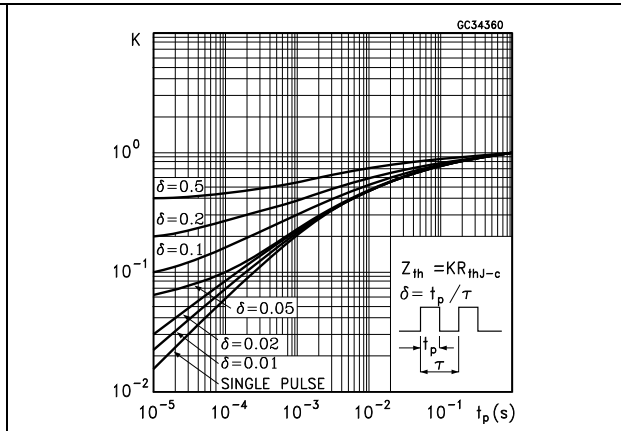


Figure 4. Output characteristics

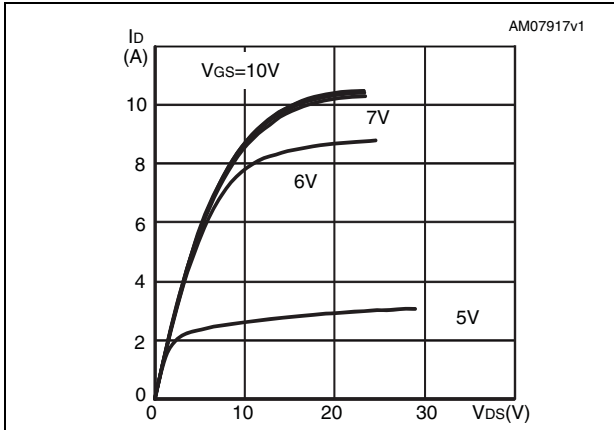


Figure 5. Transfer characteristics

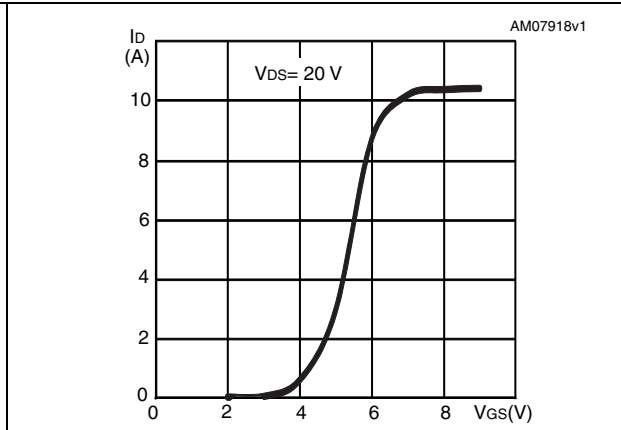


Figure 6. Static drain-source on resistance

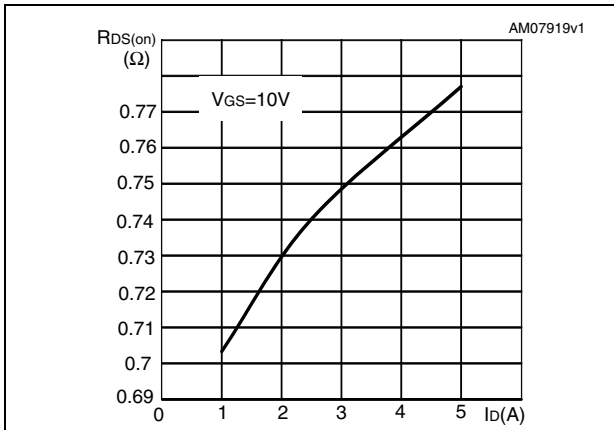


Figure 7. Gate charge vs gate-source voltage

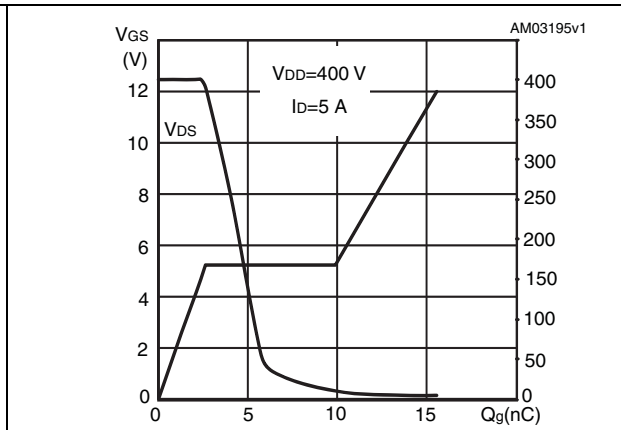


Figure 8. Capacitance variations

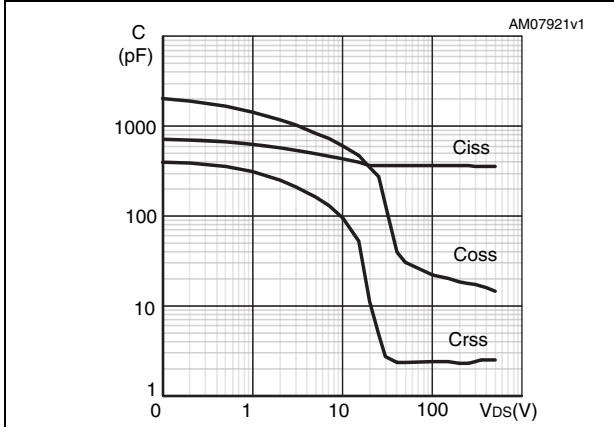


Figure 9. Normalized BV<sub>dss</sub> vs temperature

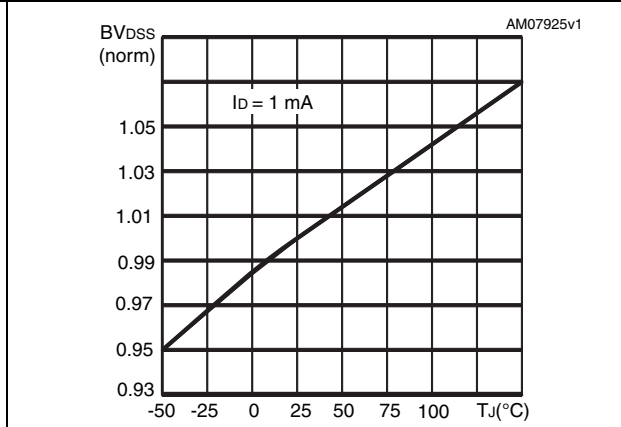


Figure 10. Normalized gate threshold voltage vs temperature

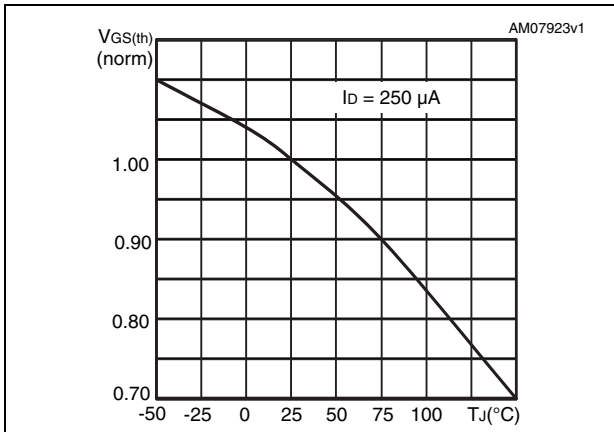
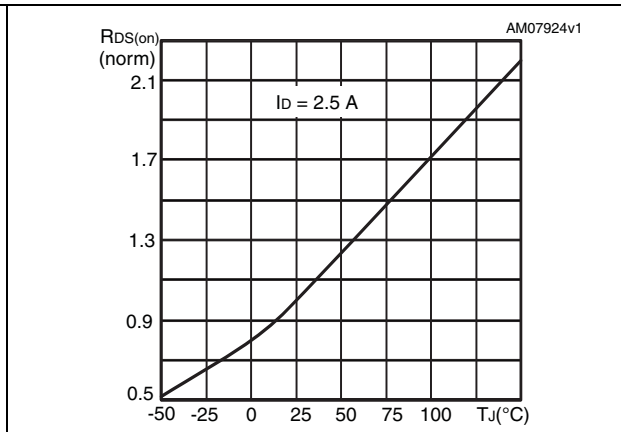
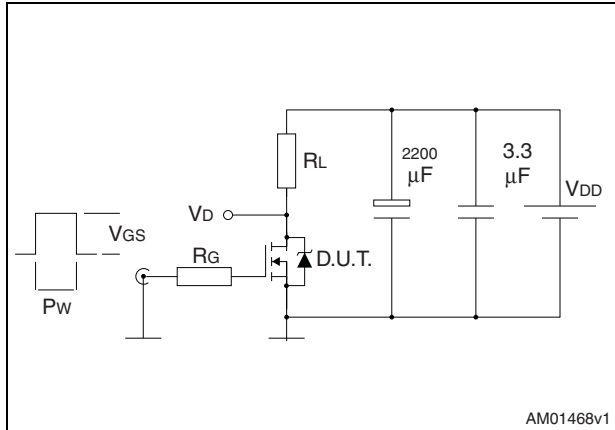


Figure 11. Normalized on resistance vs temperature



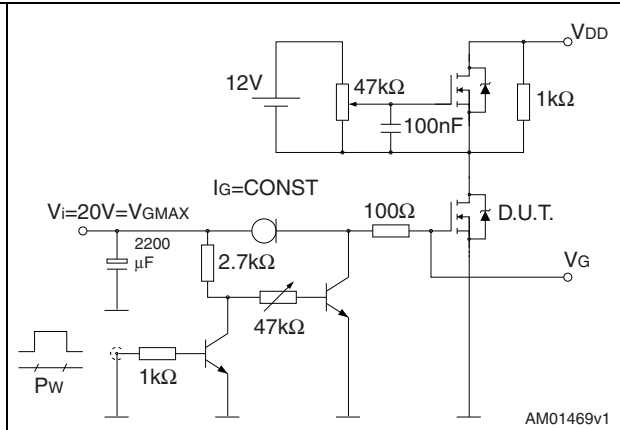
### 3 Test circuits

**Figure 12. Switching times test circuit for resistive load**



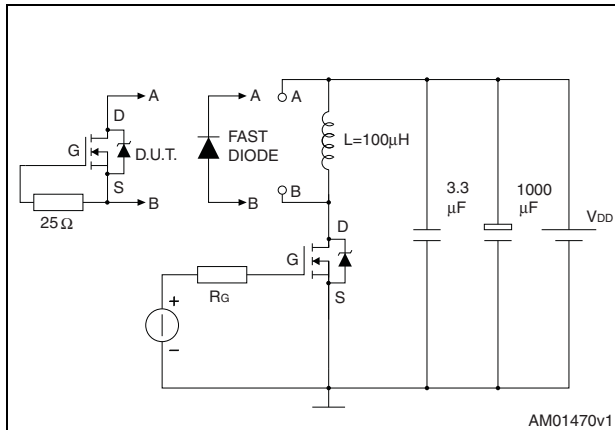
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**Figure 13. Gate charge test circuit**



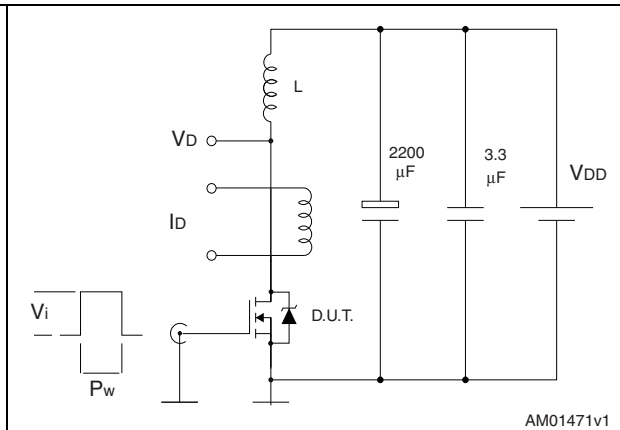
AM01469v1

**Figure 14. Test circuit for inductive load switching and diode recovery times**



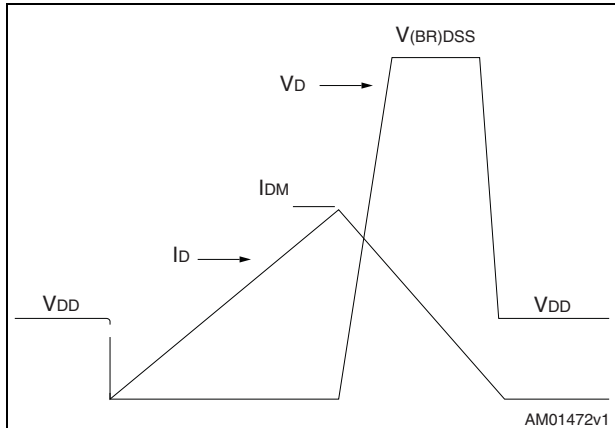
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**Figure 15. Unclamped inductive load test circuit**



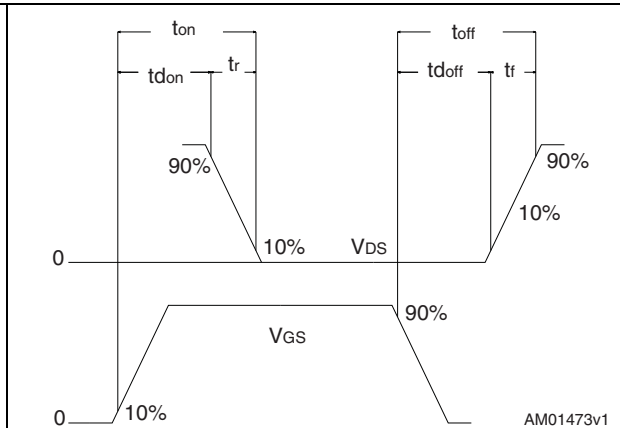
AM01471v1

**Figure 16. Unclamped inductive waveform**



AM01472v1

**Figure 17. Switching time waveform**



AM01473v1

## 4 Package mechanical data

In order to meet environmental requirements, ST offers these devices in different grades of ECOPACK<sup>®</sup> packages, depending on their level of environmental compliance. ECOPACK<sup>®</sup> specifications, grade definitions and product status are available at: [www.st.com](http://www.st.com). ECOPACK is an ST trademark.

Table 9. DPAK (TO-252) mechanical data

Dim.	mm		
	Min.	Typ.	Max.
A	2.20		2.40
A1	0.90		1.10
A2	0.03		0.23
b	0.64		0.90
b4	5.20		5.40
c	0.45		0.60
c2	0.48		0.60
D	6.00		6.20
D1		5.10	
E	6.40		6.60
E1		4.70	
e		2.28	
e1	4.40		4.60
H	9.35		10.10
L	1		1.50
L1		2.80	
L2		0.80	
L4	0.60		1
R		0.20	
V2	0°		8°

Figure 18. DPAK (TO-252) drawing

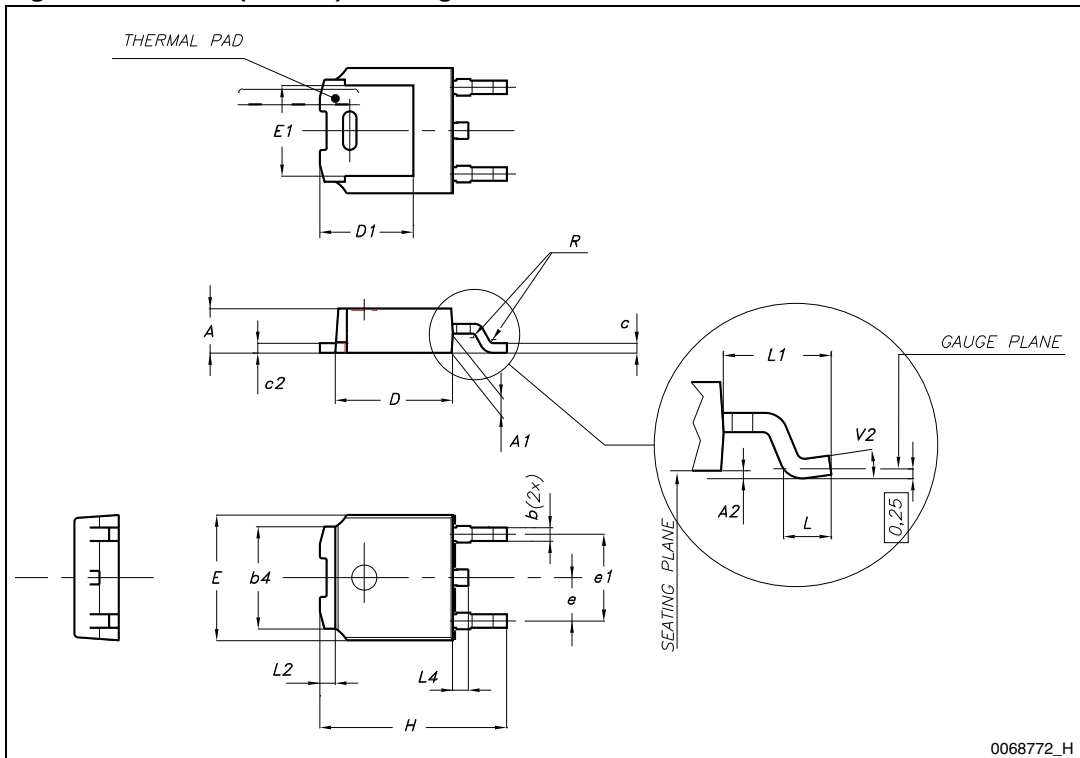
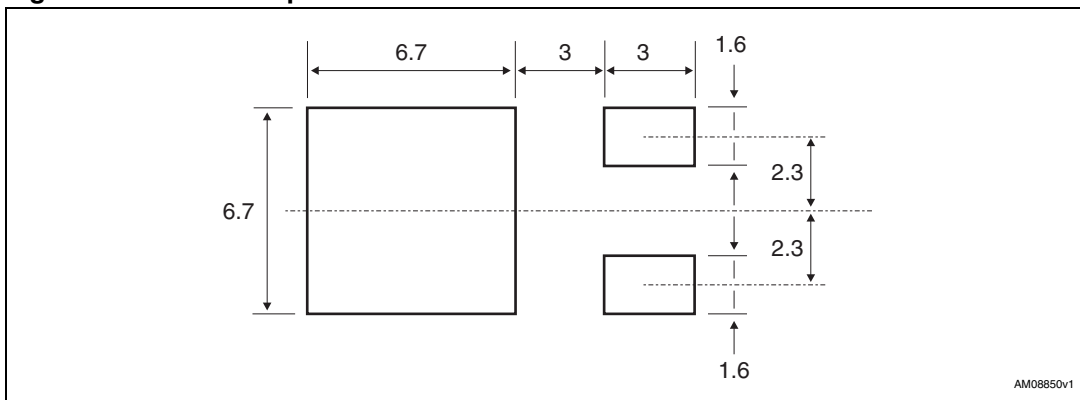


Figure 19. DPAK footprint<sup>(a)</sup>



a. All dimension are in millimeters

## 5 Packaging mechanical data

Table 10. DPAK (TO-252) tape and reel mechanical data

Tape			Reel		
Dim.	mm		Dim.	mm	
	Min.	Max.		Min.	Max.
A0	6.8	7	A		330
B0	10.4	10.6	B	1.5	
B1		12.1	C	12.8	13.2
D	1.5	1.6	D	20.2	
D1	1.5		G	16.4	18.4
E	1.65	1.85	N	50	
F	7.4	7.6	T		22.4
K0	2.55	2.75			
P0	3.9	4.1	Base qty.		2500
P1	7.9	8.1	Bulk qty.		2500
P2	1.9	2.1			
R	40				
T	0.25	0.35			
W	15.7	16.3			

Figure 20. Tape for DPAK (TO-252)

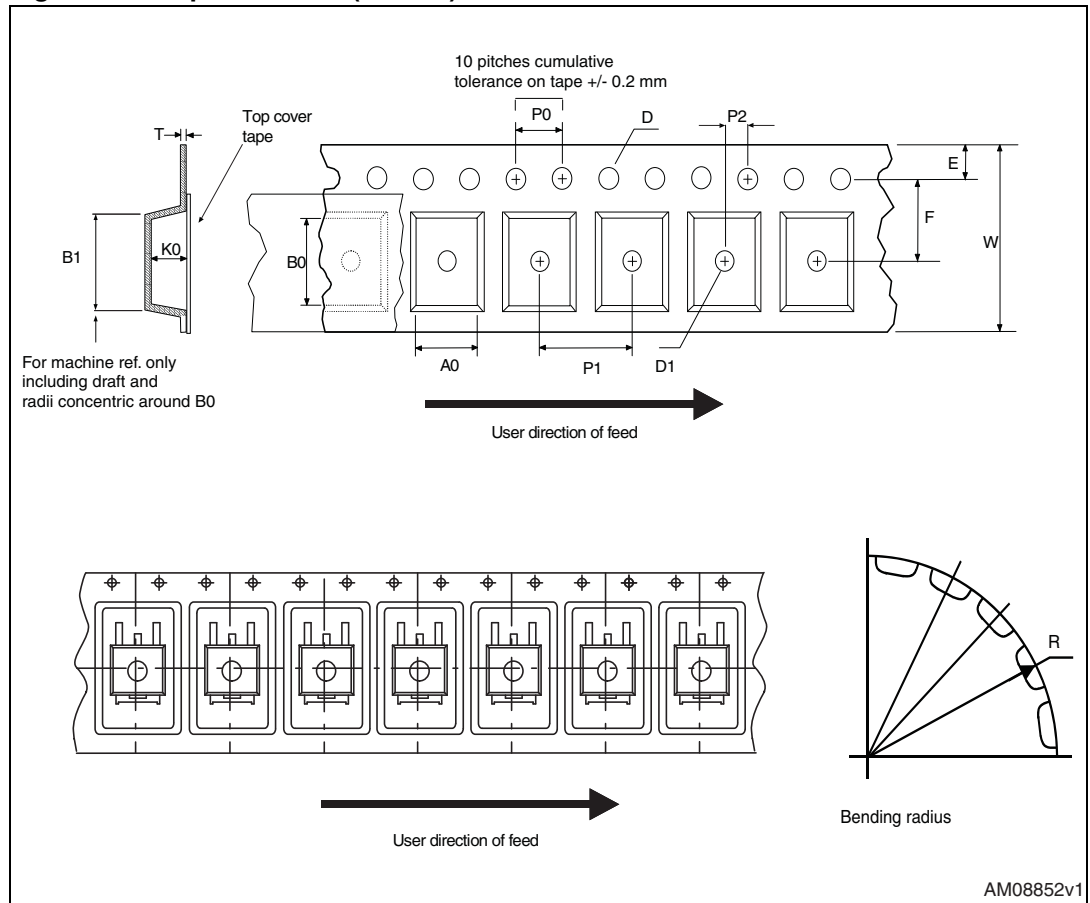
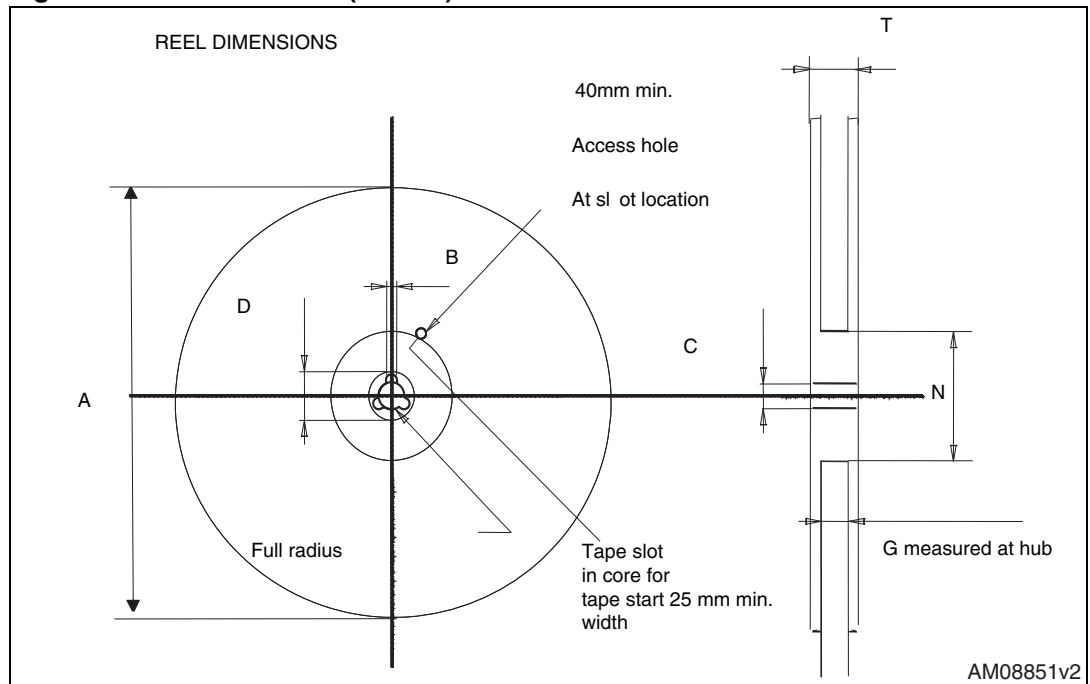


Figure 21. Reel for DPAK (TO-252)



## 6 Revision history

Table 11. Document revision history

Date	Revision	Changes
21-Sep-2011	1	First release.

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