

PHM12NQ20T

TrenchMOS™ standard level FET

Rev. 01 — 30 January 2003

Preliminary data

1. Product profile

1.1 Description

N-channel enhancement mode field-effect transistor in a plastic package using TrenchMOS™ technology.

Product availability:

PHM12NQ20T in SOT685-1 (QLPAK).

1.2 Features

- SOT96 (SO-8) footprint compatible
- Low thermal resistance
- Surface mount package
- Low profile.

1.3 Applications

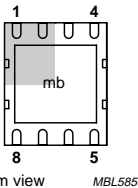
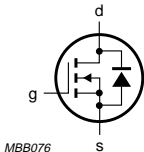
- DC-DC converter primary side switch
- Portable equipment applications.

1.4 Quick reference data

- $V_{DS} \leq 200 \text{ V}$
- $I_D \leq 14.4 \text{ A}$
- $P_{tot} \leq 62.5 \text{ W}$
- $R_{DSon} \leq 130 \text{ m}\Omega$.

2. Pinning information

Table 1: Pinning - SOT685 (QLPAK), simplified outlines and symbol

Pin	Description	Simplified outline	Symbol
1,2,3	source (s)		
4	gate (g)		
5,6,7,8	drain (d)		
mb	mounting base, connected to drain (d)		
SOT685-1 (QLPAK)			

[1] Shaded area indicates pin 1 identifier



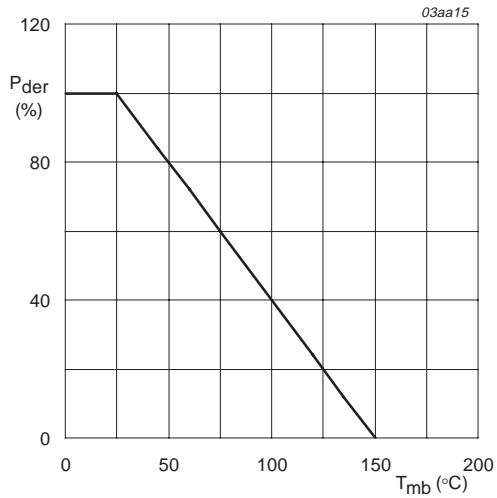
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3. Limiting values

Table 2: Limiting values

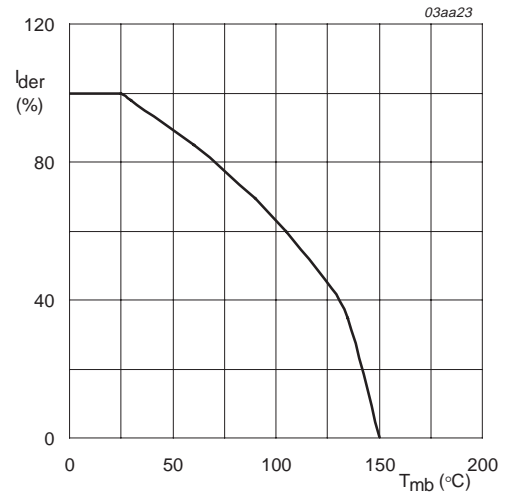
In accordance with the Absolute Maximum Rating System (IEC 60134).

Symbol	Parameter	Conditions	Min	Max	Unit
V_{DS}	drain-source voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$	-	200	V
V_{DGR}	drain-gate voltage (DC)	$25\text{ °C} \leq T_j \leq 150\text{ °C}$; $R_{GS} = 20\text{ k}\Omega$	-	200	V
V_{GS}	gate-source voltage (DC)		-	± 20	V
I_D	drain current (DC)	$T_{mb} = 25\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2 and 3	-	14.4	A
		$T_{mb} = 100\text{ °C}$; $V_{GS} = 10\text{ V}$; Figure 2	-	5.8	A
I_{DM}	peak drain current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$; Figure 3	-	56.8	A
P_{tot}	total power dissipation	$T_{mb} = 25\text{ °C}$; Figure 1	-	62.5	W
T_{stg}	storage temperature		-55	+150	°C
T_j	junction temperature		-55	+150	°C
Source-drain diode					
I_S	source (diode forward) current (DC)	$T_{mb} = 25\text{ °C}$	-	14.4	A
I_{SM}	peak source (diode forward) current	$T_{mb} = 25\text{ °C}$; pulsed; $t_p \leq 10\text{ }\mu\text{s}$	-	56	A



$$P_{der} = \frac{P_{tot}}{P_{tot(25^{\circ}C)}} \times 100\%$$

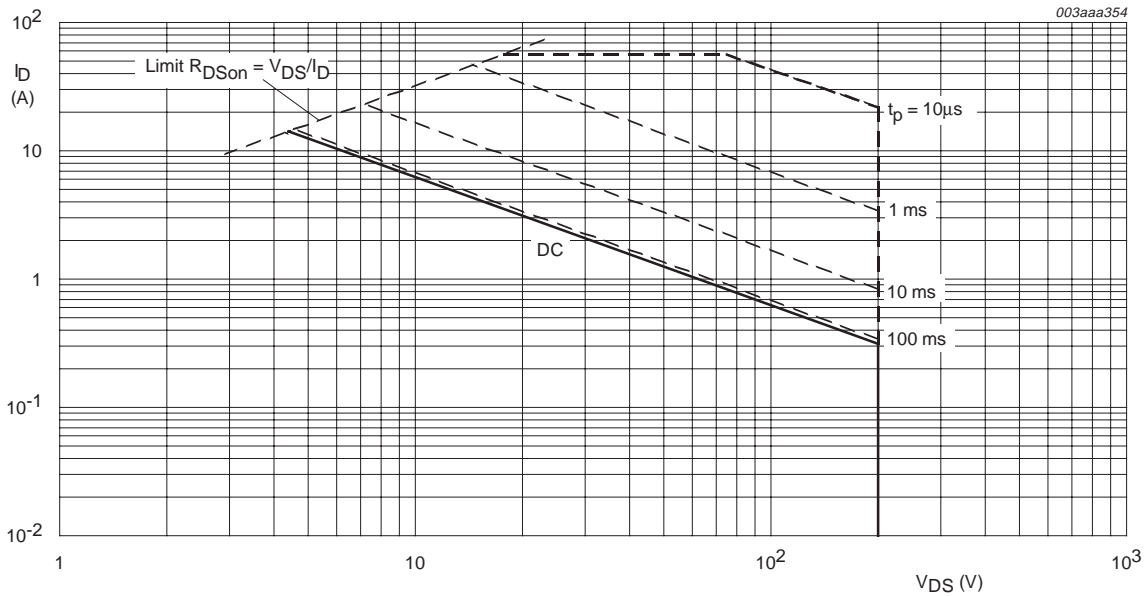
Fig 1. Normalized total power dissipation as a function of mounting base temperature.



V_{GS} ≥ 10 V

$$I_{der} = \frac{I_D}{I_{D(25^{\circ}C)}} \times 100\%$$

Fig 2. Normalized continuous drain current as a function of mounting base temperature.



T_{mb} = 25 °C; I_{DM} is single pulse.

Fig 3. Safe operating area; continuous and peak drain currents as a function of drain-source voltage.

4. Thermal characteristics

Table 3: Thermal characteristics

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
$R_{th(j-mb)}$	thermal resistance from junction to mounting base	Figure 4	-	-	2	K/W

4.1 Transient thermal impedance

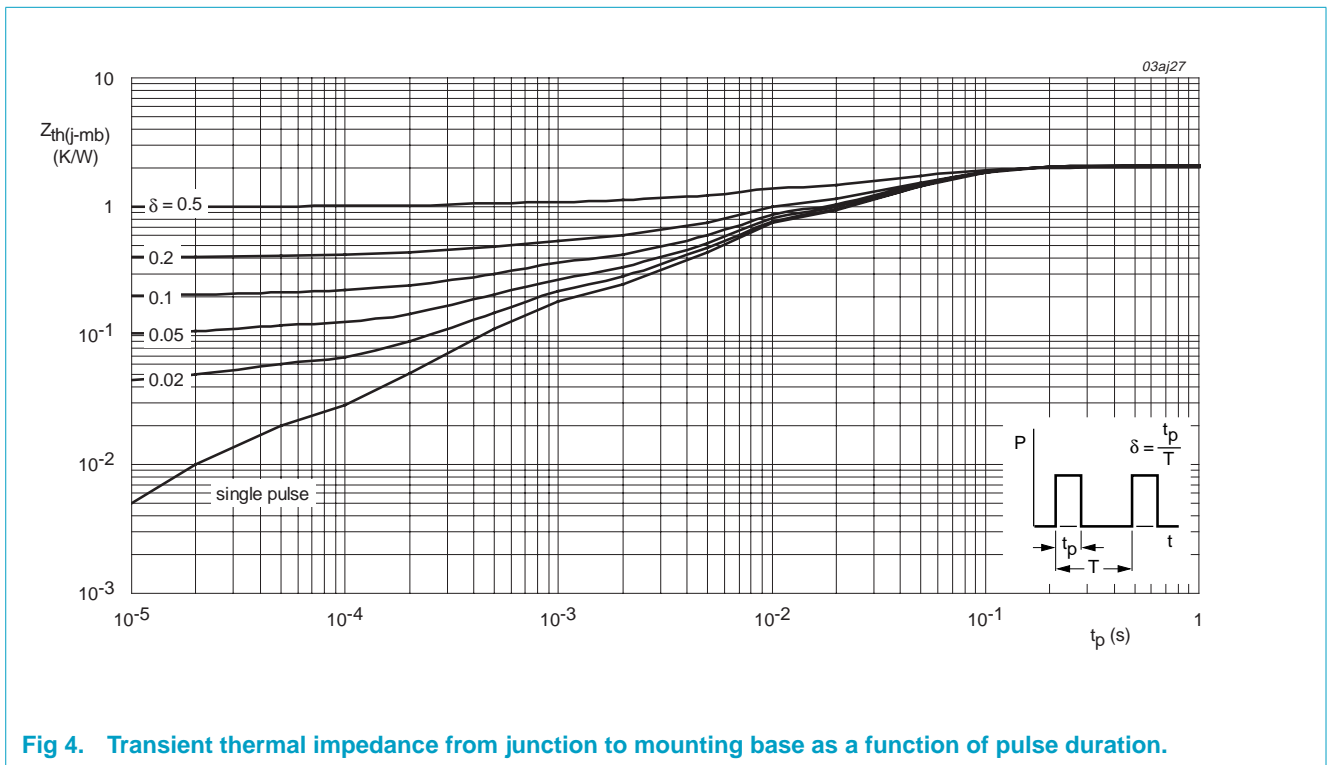
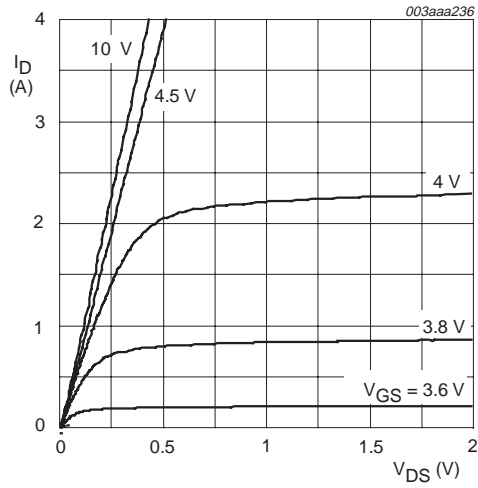


Fig 4. Transient thermal impedance from junction to mounting base as a function of pulse duration.

5. Characteristics

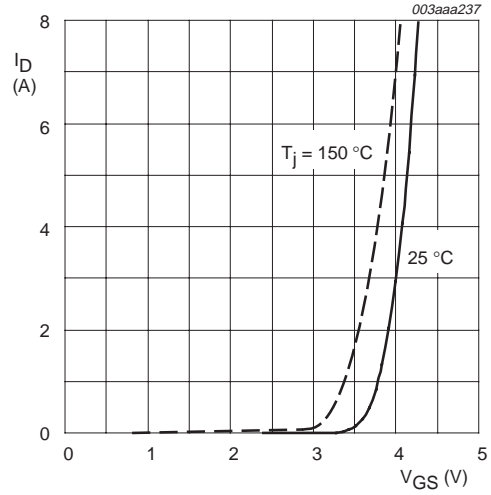
Table 4: Characteristics
T_j = 25 °C unless otherwise specified

Symbol	Parameter	Conditions	Min	Typ	Max	Unit
Static characteristics						
V _{(BR)DSS}	drain-source breakdown voltage	I _D = 250 μA; V _{GS} = 0 V				
		T _j = 25 °C	200	-	-	V
		T _j = -55 °C	178	-	-	V
V _{GS(th)}	gate-source threshold voltage	I _D = 1 mA; V _{DS} = V _{GS} ; Figure 9				
		T _j = 25 °C	2	3	4	V
		T _j = 150 °C	1.2	-	-	V
		T _j = -55 °C	-	-	6	V
I _{DSS}	drain-source leakage current	V _{DS} = 160 V; V _{GS} = 0 V				
		T _j = 25 °C	-	-	1	μA
		T _j = 150 °C	-	-	100	μA
I _{GSS}	gate-source leakage current	V _{GS} = ±10 V; V _{DS} = 0 V	-	10	100	nA
R _{DS(on)}	drain-source on-state resistance	V _{GS} = 10 V; I _D = 12 A; Figure 7 and 8				
		T _j = 25 °C	-	108	130	mΩ
		T _j = 150 °C	-	260	312	mΩ
		V _{GS} = 5 V; I _D = 3 A	-	110	150	mΩ
Dynamic characteristics						
Q _{g(tot)}	total gate charge	I _D = 4 A; V _{DD} = 100 V; V _{GS} = 10 V; Figure 13	-	26	-	nC
Q _{gs}	gate-source charge		-	4	-	nC
Q _{gd}	gate-drain (Miller) charge		-	8.7	-	nC
C _{iss}	input capacitance	V _{GS} = 0 V; V _{DS} = 25 V; f = 1 MHz; Figure 12	-	1230	-	pF
C _{oss}	output capacitance		-	155	-	pF
C _{rss}	reverse transfer capacitance		-	48	-	pF
t _{d(on)}	turn-on delay time	V _{DD} = 100 V; I _D = 4 A; V _{GS} = 10 V; R _G = 6 Ω	-	12.5	-	ns
t _r	rise time		-	10.2	-	ns
t _{d(off)}	turn-off delay time		-	34.5	-	ns
t _f	fall time		-	13.5	-	ns
Source-drain diode						
V _{SD}	source-drain (diode forward) voltage	I _S = 4 A; V _{GS} = 0 V; Figure 11	-	0.71	1.2	V
t _{rr}	reverse recovery time	I _S = 4 A; di _S /dt = -100 A/μs; V _R = 120 V;	-	104	-	ns
Q _r	recovered charge	V _{GS} = 0 V	-	245	-	nC



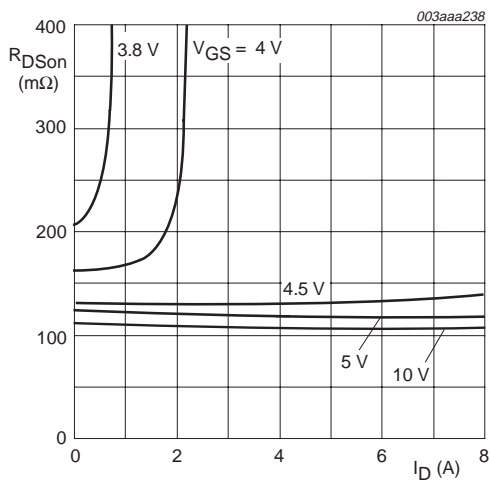
$T_j = 25\text{ }^\circ\text{C}$

Fig 5. Output characteristics: drain current as a function of drain-source voltage; typical values.



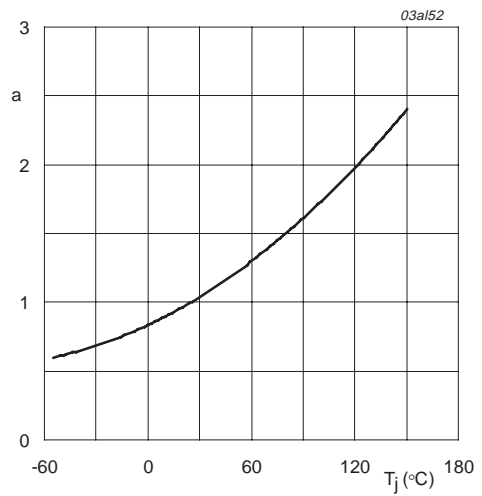
$T_j = 25\text{ }^\circ\text{C}$ and $150\text{ }^\circ\text{C}$; $V_{DS} > I_D \times R_{DSon}$

Fig 6. Transfer characteristics: drain current as a function of gate-source voltage; typical values.



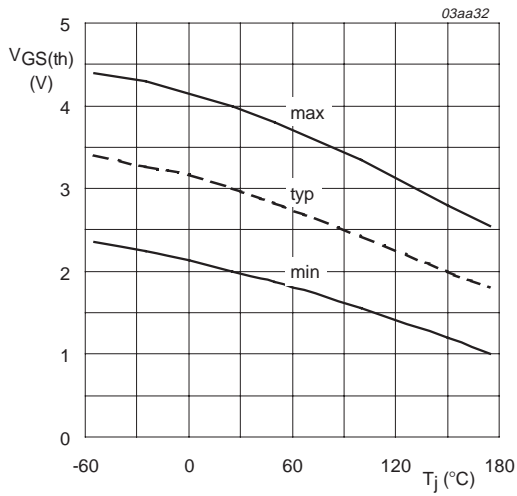
$T_j = 25\text{ }^\circ\text{C}$

Fig 7. Drain-source on-state resistance as a function of drain current; typical values.



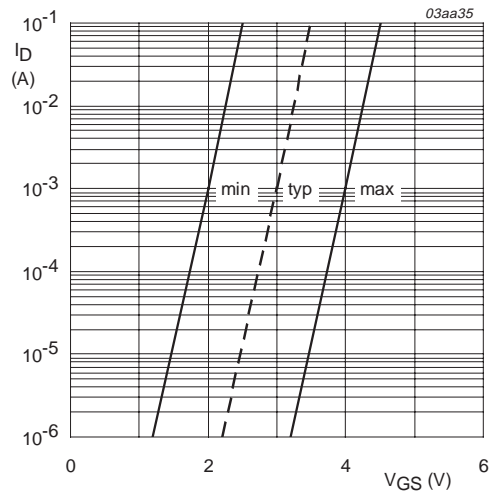
$$a = \frac{R_{DSon}}{R_{DSon(25^\circ\text{C})}}$$

Fig 8. Normalized drain-source on-state resistance factor as a function of junction temperature.



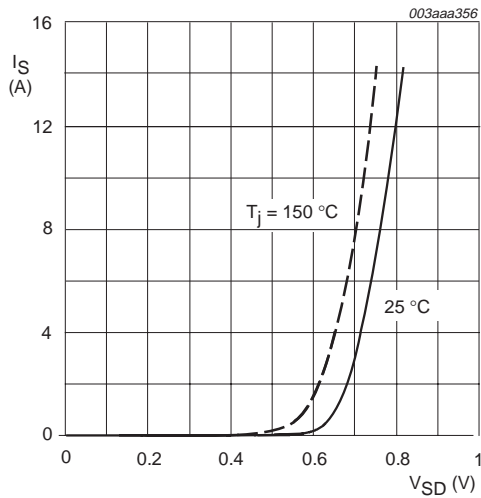
$I_D = 1 \text{ mA}; V_{DS} = V_{GS}$

Fig 9. Gate-source threshold voltage as a function of junction temperature.



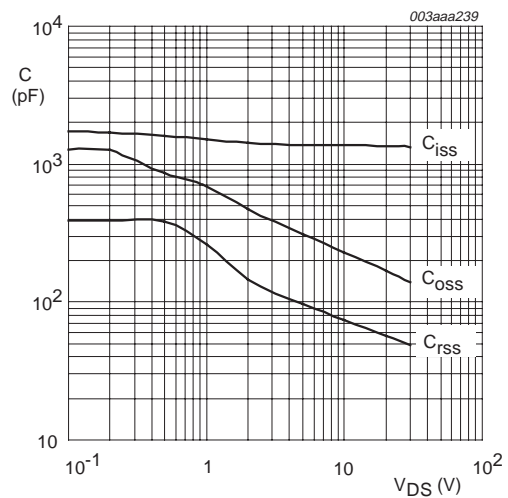
$T_j = 25 \text{ }^\circ\text{C}; V_{DS} = 5 \text{ V}$

Fig 10. Sub-threshold drain current as a function of gate-source voltage.



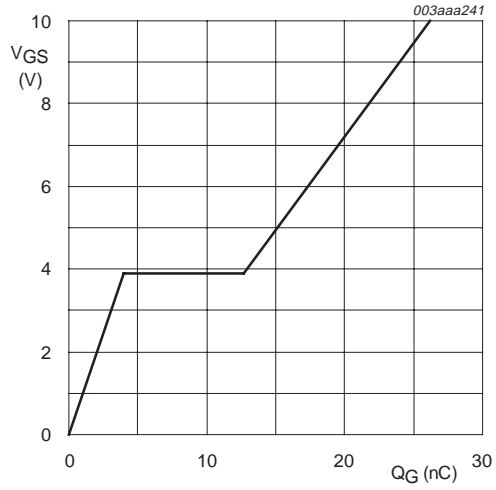
$T_j = 25 \text{ }^\circ\text{C}$ and $150 \text{ }^\circ\text{C}; V_{GS} = 0 \text{ V}$

Fig 11. Source (diode forward) current as a function of source-drain (diode forward) voltage; typical values.



$V_{GS} = 0 \text{ V}; f = 1 \text{ MHz}$

Fig 12. Input, output and reverse transfer capacitances as a function of drain-source voltage; typical values.



$I_D = 4 \text{ A}; V_{DD} = 100 \text{ V}$

Fig 13. Gate-source voltage as a function of gate charge; typical values.

6. Package outline

HVSON8: plastic thermal enhanced very thin small outline package; no leads; 8 terminals; body 6 x 5 x 0.85 mm

SOT685-1

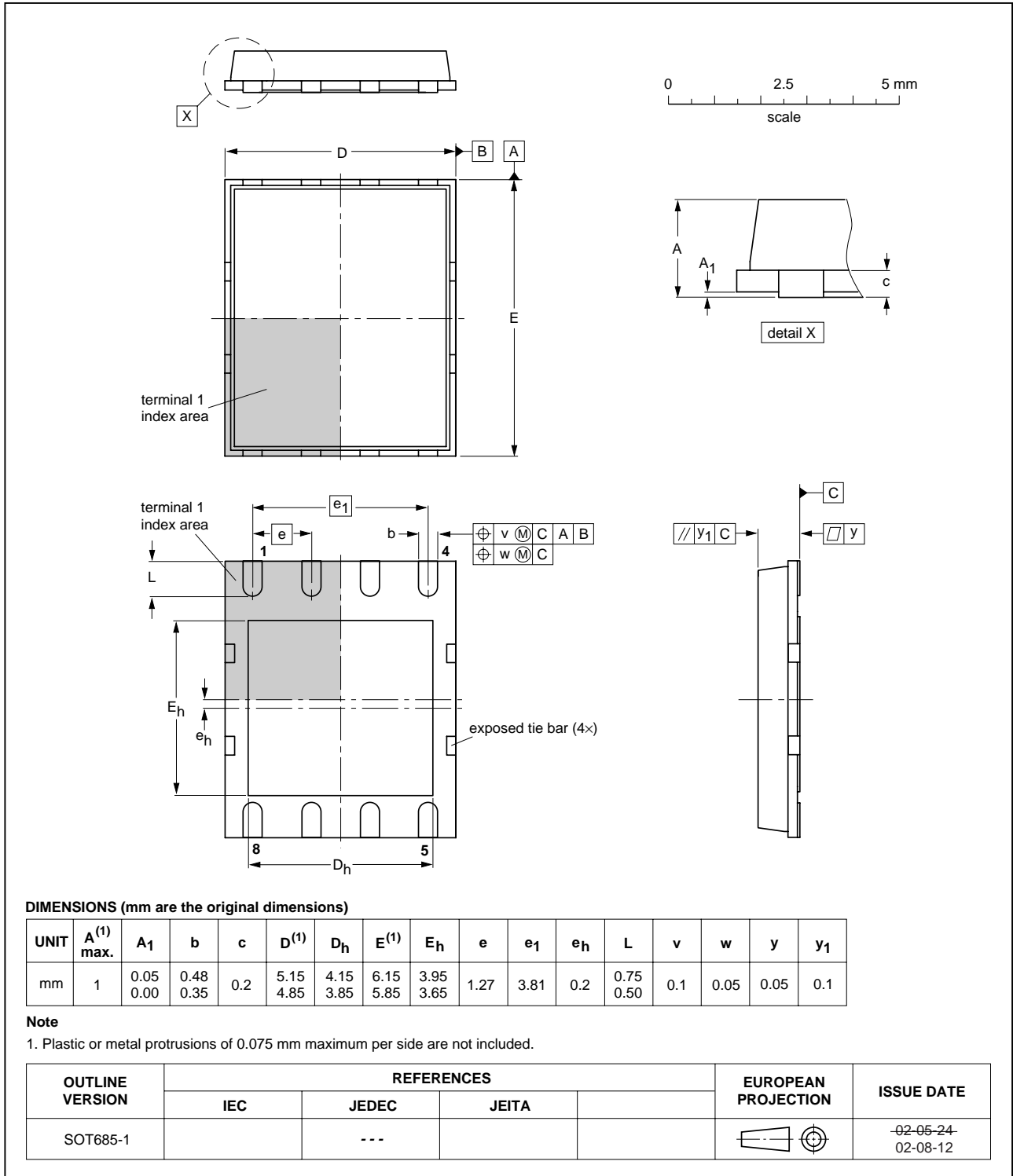


Fig 14. SOT685-1 (QLPAK).

7. Revision history

Table 5: Revision history

Rev	Date	CPCN	Description
01	20030130	-	Preliminary data (9397 750 10876)

8. Data sheet status

Level	Data sheet status ^[1]	Product status ^{[2][3]}	Definition
I	Objective data	Development	This data sheet contains data from the objective specification for product development. Philips Semiconductors reserves the right to change the specification in any manner without notice.
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