



**THE DATASHEET OF
NCP4625DSN50T1G**



NCP4625

300 mA, 10 V, Low Dropout Regulator

The NCP4625 is a CMOS Linear voltage regulator with 300 mA output current capability. The device is capable of operating with input voltages up to 10 V, with high output voltage accuracy and low temperature–drift coefficient. The NCP4625 is easy to use, with output current fold–back protection and a thermal shutdown circuit included. A Chip Enable function is included to save power by lowering supply current.

Features

- Operating Input Voltage Range: 2.6 V to 10 V
- Output Voltage Range: 1.2 to 6.0 V (available in 0.1 V steps)
- Low Supply Current: 23 μ A
- Very Low Dropout:
 - ◆ 200 mV ($I_{OUT} = 100$ mA, $V_{IN} = 3.0$ V)
 - ◆ 770 mV ($I_{OUT} = 300$ mA, $V_{IN} = 2.8$ V)
- High PSRR: 70 dB at 1 kHz
- Line Regulation 0.02%/V Typ
- Current Fold Back Protection
- Thermal Shutdown Protection
- Stable with Ceramic Capacitors
- Available in SC–70, SOT89 and SOT–23 Package
- These are Pb–Free Devices

Typical Applications

- Battery products powered by Two Lithium Ion cells
- Networking and Communication Equipment
- Cameras, DVRs, STB and Camcorders
- Toys, industrial applications

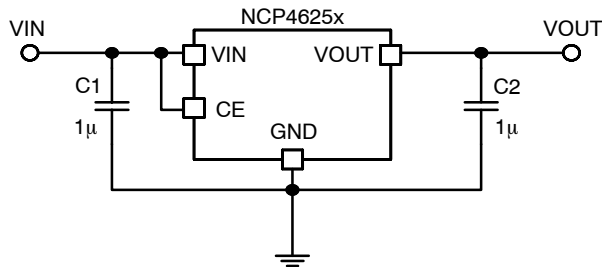


Figure 1. Typical Application Schematic



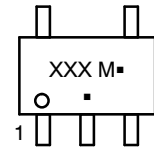
ON Semiconductor™

<http://onsemi.com>

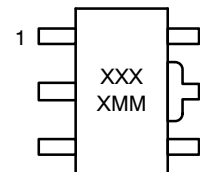
MARKING DIAGRAMS



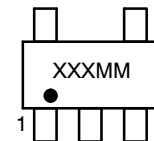
SC–70
CASE 419A



SOT–89 5
CASE 528AB



SOT–23–5
CASE 1212



XX, XXX= Specific Device Code
M, MM = Date Code
A = Assembly Location
Y = Year
W = Work Week
▪ = Pb–Free Package

(*Note: Microdot may be in either location)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 14 of this data sheet.

NCP4625

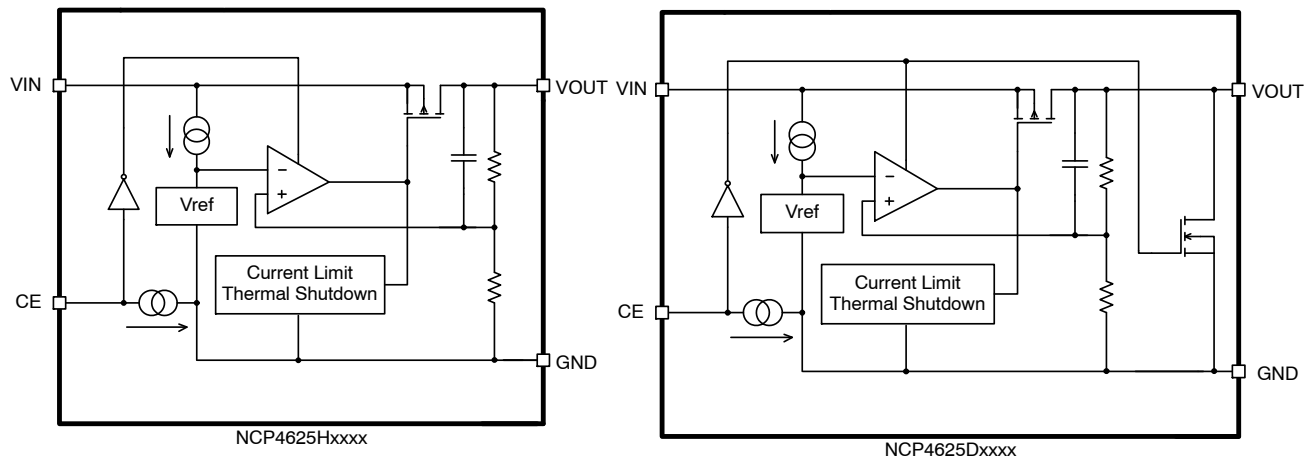


Figure 2. Simplified Schematic Block Diagram

PIN FUNCTION DESCRIPTION

Pin No. SOT89	Pin No. SC-70	Pin No. SOT23	Pin Name	Description
5	5	1	VIN	Input pin
2	3	2	GND	Ground
3	1	3	CE	Chip enable pin (Active "H")
1	4	5	VOUT	Output pin
4	2	4	NC	No connection

ABSOLUTE MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Input Voltage (Note 1)	V_{IN}	12.0	V
Output Voltage	V_{OUT}	-0.3 to $V_{IN} + 0.3$	V
Chip Enable Input	V_{CE}	12.0	V
Output Current	I_{OUT}	330	mA
Power Dissipation SOT89	P_D	900	mW
Power Dissipation SC-70		380	
Power Dissipation SOT23		420	
Junction Temperature	T_J	-40 to 150	°C
Storage Temperature	T_{STG}	-55 to 125	°C
ESD Capability, Human Body Model (Note 2)	ESD_{HBM}	2000	V
ESD Capability, Machine Model (Note 2)	ESD_{MM}	200	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Refer to ELECTRICAL CHARACTERISTICS and APPLICATION INFORMATION for Safe Operating Area.
2. This device series incorporates ESD protection and is tested by the following methods:
 ESD Human Body Model tested per AEC-Q100-002 (EIA/JESD22-A114)
 ESD Machine Model tested per AEC-Q100-003 (EIA/JESD22-A115)
 Latchup Current Maximum Rating tested per JEDEC standard: JESD78.

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THERMAL CHARACTERISTICS

Rating	Symbol	Value	Unit
Thermal Characteristics, SOT89 Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	111	$^{\circ}\text{C}/\text{W}$
Thermal Characteristics, SOT23 Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	238	$^{\circ}\text{C}/\text{W}$
Thermal Characteristics, SC-70 Thermal Resistance, Junction-to-Air	$R_{\theta JA}$	263	$^{\circ}\text{C}/\text{W}$

ELECTRICAL CHARACTERISTICS $-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$; $V_{IN} = V_{OUT(NOM)} + 1\text{ V}$; $I_{OUT} = 1\text{ mA}$, $C_{IN} = C_{OUT} = 0.47\text{ }\mu\text{F}$, unless otherwise noted. Typical values are at $T_A = +25^{\circ}\text{C}$.

Parameter	Test Conditions	Symbol	Min	Typ	Max	Unit	
Operating Input Voltage		V_{IN}	2.6		10	V	
Output Voltage	$T_A = +25^{\circ}\text{C}$	$V_{OUT} > 1.5\text{ V}$	V_{OUT}	x0.99	x1.01	V	
		$V_{OUT} \leq 1.5\text{ V}$		-15	15	mV	
	$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$	$V_{OUT} > 1.5\text{ V}$	x0.974	x1.023	V		
		$V_{OUT} \leq 1.5\text{ V}$	-40	35	mV		
Output Voltage Temp. Coefficient	$-40^{\circ}\text{C} \leq T_A \leq 85^{\circ}\text{C}$			± 80		ppm/ $^{\circ}\text{C}$	
Line Regulation	$V_{OUT(NOM)} + 0.5\text{ V}$ or 2.6 V (whichever is higher) $\leq V_{IN} \leq 10\text{ V}$	LineReg		0.02	0.2	%/V	
Load Regulation	$I_{OUT} = 0.1\text{ mA}$ to 300 mA	LineReg		10	70	mV	
Dropout Voltage	$I_{OUT} = 300\text{ mA}$	$1.2\text{ V} \leq V_{OUT} < 1.3\text{ V}$	V_{DO}		1.40	1.80	V
		$1.3\text{ V} \leq V_{OUT} < 1.5\text{ V}$			1.35	1.75	
		$1.5\text{ V} \leq V_{OUT} < 1.8\text{ V}$			1.20	1.55	
		$1.8\text{ V} \leq V_{OUT} < 2.3\text{ V}$			0.98	1.30	
		$2.3\text{ V} \leq V_{OUT} < 3.0\text{ V}$			0.77	1.08	
		$3.0\text{ V} \leq V_{OUT} < 4.0\text{ V}$			0.60	0.85	
		$4.0\text{ V} \leq V_{OUT} < 6.0\text{ V}$			0.50	0.75	
Output Current		I_{OUT}	300			mA	
Short Current Limit	$V_{OUT} = 0\text{ V}$	I_{SC}		40		mA	
Quiescent Current		I_Q		23	40	μA	
Standby Current	$V_{IN} = 10\text{ V}$, $V_{CE} = 0\text{ V}$, $T_A = 25^{\circ}\text{C}$	I_{STB}		0.1	1.0	μA	
CE Pin Threshold Voltage	CE Input Voltage "H"	V_{CEH}	1.7			V	
	CE Input Voltage "L"	V_{CEL}			0.8		
CE Pull Down Current		I_{CEPD}		0.3		μA	
Power Supply Rejection Ratio	$V_{IN} = V_{OUT} + 1\text{ V}$ or 3.0 V whichever is higher, $\Delta V_{IN} = 0.2\text{ V}_{pk-pk}$, $I_{OUT} = 30\text{ mA}$, $f = 1\text{ kHz}$	PSRR		70		dB	
Output Noise Voltage	$f = 10\text{ Hz}$ to 100 kHz	V_N		85		μV_{rms}	
Low Output N-channel Tr. On Resistance	$V_{IN} = 7\text{ V}$, $V_{CE} = 0\text{ V}$, $V_{OUT} = 1.2\text{ V}$, $V_{IN} = 2.6\text{ V}$, $I_{OUT} = 30\text{ mA}$	R_{LOW}		250		Ω	
Thermal Shutdown Temperature		T_{TSD}		165		$^{\circ}\text{C}$	
Thermal Shutdown Release		T_{TSR}		110		$^{\circ}\text{C}$	

TYPICAL CHARACTERISTICS

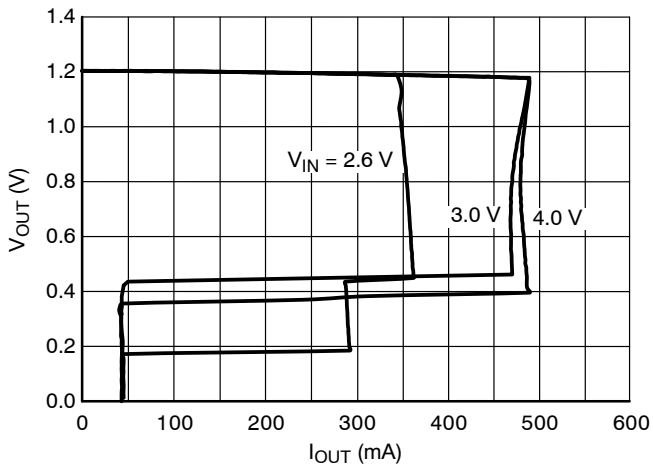


Figure 3. Output Voltage vs. Output Current
1.2 V Version ($T_J = 25^\circ\text{C}$)

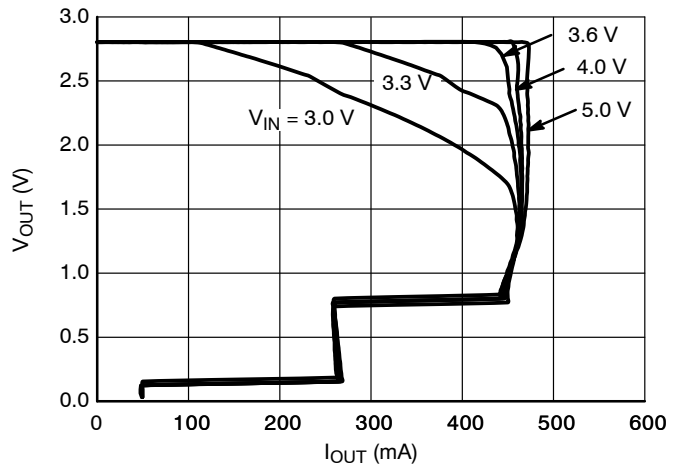


Figure 4. Output Voltage vs. Output Current
2.8 V Version ($T_J = 25^\circ\text{C}$)

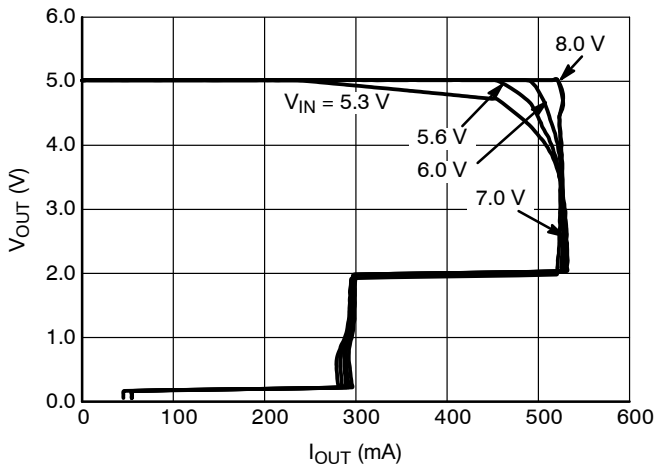


Figure 5. Output Voltage vs. Output Current
5.0 V Version ($T_J = 25^\circ\text{C}$)

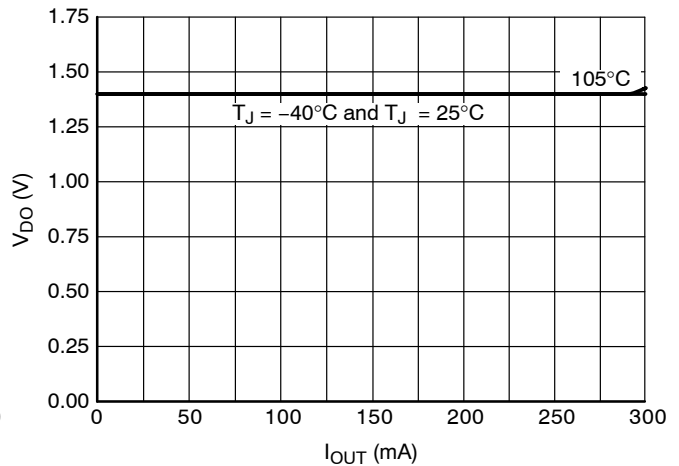


Figure 6. Dropout Voltage vs. Output Current
1.2 V Version

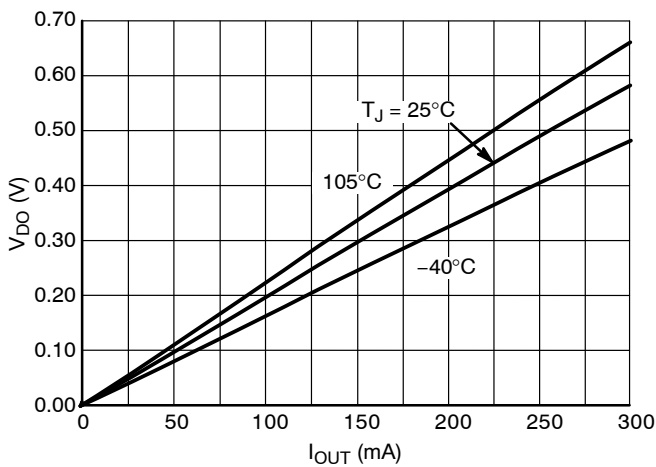


Figure 7. Dropout Voltage vs. Output Current
2.8 V Version

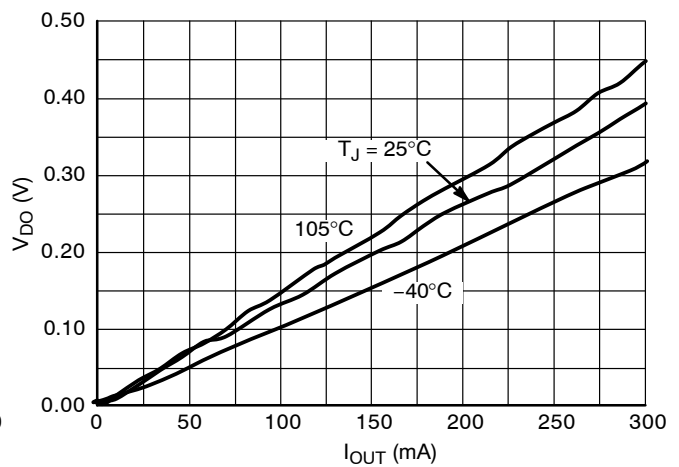


Figure 8. Dropout Voltage vs. Output Current
5.0 V Version

TYPICAL CHARACTERISTICS

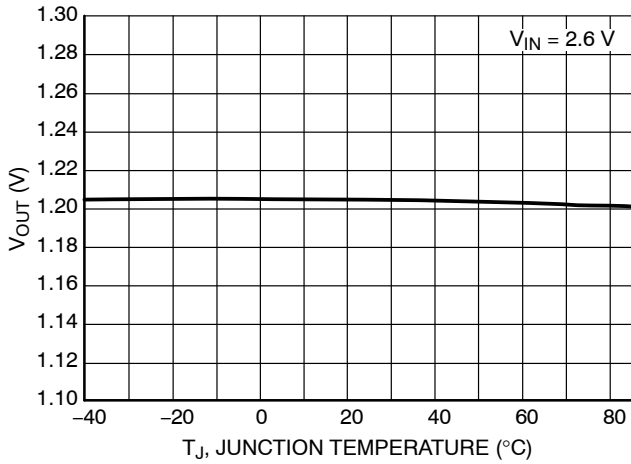


Figure 9. Output Voltage vs. Temperature, 1.2 V Version

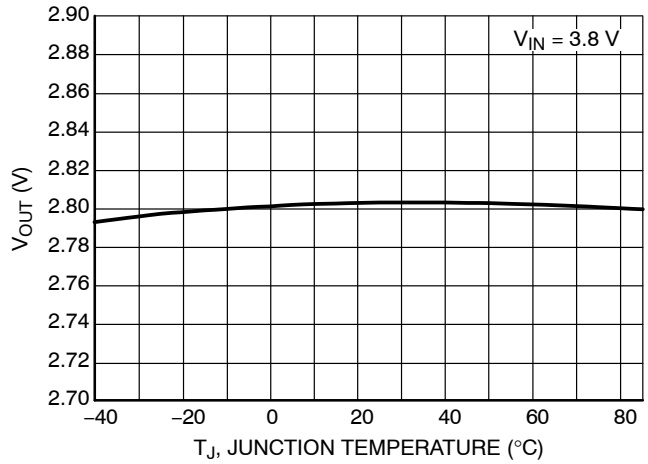


Figure 10. Output Voltage vs. Temperature, 2.8 V Version

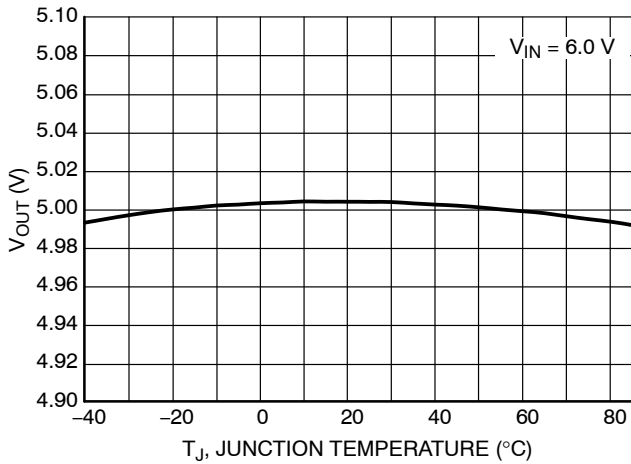


Figure 11. Output Voltage vs. Temperature, 5.0 V Version

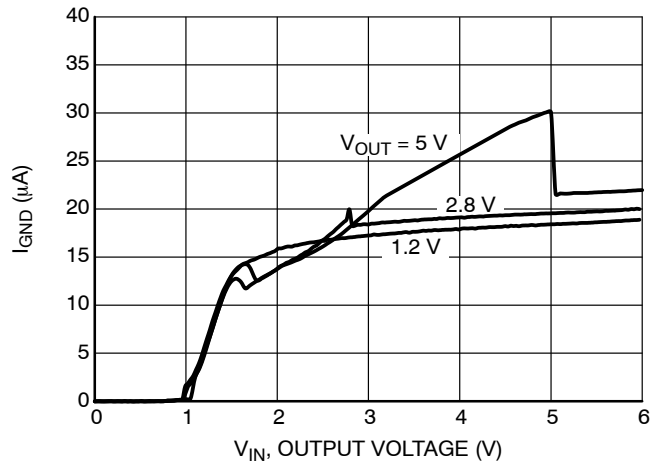


Figure 12. Supply Current vs. Input Voltage

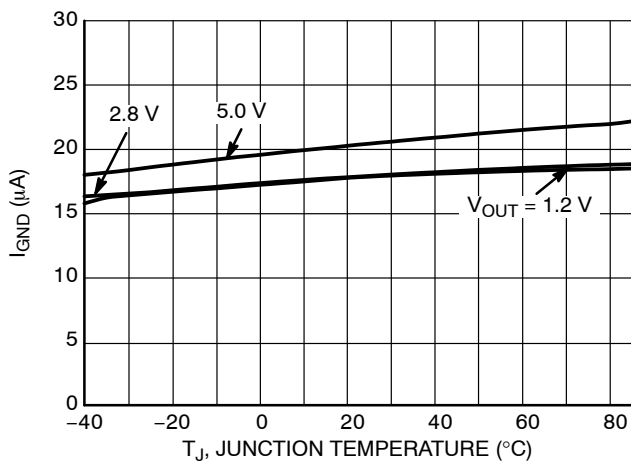


Figure 13. Supply Current vs. Temperature, 1.2 V Version

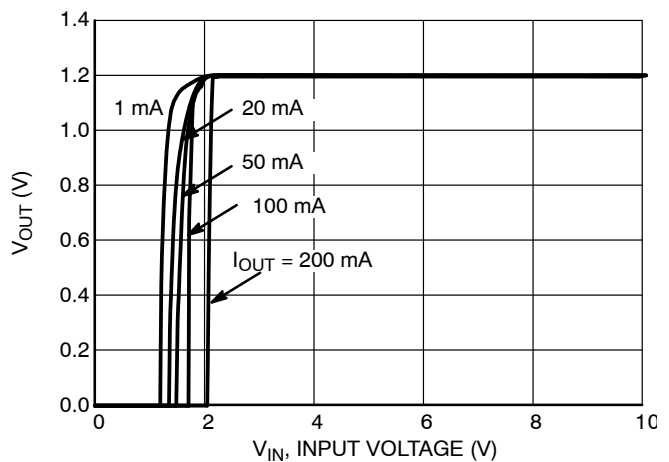


Figure 14. Output Voltage vs. Input Voltage, 1.2 V Version

TYPICAL CHARACTERISTICS

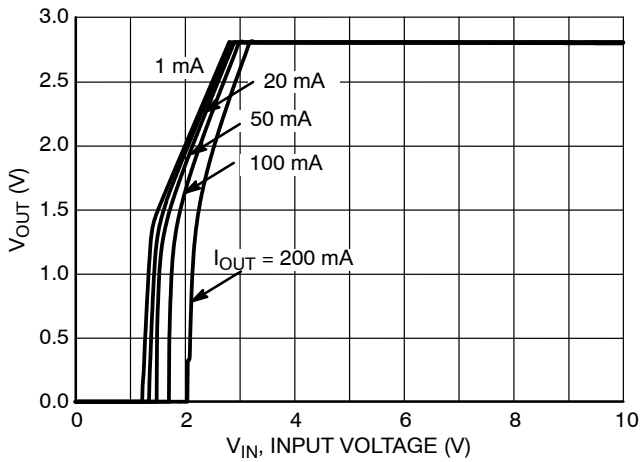


Figure 15. Output Voltage vs. Input Voltage, 2.8 V Version

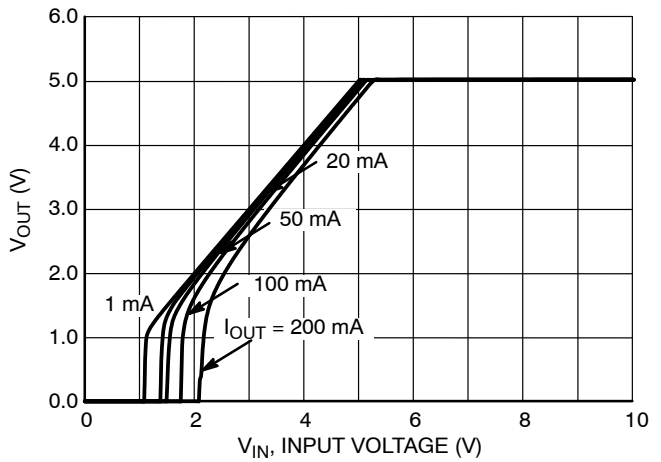


Figure 16. Output Voltage vs. Input Voltage, 5.0 V Version

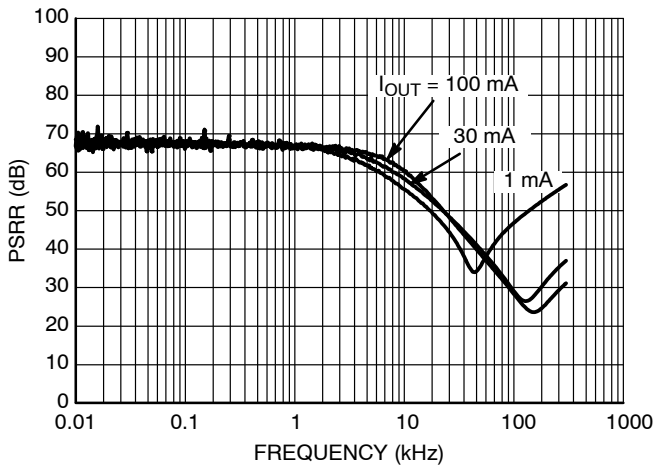


Figure 17. PSRR, 1.2 V Version, $V_{IN} = 2.6 V$

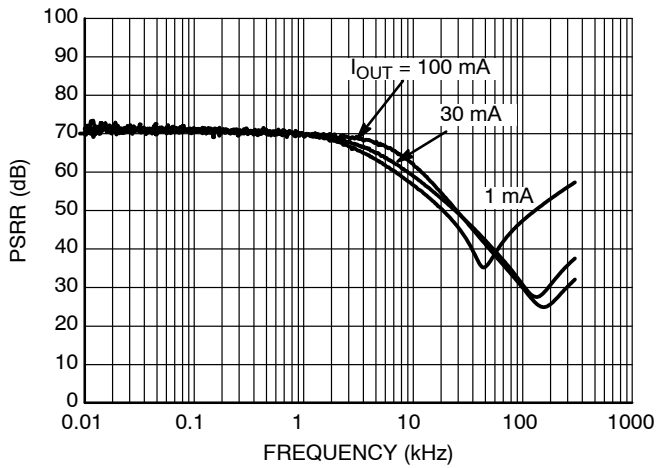


Figure 18. PSRR, 1.2 V Version, $V_{IN} = 3.0 V$

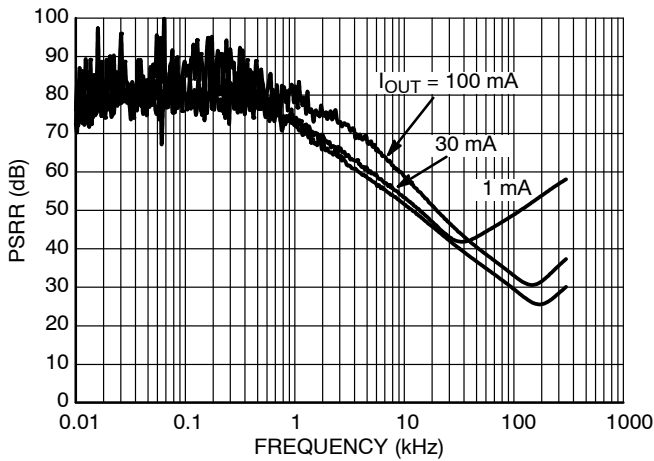


Figure 19. PSRR, 2.8 V Version, $V_{IN} = 3.8 V$

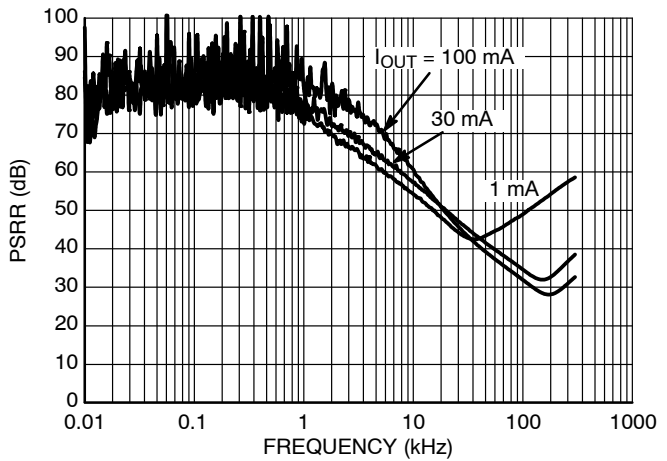


Figure 20. PSRR, 2.8 V Version, $V_{IN} = 4.8 V$

TYPICAL CHARACTERISTICS

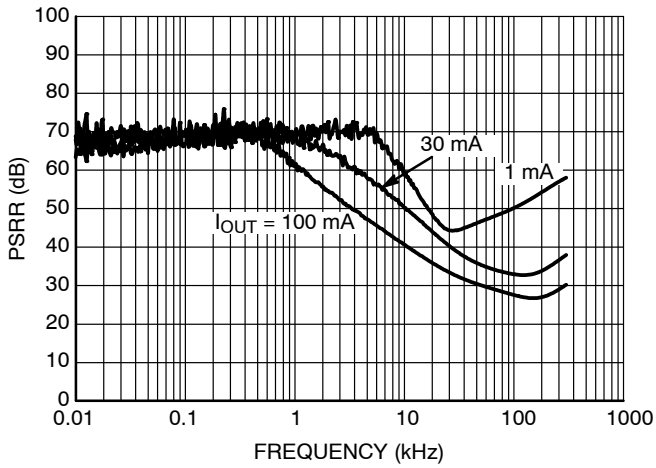


Figure 21. PSRR, 5.0 V Version, $V_{IN} = 6.0$ V

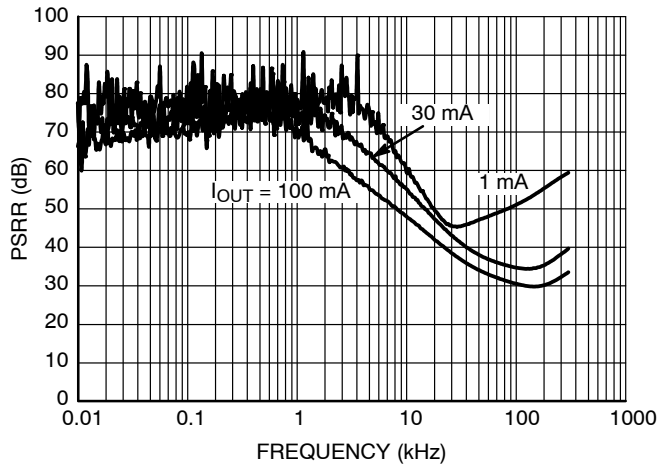


Figure 22. PSRR, 5.0 V Version, $V_{IN} = 7.0$ V

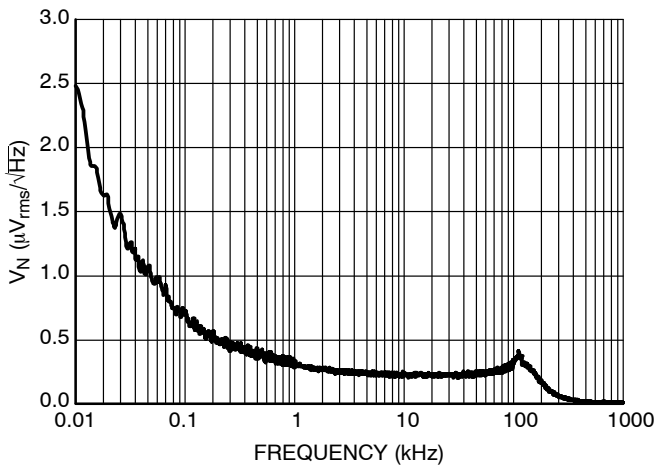


Figure 23. Output Voltage Noise, 1.2 V Version, $V_{IN} = 2.6$ V

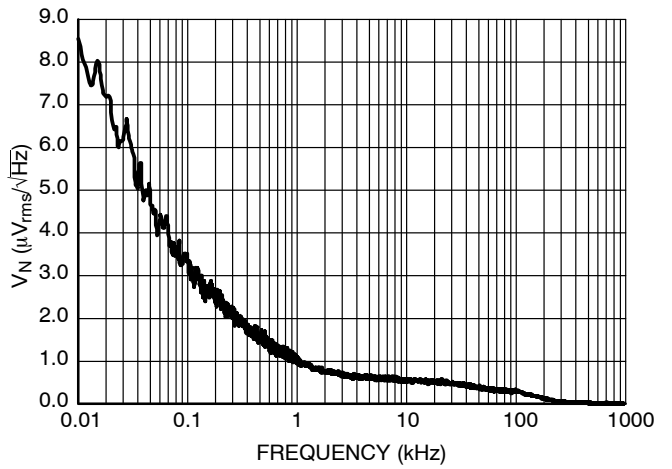


Figure 24. Output Voltage Noise, 2.8 V Version, $V_{IN} = 3.8$ V

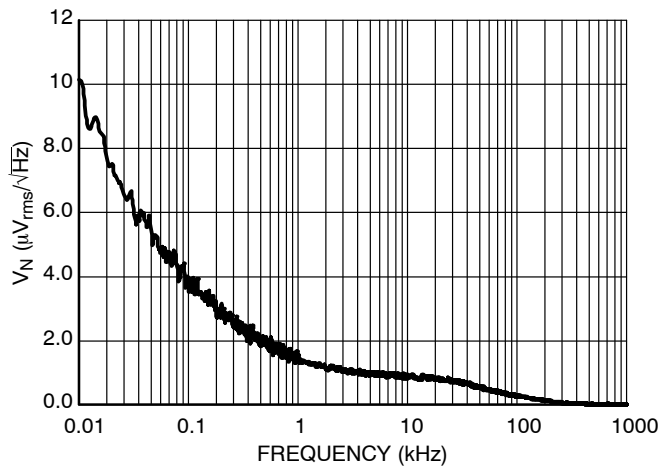


Figure 25. Output Voltage Noise, 5.0 V Version, $V_{IN} = 6.0$ V

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TYPICAL CHARACTERISTICS

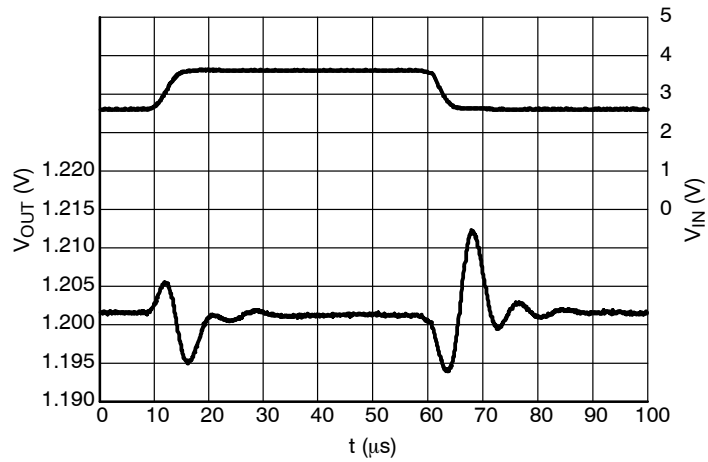


Figure 26. Line Transients, 1.2 V Version,
 $t_R = t_F = 5 \mu\text{s}$, $I_{OUT} = 30 \text{ mA}$

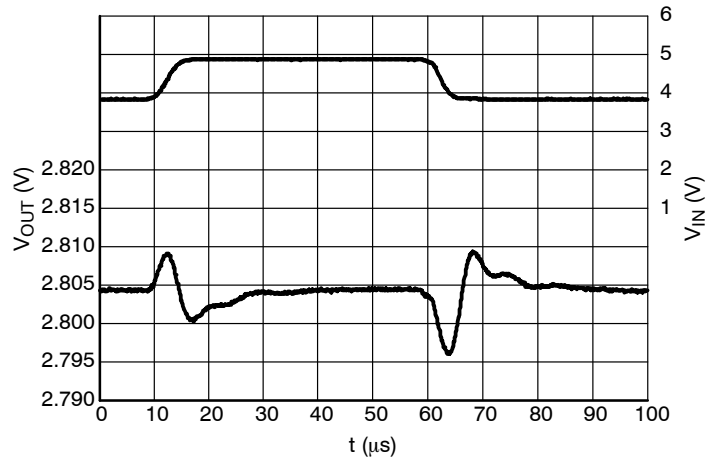


Figure 27. Line Transients, 2.8 V Version,
 $t_R = t_F = 5 \mu\text{s}$, $I_{OUT} = 30 \text{ mA}$

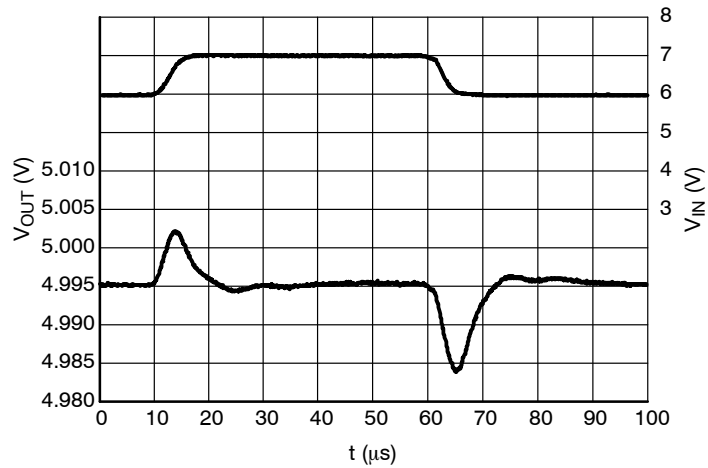
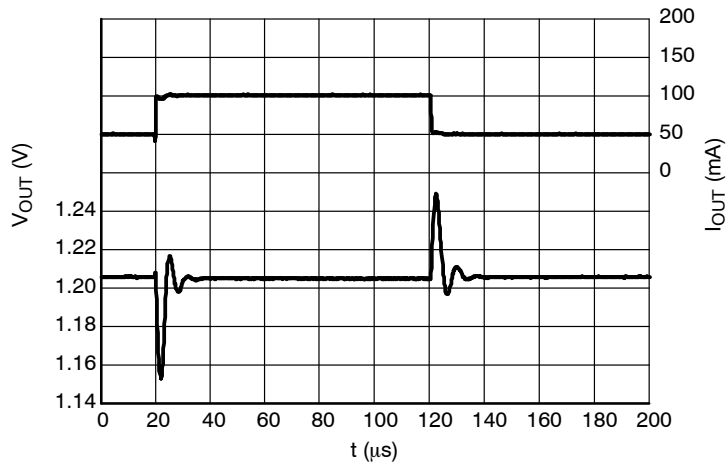


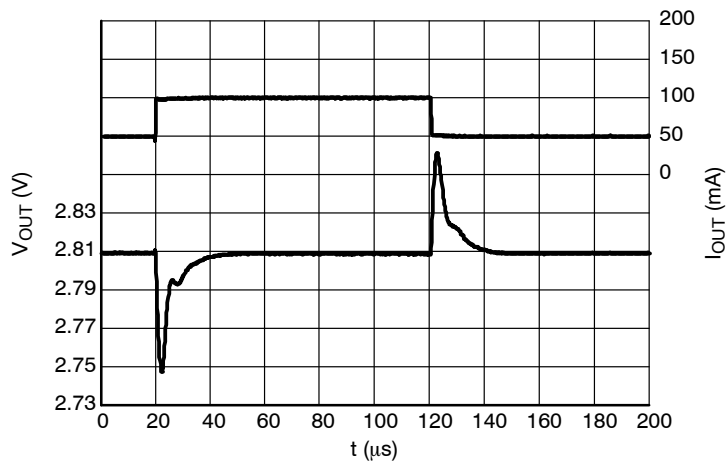
Figure 28. Line Transients, 5.0 V Version,
 $t_R = t_F = 5 \mu\text{s}$, $I_{OUT} = 30 \text{ mA}$

NCP4625

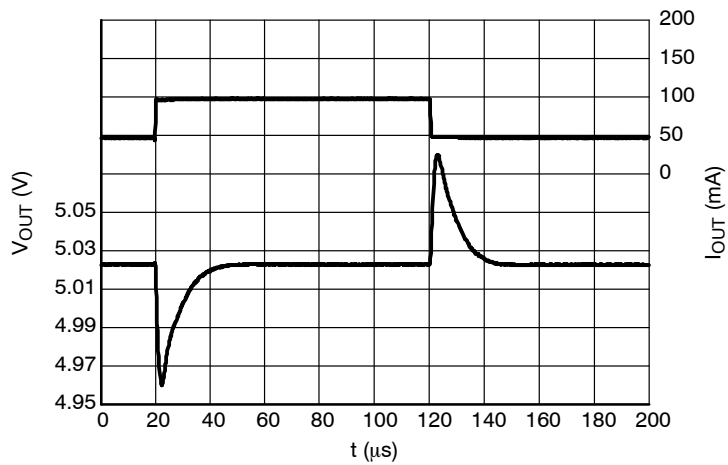
TYPICAL CHARACTERISTICS



**Figure 29. Load Transients, 1.2 V Version,
 $I_{OUT} = 50 - 100 \text{ mA}$, $t_R = t_F = 0.5 \mu s$, $V_{IN} = 2.6 \text{ V}$**



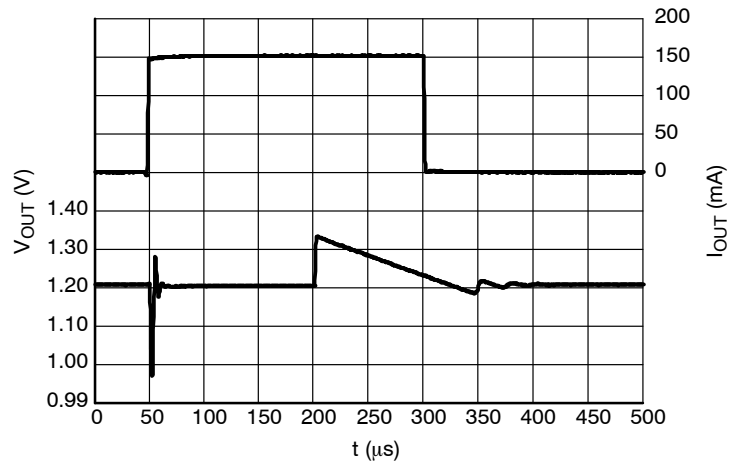
**Figure 30. Load Transients, 2.8 V Version,
 $I_{OUT} = 50 - 100 \text{ mA}$, $t_R = t_F = 0.5 \mu s$, $V_{IN} = 3.8 \text{ V}$**



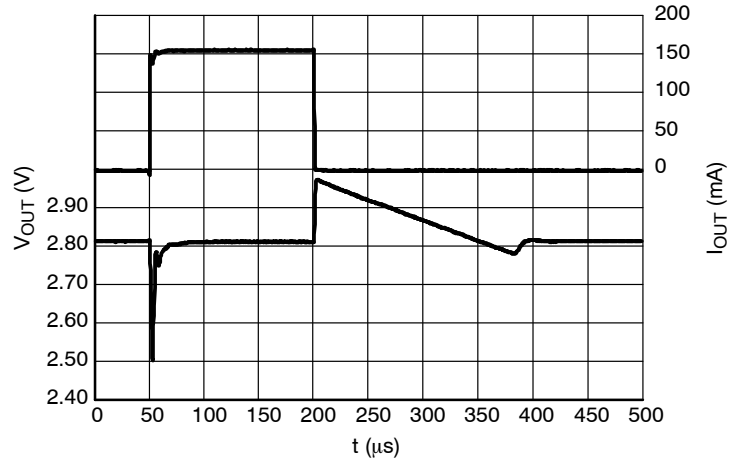
**Figure 31. Load Transients, 5.0 V Version,
 $I_{OUT} = 50 - 100 \text{ mA}$, $t_R = t_F = 0.5 \mu s$, $V_{IN} = 6.0 \text{ V}$**

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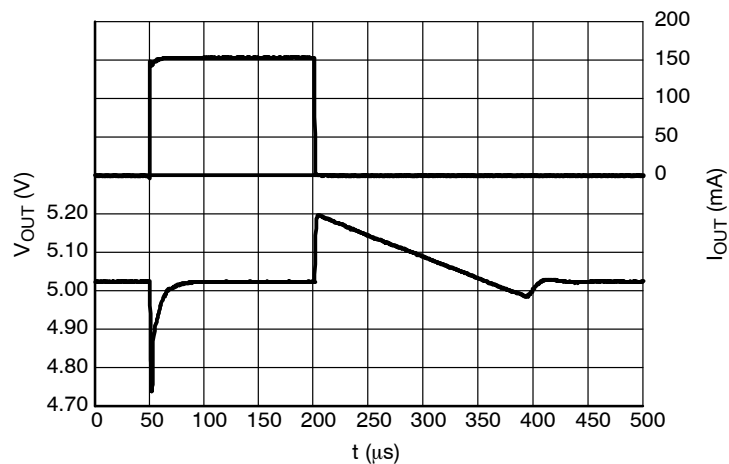
TYPICAL CHARACTERISTICS



**Figure 32. Load Transients, 1.2 V Version,
 $I_{OUT} = 1 - 150 \text{ mA}$, $t_R = t_F = 0.5 \mu\text{s}$, $V_{IN} = 2.6 \text{ V}$**



**Figure 33. Load Transients, 2.8 V Version,
 $I_{OUT} = 1 - 150 \text{ mA}$, $t_R = t_F = 0.5 \mu\text{s}$, $V_{IN} = 3.8 \text{ V}$**



**Figure 34. Load Transients, 5.0 V Version,
 $I_{OUT} = 1 - 150 \text{ mA}$, $t_R = t_F = 0.5 \mu\text{s}$, $V_{IN} = 6.0 \text{ V}$**

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TYPICAL CHARACTERISTICS

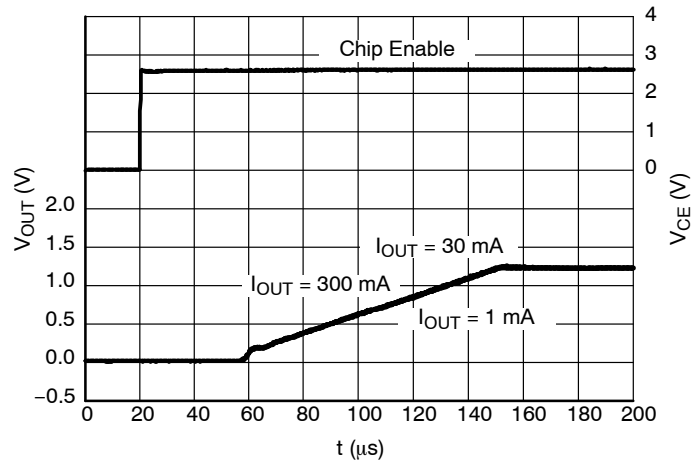


Figure 35. Start-up, 1.2 V Version, $V_{IN} = 2.6$ V

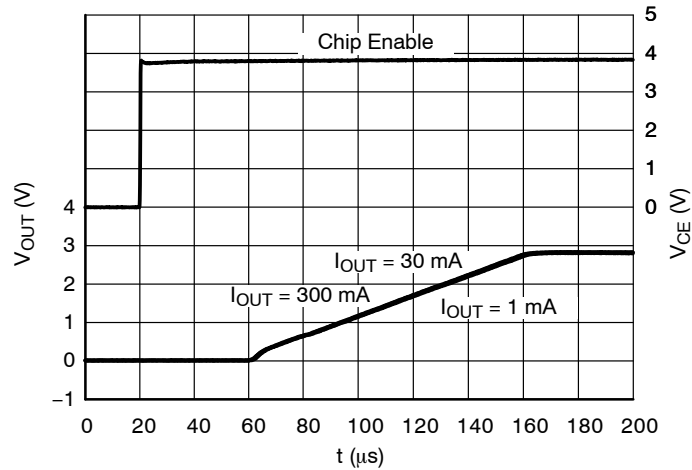


Figure 36. Start-up, 2.8 V Version, $V_{IN} = 3.8$ V

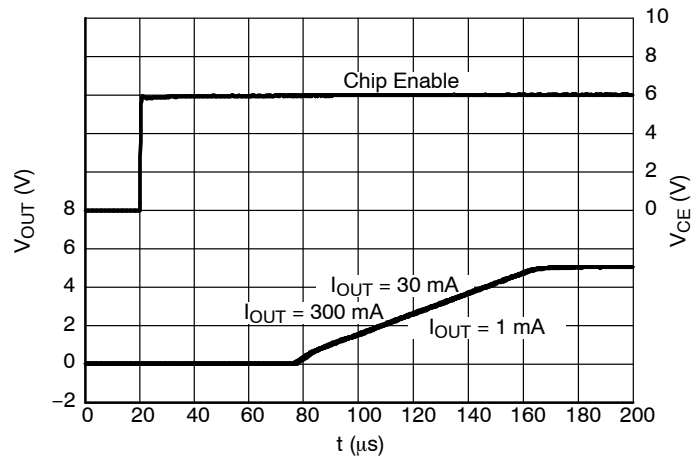


Figure 37. Start-up, 5.0 V Version, $V_{IN} = 6.0$ V

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TYPICAL CHARACTERISTICS

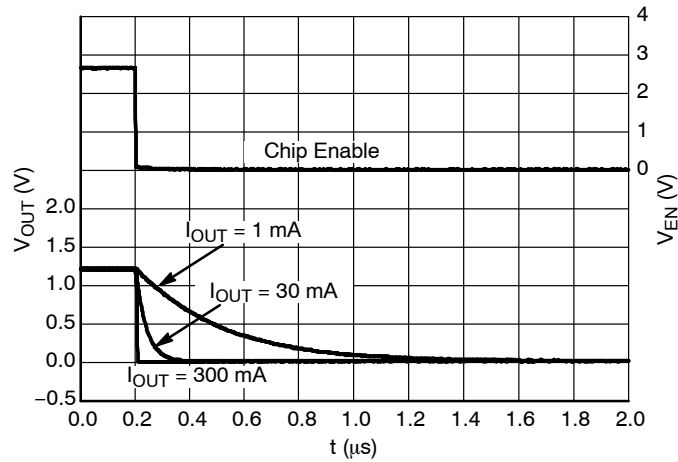


Figure 38. Shutdown, 1.2 V Version D,
 $V_{IN} = 2.6 \text{ V}$

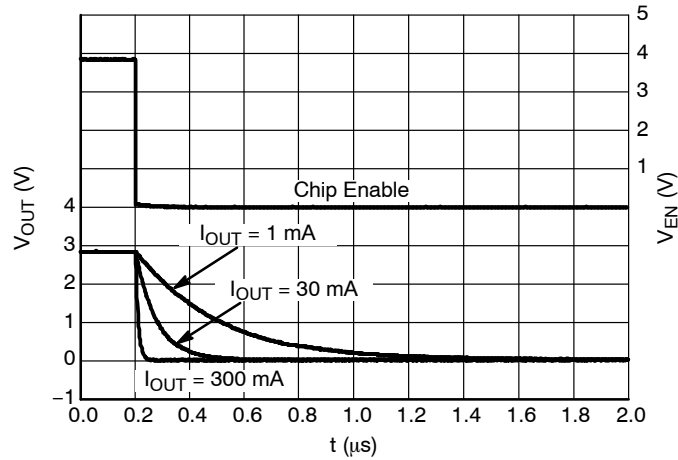


Figure 39. Shutdown, 2.8 V Version D,
 $V_{IN} = 3.8 \text{ V}$

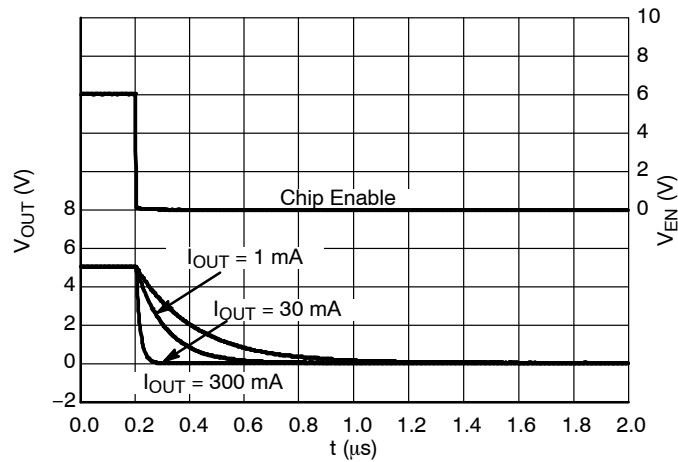


Figure 40. Shutdown, 5.0 V Version D,
 $V_{IN} = 6.0 \text{ V}$

APPLICATION INFORMATION

A typical application circuit for NCP4625 series is shown in Figure 41.

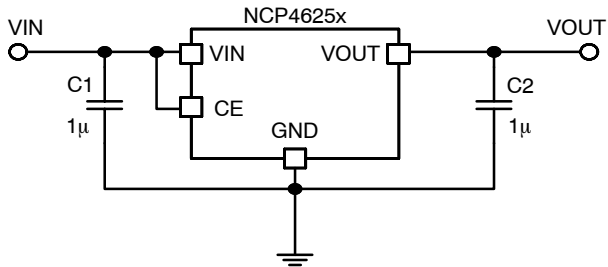


Figure 41. Typical Application Schematic

Input Decoupling Capacitor (C1)

A 1 μF ceramic input decoupling capacitor should be connected as close as possible to the input and ground pin of the NCP4625. Higher values and lower ESR improves line transient response.

Output Decoupling Capacitor (C2)

A 1 μF ceramic output decoupling capacitor is enough to achieve stable operation of the IC. If a tantalum capacitor is used, and its ESR is high, loop oscillation may result. The capacitors should be connected as close as possible to the output and ground pins. Larger values and lower ESR improves dynamic parameters.

Enable Operation

The enable pin CE may be used for turning the regulator on and off. The IC is switched on when a high level voltage is applied to the CE pin. The enable pin has an internal pull down current source. If the enable function is not needed connect CE pin to VIN.

Output Discharger

The D version includes a transistor between V_{OUT} and GND that is used for faster discharging of the output capacitor. This function is activated when the IC goes into disable mode.

Thermal

As a power across the IC increase, it might become necessary to provide some thermal relief. The maximum power dissipation supported by the device is dependent upon board design and layout. Mounting pad configuration on the PCB, the board material, and also the ambient temperature affect the rate of temperature increase for the part. When the device has good thermal conductivity through the PCB the junction temperature will be relatively low in high power dissipation applications.

PCB Layout

Make the VIN and GND line as large as practical. If their impedance is high, noise pickup or unstable operation may result. Connect capacitors C1 and C2 as close as possible to the IC, and make wiring as short as possible.

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ORDERING INFORMATION

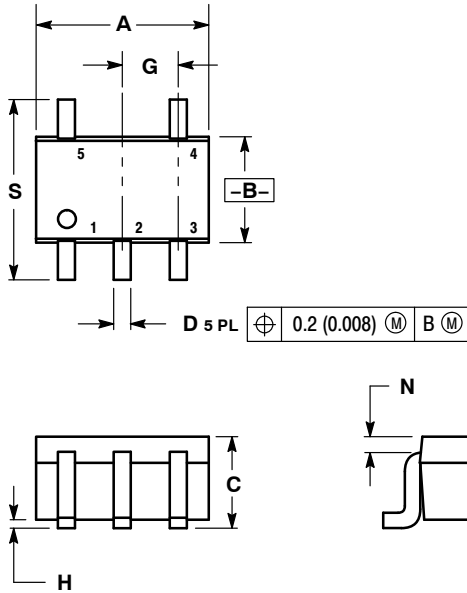
Device	Nominal Output Voltage	Description	Marking	Package	Shipping [†]
NCP4625DSN12T1G	1.2 V	Auto discharge	FBA	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625DSN18T1G	1.8 V	Auto discharge	FBH	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625DSN28T1G	2.8 V	Auto discharge	FBU	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625DSN30T1G	3.0 V	Auto discharge	FBX	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625DSN33T1G	3.3 V	Auto discharge	GBA	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625DSN50T1G	5.0 V	Auto discharge	GBT	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625HSN12T1G	1.2 V	Standard	FAA	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625HSN18T1G	1.8 V	Standard	FAH	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625HSN28T1G	2.8 V	Standard	FAU	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625HSN30T1G	3.0 V	Standard	FAX	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625HSN33T1G	3.3 V	Standard	GAA	SOT-23 (Pb-Free)	3000 / Tape & Reel
NCP4625HSN50T1G	5.0 V	Standard	GAT	SOT-23 (Pb-Free)	3000 / Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

NCP4625

PACKAGE DIMENSIONS

SC-88A (SC-70-5/SOT-353)
 CASE 419A-02
 ISSUE K



NOTES:

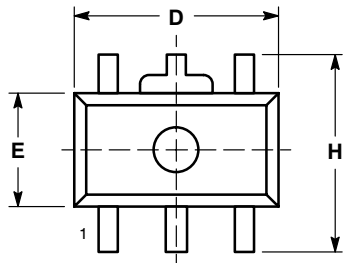
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. 419A-01 OBSOLETE. NEW STANDARD 419A-02.
4. DIMENSIONS A AND B DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.071	0.087	1.80	2.20
B	0.045	0.053	1.15	1.35
C	0.031	0.043	0.80	1.10
D	0.004	0.012	0.10	0.30
G	0.026 BSC		0.65 BSC	
H	---	0.004	---	0.10
J	0.004	0.010	0.10	0.25
K	0.004	0.012	0.10	0.30
N	0.008 REF		0.20 REF	
S	0.079	0.087	2.00	2.20

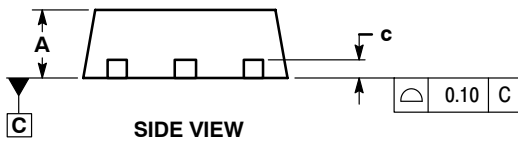
NCP4625

PACKAGE DIMENSIONS

SOT-89, 5 LEAD
CASE 528AB-01
ISSUE O



TOP VIEW

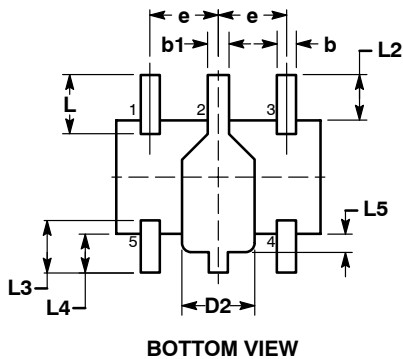


SIDE VIEW

NOTES:

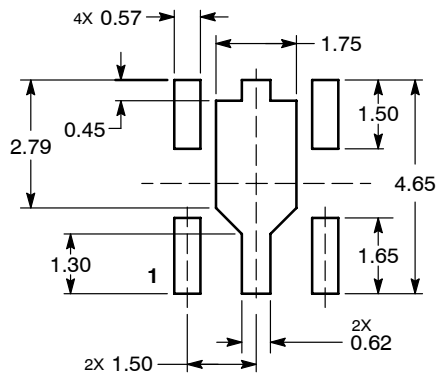
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. LEAD THICKNESS INCLUDES LEAD FINISH.
4. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH, PROTRUSIONS, OR GATE BURRS.
5. DIMENSIONS L, L2, L3, L4, L5, AND H ARE MEASURED AT DATUM PLANE C.

DIM	MILLIMETERS	
	MIN	MAX
A	1.40	1.60
b	0.32	0.52
b1	0.37	0.57
c	0.30	0.50
D	4.40	4.60
D2	1.40	1.80
E	2.40	2.60
e	1.40	1.60
H	4.25	4.45
L	1.10	1.50
L2	0.80	1.20
L3	0.95	1.35
L4	0.65	1.05
L5	0.20	0.60



BOTTOM VIEW

RECOMMENDED MOUNTING FOOTPRINT*



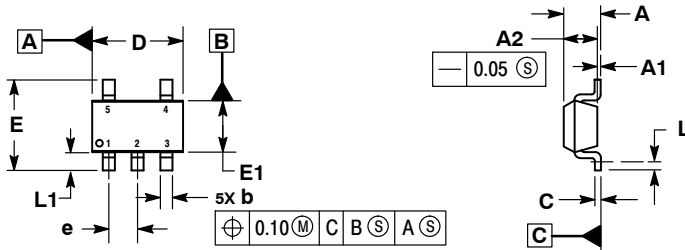
DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCP4625

PACKAGE DIMENSIONS

SOT-23 5-LEAD CASE 1212-01 ISSUE A

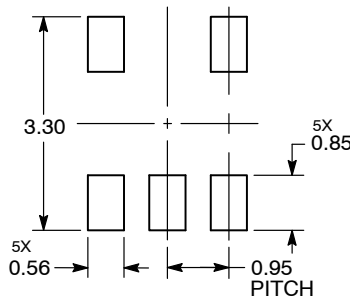


NOTES:

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSIONS: MILLIMETERS.
3. DATUM C IS THE SEATING PLANE.


MILLIMETERS		
DIM	MIN	MAX
A	---	1.45
A1	0.00	0.10
A2	1.00	1.30
b	0.30	0.50
c	0.10	0.25
D	2.70	3.10
E	2.50	3.10
E1	1.50	1.80
e	0.95 BSC	
L	0.20	---
L1	0.45	0.75

RECOMMENDED SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

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