



**THE DATASHEET OF  
IRL1104PBF**



# IRL1104PbF

HEXFET® Power MOSFET

- Logic-Level Gate Drive
- Advanced Process Technology
- Ultra Low On-Resistance
- Dynamic dv/dt Rating
- 175°C Operating Temperature
- Fast Switching
- Fully Avalanche Rated
- Lead-Free

## Description

Fifth Generation HEXFET® power MOSFETs from International Rectifier utilize advanced processing techniques to achieve the lowest possible on-resistance per silicon area. This benefit, combined with the fast switching speed and ruggedized device design that HEXFET® power MOSFETs are well known for, provides the designer with an extremely efficient device for use in a wide variety of applications.

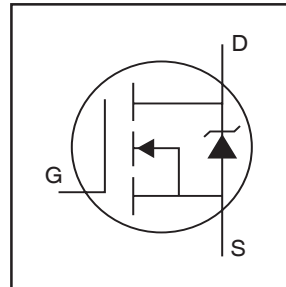
The TO-220 package is universally preferred for all commercial-industrial applications at power dissipation levels to approximately 50 watts. The low thermal resistance and low package cost of the TO-220 contribute to its wide acceptance throughout the industry.

## Absolute Maximum Ratings

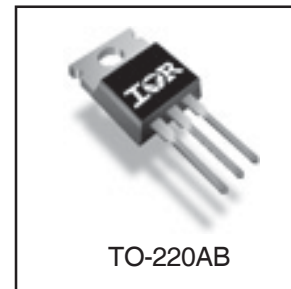
	Parameter	Max.	Units
$I_D$ @ $T_C = 25^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	104 <sup>⑤</sup>	A
$I_D$ @ $T_C = 100^\circ\text{C}$	Continuous Drain Current, $V_{GS}$ @ 10V	74	
$I_{DM}$	Pulsed Drain Current <sup>①</sup>	416	
$P_D$ @ $T_C = 25^\circ\text{C}$	Power Dissipation	167	W
	Linear Derating Factor	1.1	W/°C
$V_{GS}$	Gate-to-Source Voltage	±16	V
$E_{AS}$	Single Pulse Avalanche Energy <sup>②</sup>	340	mJ
$I_{AR}$	Avalanche Current <sup>③</sup>	62	A
$E_{AR}$	Repetitive Avalanche Energy <sup>④</sup>	17	mJ
dv/dt	Peak Diode Recovery dv/dt <sup>③</sup>	5.0	V/ns
$T_J$ $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to +175	°C
	Soldering Temperature, for 10 seconds	300 (1.6mm from case)	
	Mounting torque, 6-32 or M3 screw.	10 lbf•in (1.1N•m)	

## Thermal Resistance

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case	—	—	0.9	°C/W
$R_{\theta CS}$	Case-to-Sink, Flat, Greased Surface	—	0.50	—	
$R_{\theta JA}$	Junction-to-Ambient	—	—	62	

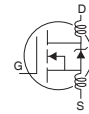


$V_{DSS} = 40\text{V}$
$R_{DS(on)} = 0.008\Omega$
$I_D = 104\text{A}$ <sup>⑤</sup>



Electrical Characteristics @ T<sub>J</sub> = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
V <sub>(BR)DSS</sub>	Drain-to-Source Breakdown Voltage	40	—	—	V	V <sub>GS</sub> = 0V, I <sub>D</sub> = 250μA
ΔV <sub>(BR)DSS/ΔT<sub>J</sub></sub>	Breakdown Voltage Temp. Coefficient	—	0.04	—	V/°C	Reference to 25°C, I <sub>D</sub> = 1mA
R <sub>DS(on)</sub>	Static Drain-to-Source On-Resis-	—	—	0.008	Ω	V <sub>GS</sub> = 10V, I <sub>D</sub> = 62A ④
		—	—	0.012		V <sub>GS</sub> = 4.5V, I <sub>D</sub> = 52A ④
V <sub>GS(th)</sub>	Gate Threshold Voltage	1.0	—	—	V	V <sub>DS</sub> = V <sub>GS</sub> , I <sub>D</sub> = 250μA
g <sub>fs</sub>	Forward Transconductance	53	—	—	S	V <sub>DS</sub> = 25V, I <sub>D</sub> = 62A
I <sub>DSS</sub>	Drain-to-Source Leakage Current	—	—	25	μA	V <sub>DS</sub> = 40V, V <sub>GS</sub> = 0V
		—	—	250		V <sub>DS</sub> = 32V, V <sub>GS</sub> = 0V, T <sub>J</sub> = 150°C
I <sub>GSS</sub>	Gate-to-Source Forward Leakage	—	—	100	nA	V <sub>GS</sub> = 16V
	Gate-to-Source Reverse Leakage	—	—	-100		V <sub>GS</sub> = -16V
Q <sub>g</sub>	Total Gate Charge	—	—	68	nC	I <sub>D</sub> = 62A
Q <sub>gs</sub>	Gate-to-Source Charge	—	—	24		V <sub>DS</sub> = 32V
Q <sub>gd</sub>	Gate-to-Drain ("Miller") Charge	—	—	33		V <sub>GS</sub> = 4.5V, See Fig. 6 and 13 ④
t <sub>d(on)</sub>	Turn-On Delay Time	—	18	—	ns	V <sub>DD</sub> = 20V
t <sub>r</sub>	Rise Time	—	257	—		I <sub>D</sub> = 62A
t <sub>d(off)</sub>	Turn-Off Delay Time	—	32	—		R <sub>G</sub> = 3.6Ω, V <sub>GS</sub> = 4.5V
t <sub>f</sub>	Fall Time	—	64	—		R <sub>D</sub> = 0.4Ω, See Fig. 10 ④
L <sub>D</sub>	Internal Drain Inductance	—	4.5	—	nH	Between lead, 6mm (0.25in.) from package and center of die contact
L <sub>S</sub>	Internal Source Inductance	—	7.5	—		
C <sub>iss</sub>	Input Capacitance	—	3445	—	pF	V <sub>GS</sub> = 0V
C <sub>oss</sub>	Output Capacitance	—	1065	—		V <sub>DS</sub> = 25V
C <sub>rss</sub>	Reverse Transfer Capacitance	—	270	—		f = 1.0MHz, See Fig. 5



Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I <sub>S</sub>	Continuous Source Current (Body Diode)	—	—	104⑤	A	MOSFET symbol showing the integral reverse p-n junction diode.
I <sub>SM</sub>	Pulsed Source Current (Body Diode) ①	—	—	416		
V <sub>SD</sub>	Diode Forward Voltage	—	—	1.3	V	T <sub>J</sub> = 25°C, I <sub>S</sub> = 62A, V <sub>GS</sub> = 0V ④
t <sub>rr</sub>	Reverse Recovery Time	—	84	126	ns	T <sub>J</sub> = 25°C, I <sub>F</sub> = 62A
Q <sub>rr</sub>	Reverse Recovery Charge	—	223	335	nC	di/dt = 100A/μs ④
t <sub>on</sub>	Forward Turn-On Time	Intrinsic turn-on time is negligible (turn-on is dominated by L <sub>S</sub> +L <sub>D</sub> )				

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature. ( See fig. 11 )
- ② V<sub>DD</sub> = 15V, starting T<sub>J</sub> = 25°C, L = 0.18mH  
R<sub>G</sub> = 25Ω, I<sub>AS</sub> = 62A. (See Figure 12)
- ③ I<sub>SD</sub> ≤ 62A, di/dt ≤ 217A/μs, V<sub>DD</sub> ≤ V<sub>(BR)DSS</sub>.  
T<sub>J</sub> ≤ 175°C

④ Pulse width ≤ 300μs; duty cycle ≤ 2%.

⑤ Calculated continuous current based on maximum allowable junction temperature; for recommended current-handling of the package refer to Design Tip # 93-4

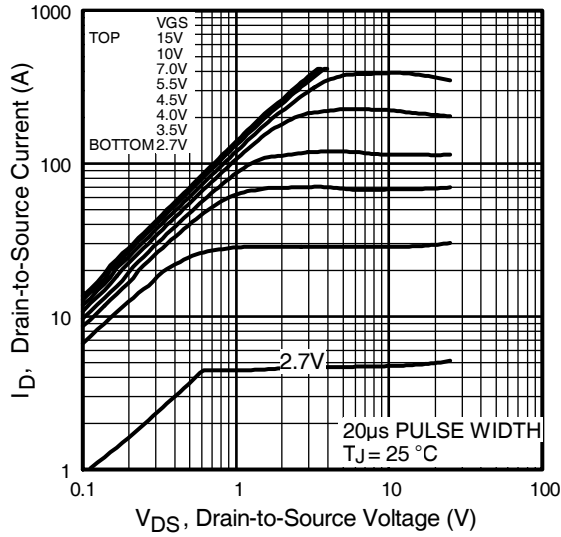


Fig 1. Typical Output Characteristics

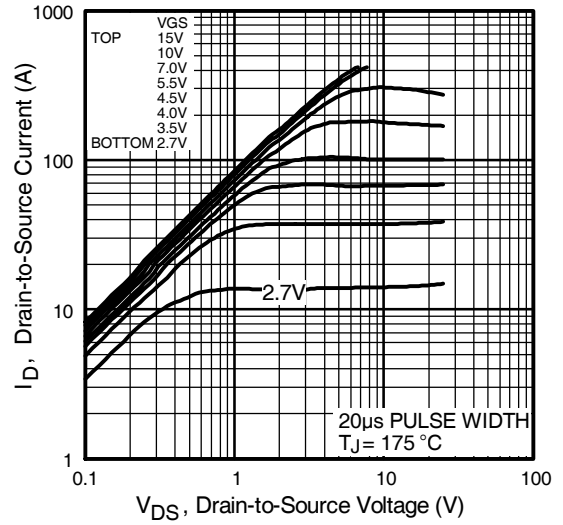


Fig 2. Typical Output Characteristics

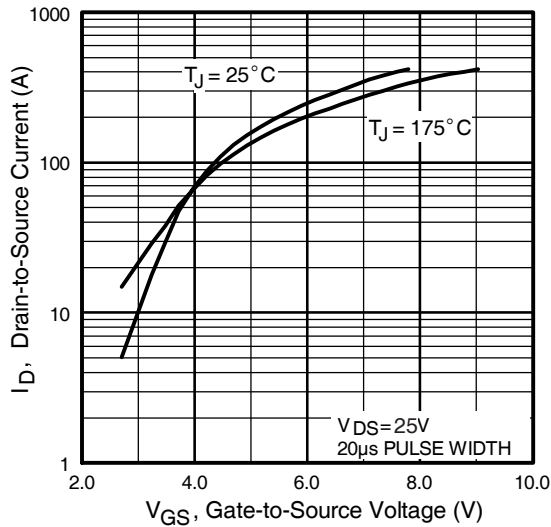


Fig 3. Typical Transfer Characteristics

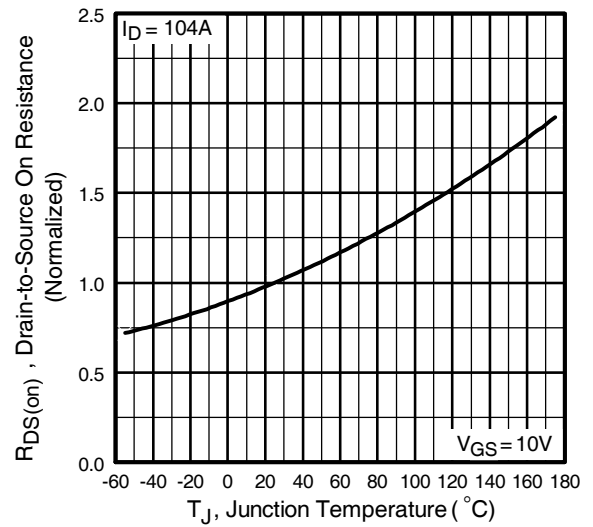


Fig 4. Normalized On-Resistance Vs. Temperature

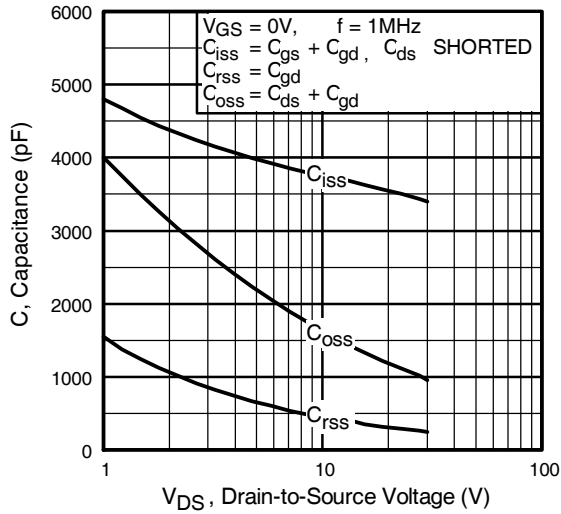


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

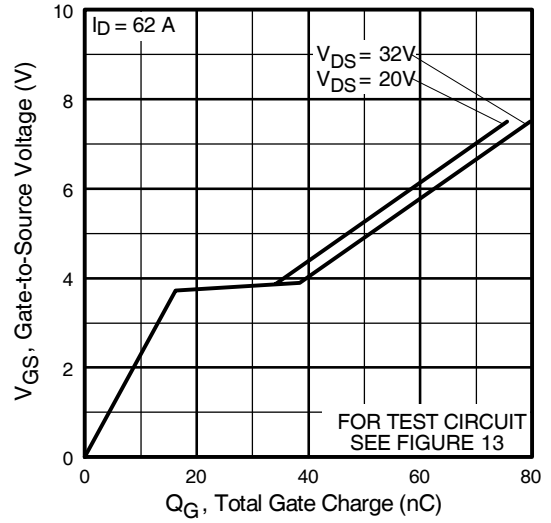


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

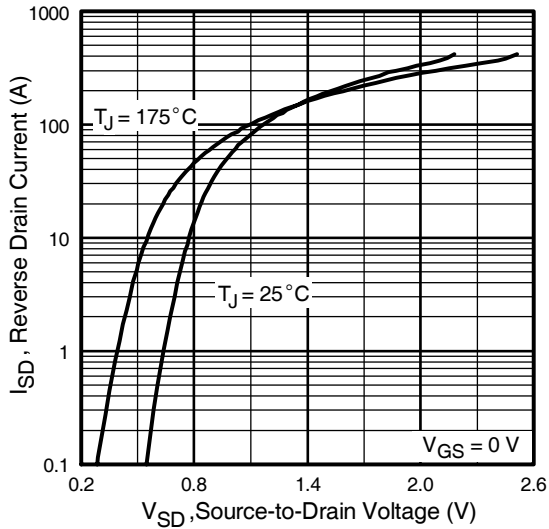


Fig 7. Typical Source-Drain Diode Forward Voltage

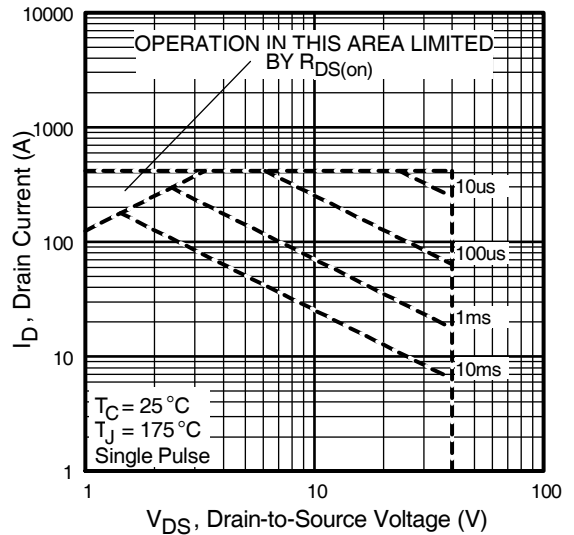


Fig 8. Maximum Safe Operating Area

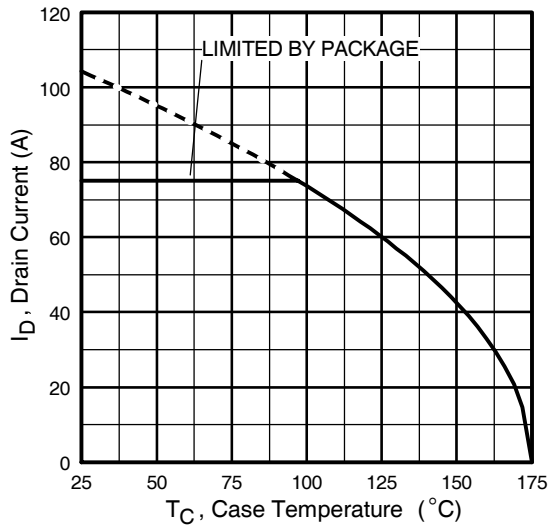


Fig 9. Maximum Drain Current Vs. Case Temperature

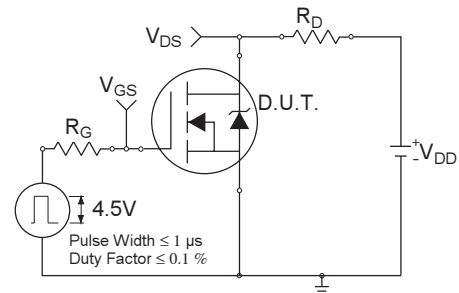


Fig 10a. Switching Time Test Circuit

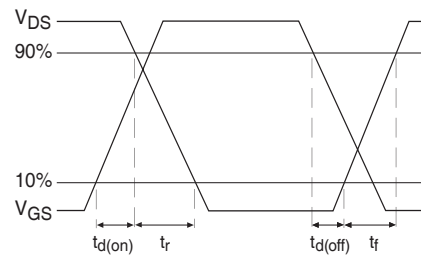


Fig 10b. Switching Time Waveforms

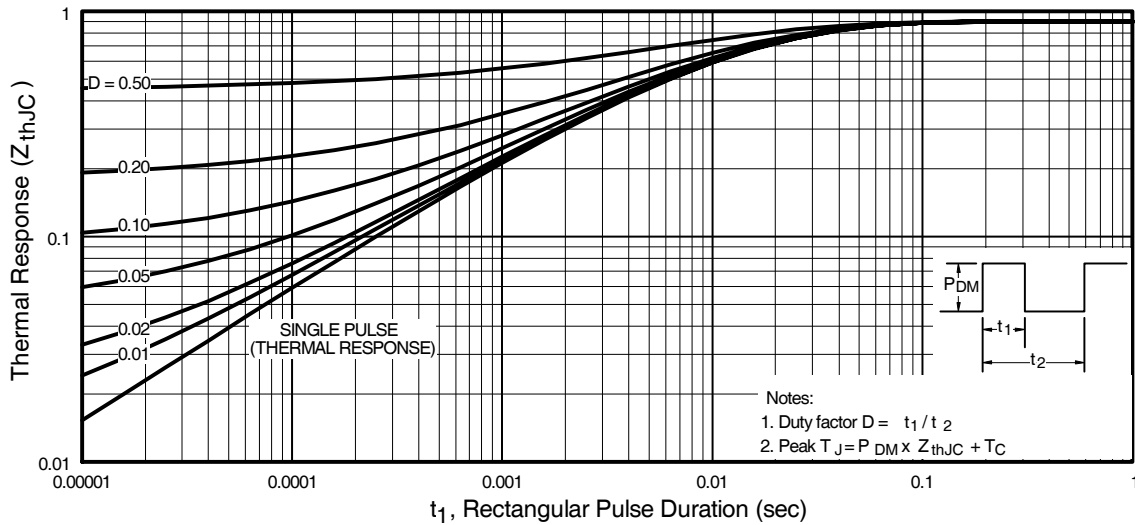


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

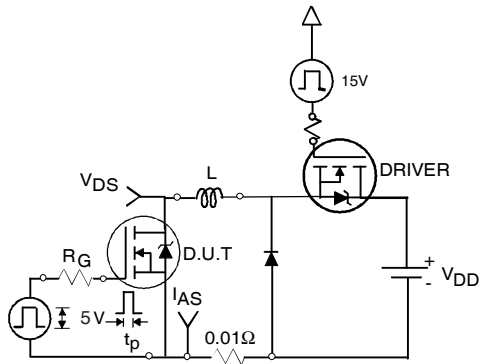


Fig 12a. Unclamped Inductive Test Circuit

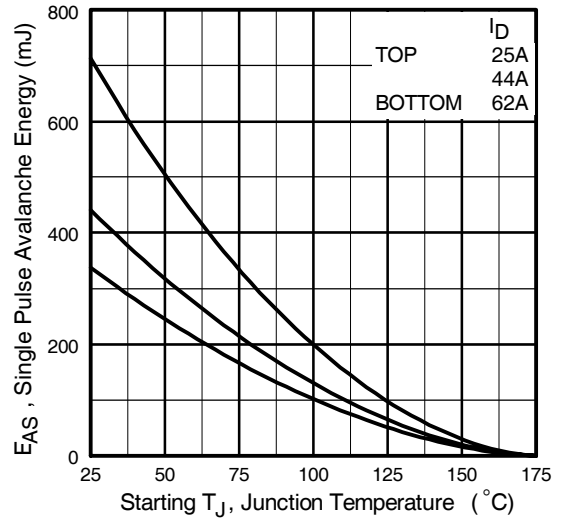


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

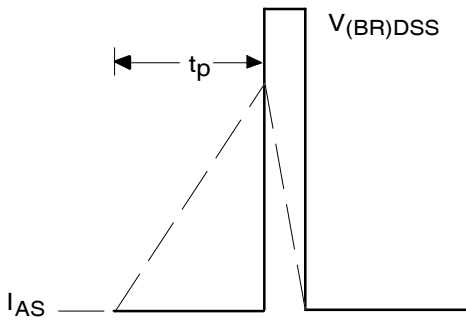


Fig 12b. Unclamped Inductive Waveforms

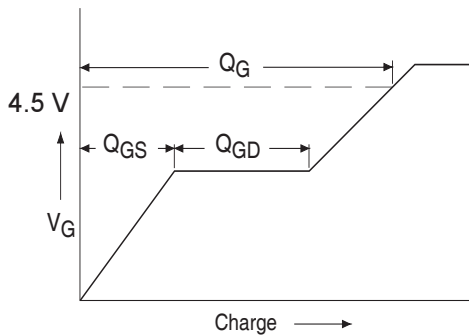


Fig 13a. Basic Gate Charge Waveform

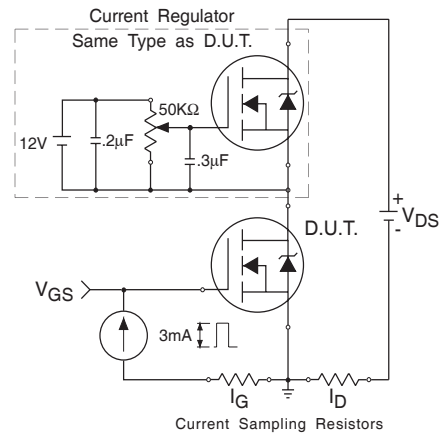
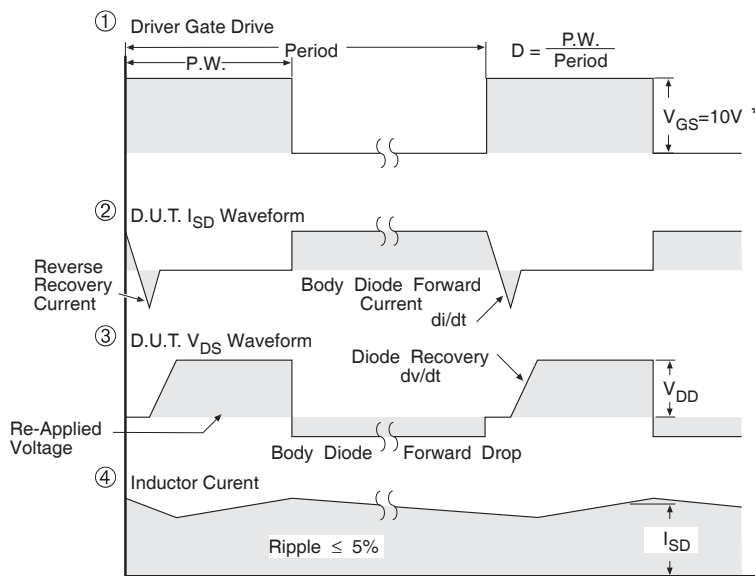
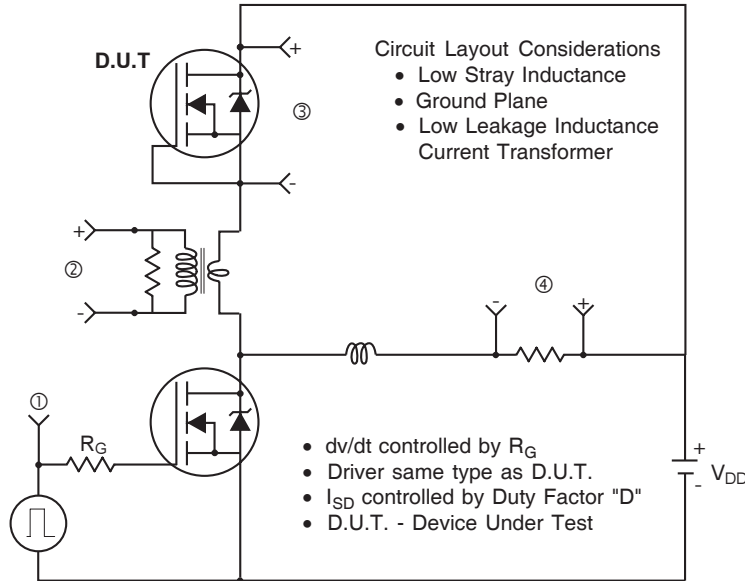


Fig 13b. Gate Charge Test Circuit

**Peak Diode Recovery dv/dt Test Circuit**

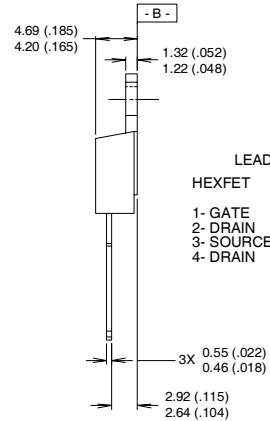
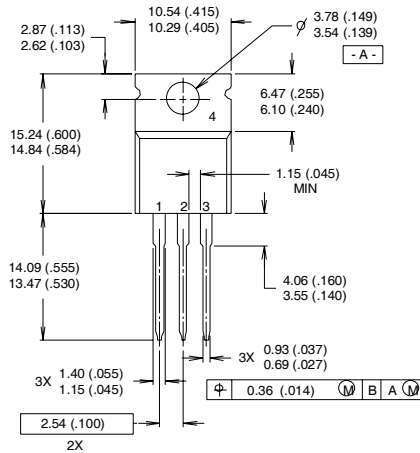


\*  $V_{GS} = 5V$  for Logic Level Devices

**Fig 14.** For N-Channel HEXFET® power MOSFETs

### TO-220AB Package Outline

Dimensions are shown in millimeters (inches)



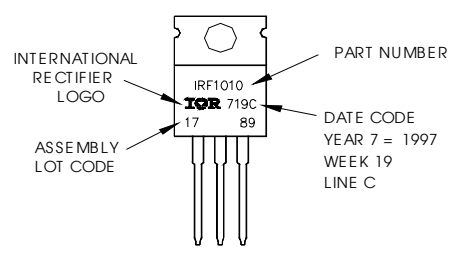
**LEAD ASSIGNMENTS**

HEXFET	IGBTs, CoPACK
1- GATE	1- GATE
2- DRAIN	2- COLLECTOR
3- SOURCE	3- EMITTER
4- DRAIN	4- COLLECTOR

- NOTES:
- 1 DIMENSIONING & TOLERANCING PER ANSI Y14.5M, 1982.
  - 2 CONTROLLING DIMENSION : INCH
  - 3 OUTLINE CONFORMS TO JEDEC OUTLINE TO-220AB.
  - 4 HEATSINK & LEAD MEASUREMENTS DO NOT INCLUDE BURRS.

### TO-220AB Part Marking Information

EXAMPLE: THIS IS AN IRF1010  
 LOT CODE 1789  
 ASSEMBLED ON WW 19, 1997  
 IN THE ASSEMBLY LINE "C"  
**Note:** "P" in assembly line position indicates "Lead-Free"



Data and specifications subject to change without notice.



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Note: For the most current drawings please refer to the IR website at:  
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