



**THE DATASHEET OF  
AD5228BUJZ10**



### FEATURES

- 32-position digital potentiometer
- 10 kΩ, 50 kΩ, 100 kΩ end-to-end terminal resistance
- Simple manual up/down control
- Self-contained, requires only 2 pushbutton tactile switches
- Built-in adaptive debouncer
- Discrete step-up/step-down control
- Autoscan up/down control with 4 steps per second
- Pin-selectable zero-scale/midscale preset
- Low potentiometer mode tempco, 5 ppm/°C
- Low rheostat mode tempco, 35 ppm/°C
- Digital control compatible
- Ultralow power,  $I_{DD} = 0.4 \mu\text{A}$  typ and  $3 \mu\text{A}$  max
- Low operating voltage, 2.7 V to 5.5 V
- Temperature range,  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$
- Compact thin SOT-23-8 (2.9 mm × 3 mm) Pb-free package

### APPLICATIONS

- Mechanical potentiometer and trimmer replacements
- LCD backlight, contrast, and brightness controls
- Digital volume control
- Portable device-level adjustments
- Electronic front panel-level controls
- Programmable power supply

### GENERAL DESCRIPTION

The AD5228 is Analog Devices' latest 32-step-up/step-down control digital potentiometer emulating mechanical potentiometer operation<sup>1</sup>. Its simple up/down control interface allows manual control with just two external pushbutton tactile switches. The AD5228 is designed with a built-in adaptive debouncer that ignores invalid bounces due to contact bounce commonly found in mechanical switches. The debouncer is adaptive, accommodating a variety of pushbutton tactile switches that generally have less than 10 ms of bounce time during contact closures. When choosing the switch, the user should consult the timing specification of the switch to ensure its suitability in an AD5228 application.

<sup>1</sup>The terms *digital potentiometer* and *RDAC* are used interchangeably.

### FUNCTIONAL BLOCK DIAGRAM

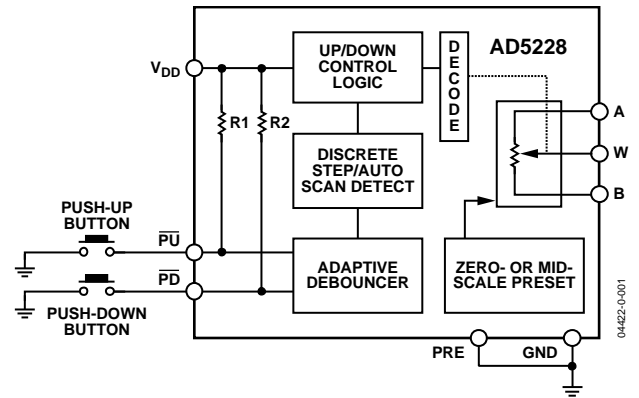


Figure 1.

The AD5228 can increment or decrement the resistance in discrete steps or in autoscan mode. When the  $\overline{\text{PU}}$  or  $\overline{\text{PD}}$  button is pressed briefly (no longer than 0.6 s), the resistance of the AD5228 changes by one step. When the  $\overline{\text{PU}}$  or  $\overline{\text{PD}}$  button is held continuously for more than a second, the device activates the autoscan mode and changes four resistance steps per second.

The AD5228 can also be controlled digitally; its up/down features simplify microcontroller usage. The AD5228 is available in a compact thin SOT-23-8 (TSOT-8) package. The part is guaranteed to operate over the temperature range of  $-40^\circ\text{C}$  to  $+105^\circ\text{C}$ .

The AD5228's simple interface, small footprint, and very low cost enable it to replace mechanical potentiometers and trimmers with typically 3× improved resolution, solid-state reliability, and faster adjustment, resulting in considerable cost saving in end users' systems.

Users who consider EEMEM potentiometers should refer to the recommendations in the Applications section.

Table 1. Truth Table

$\overline{\text{PU}}$	$\overline{\text{PD}}$	Operation <sup>1</sup>
0	0	$R_{WB}$ Decrement
0	1	$R_{WB}$ Increment
1	0	$R_{WB}$ Decrement
1	1	$R_{WB}$ Does Not Change

<sup>1</sup> $R_{WA}$  increments if  $R_{WB}$  decrements and vice versa.

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## REVISION HISTORY

### 6/15—Rev. A to Rev. B

Changes to Features Section and General Description Section....	1
Changes to Ordering Guide .....	18

### 4/09—Rev. 0 to Rev. A

Changes to Table 2.....	3
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### 4/04—Revision 0: Initial Version

## ELECTRICAL CHARACTERISTICS

10 k $\Omega$ , 50 k $\Omega$ , 100 k $\Omega$  versions:  $V_{DD} = 3\text{ V} \pm 10\%$  or  $5\text{ V} \pm 10\%$ ,  $V_A = V_{DD}$ ,  $V_B = 0\text{ V}$ ,  $-40^\circ\text{C} < T_A < +105^\circ\text{C}$ , unless otherwise noted.

Table 2.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
<b>DC CHARACTERISTICS, RHEOSTAT MODE</b>						
Resistor Differential Nonlinearity <sup>2</sup>	R-DNL	$R_{WB}$ , A terminal = no connect	-0.5	$\pm 0.05$	+0.5	LSB
Resistor Integral Nonlinearity <sup>2</sup>	R-INL	$R_{WB}$ , A terminal = no connect	-0.5	$\pm 0.1$	+0.5	LSB
Nominal Resistor Tolerance <sup>3</sup>	$\Delta R_{AB}/R_{AB}$		-20		+20	%
Resistance Temperature Coefficient	$(\Delta R_{AB}/R_{AB}) \times 10^4/\Delta T$			35		ppm/ $^\circ\text{C}$
Wiper Resistance	$R_W$	$V_{DD} = 2.7\text{ V}$ $V_{DD} = 2.8\text{ V to } 5.5\text{ V}$		100	250	$\Omega$
				50	200	$\Omega$
<b>DC CHARACTERISTICS, POTENTIOMETER DIVIDER MODE</b> (Specifications apply to all RDACs)						
Resolution	N				5	Bits
Integral Nonlinearity <sup>3</sup>	INL		-0.5	$\pm 0.05$	+0.5	LSB
Differential Nonlinearity <sup>3,5</sup>	DNL		-0.5	$\pm 0.05$	+0.5	LSB
Voltage Divider Temperature Coefficient	$(\Delta V_W/V_W) \times 10^4/\Delta T$	Midscale		5		ppm/ $^\circ\text{C}$
Full-Scale Error	$V_{WFSE}$	$\geq +15$ steps from midscale	-1.2	-0.5	0	LSB
Zero-Scale Error	$V_{WZSE}$	$\leq -16$ steps from midscale	0	0.3	0.6	LSB
<b>RESISTOR TERMINALS</b>						
Voltage Range <sup>6</sup>	$V_{A,B,W}$	With respect to GND	0		$V_{DD}$	V
Capacitance <sup>4</sup> A, B	$C_{A,B}$	$f = 1\text{ MHz}$ , measured to GND		140		pF
Capacitance <sup>4</sup> W	$C_W$	$f = 1\text{ MHz}$ , measured to GND		150		pF
Common-Mode Leakage	$I_{CM}$	$V_A = V_B = V_W$		1		nA
<b><math>\overline{\text{PU}}</math>, <math>\overline{\text{PD}}</math> INPUTS</b>						
Input High	$V_{IH}$	$V_{DD} = 5\text{ V}$	2.4		5.5	V
Input Low	$V_{IL}$	$V_{DD} = 5\text{ V}$	0		0.8	V
Input Current	$I_i$	$V_{IN} = 0\text{ V or } 5\text{ V}$			$\pm 1$	$\mu\text{A}$
Input Capacitance <sup>4</sup>	$C_i$			5		pF
<b>POWER SUPPLIES</b>						
Power Supply Range	$V_{DD}$	$V_{DD} = 5\text{ V}$ , $\overline{\text{PU}} = \overline{\text{PD}} = V_{DD}$	2.7		5.5	V
Supply Standby Current	$I_{DD\_STBY}$			0.4	3	$\mu\text{A}$
Supply Active Current <sup>7</sup>	$I_{DD\_ACT}$	$V_{DD} = 5\text{ V}$ , $\overline{\text{PU}}$ or $\overline{\text{PD}} = 0\text{ V}$		50	110	$\mu\text{A}$
Power Dissipation <sup>7,8</sup>	$P_{DISS}$	$V_{DD} = 5\text{ V}$			17	$\mu\text{W}$
Power Supply Sensitivity	PSSR	$V_{DD} = 5\text{ V} \pm 10\%$		0.01	0.05	%/%

Footnotes on next page.

Parameter	Symbol	Conditions	Min	Typ <sup>1</sup>	Max	Unit
DYNAMIC CHARACTERISTICS <sup>4, 9, 10, 11</sup>						
Built-in Debounce and Settling Time <sup>12</sup>	$t_{DB}$		6			ms
$\overline{PU}$ Low Pulse Width	$t_{PU}$		12			ms
$\overline{PD}$ Low Pulse Width	$t_{PD}$		12			ms
$\overline{PU}$ High Repetitive Pulse Width	$t_{PU\_REP}$		1			$\mu$ s
$\overline{PD}$ High Repetitive Pulse Width	$t_{PD\_REP}$		1			$\mu$ s
Autoscan Start Time	$t_{AS\_START}$	$\overline{PU}$ or $\overline{PD} = 0$ V	0.6	0.8	1.2	s
Autoscan Time	$t_{AS}$	$\overline{PU}$ or $\overline{PD} = 0$ V	0.16	0.25	0.38	s
Bandwidth –3 dB	BW_10	$R_{AB} = 10$ k $\Omega$ , midscale		460		kHz
	BW_50	$R_{AB} = 50$ k $\Omega$ , midscale		100		kHz
	BW_100	$R_{AB} = 100$ k $\Omega$ , midscale		50		kHz
Total Harmonic Distortion	THD	$V_A = 1$ V rms, $R_{AB} = 10$ k $\Omega$ , $V_B = 0$ V dc, $f = 1$ kHz		0.05		%
Resistor Noise Voltage	$e_{N\_WB}$	$R_{WB} = 5$ k $\Omega$ , $f = 1$ kHz		14		nV/ $\sqrt$ Hz

<sup>1</sup> Typical values represent average readings at 25°C,  $V_{DD} = 5$  V.

<sup>2</sup> Resistor position nonlinearity error, R-INL, is the deviation from an ideal value measured between the maximum resistance and the minimum resistance wiper positions. R-DNL measures the relative step change from ideal between successive tap positions. Parts are guaranteed monotonic.

<sup>3</sup> INL and DNL are measured at  $V_W$  with the RDAC configured as a potentiometer divider similar to a voltage output D/A converter.  $V_A = V_{DD}$  and  $V_B = 0$  V.

<sup>4</sup> Guaranteed by design and not subject to production test.

<sup>5</sup> DNL specification limits of  $\pm 1$  LSB maximum are guaranteed monotonic operating conditions.

<sup>6</sup> Resistor Terminals A, B, and W have no limitations on polarity with respect to each other.

<sup>7</sup>  $\overline{PU}$  and  $\overline{PD}$  have 100 k $\Omega$  internal pull-up resistors,  $I_{DD\_ACT} = V_{DD}/100$  k $\Omega + I_{OSC}$  (internal oscillator operating current) when  $\overline{PU}$  or  $\overline{PD}$  is connected to ground.

<sup>8</sup>  $P_{DISS}$  is calculated based on  $I_{DD\_STBY} \times V_{DD}$  only.  $I_{DD\_ACT}$  duration should be short. Users should not hold  $\overline{PU}$  or  $\overline{PD}$  pin to ground longer than necessary to elevate power dissipation.

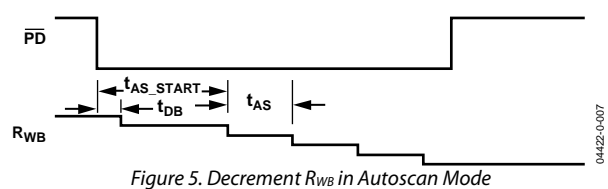
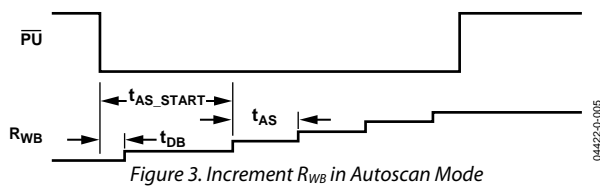
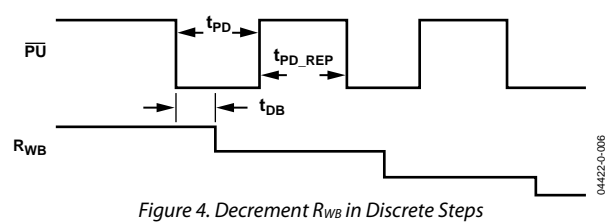
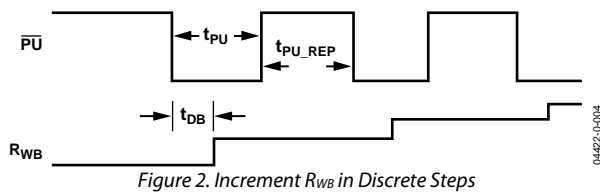
<sup>9</sup> Bandwidth, noise, and settling time are dependent on the terminal resistance value chosen. The lowest R value results in the fastest settling time and highest bandwidth. The highest R value results in the minimum overall power consumption.

<sup>10</sup> All dynamic characteristics use  $V_{DD} = 5$  V.

<sup>11</sup> Note that all input control voltages are specified with  $t_R = t_F = 1$  ns (10% to 90% of  $V_{DD}$ ) and timed from a voltage level of 1.6 V. Switching characteristics are measured using  $V_{DD} = 5$  V.

<sup>12</sup> The debouncer keeps monitoring the logic-low level once  $\overline{PU}$  is connected to ground. Once the signal lasts longer than 11 ms, the debouncer assumes the last bounce is met and allows the AD5228 to increment by one step. If the  $\overline{PU}$  signal remains at low and reaches  $t_{AS\_START}$ , the AD5228 increments again, see Figure 7. Similar characteristics apply to  $\overline{PD}$  operation.

## INTERFACE TIMING DIAGRAMS



## ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
V <sub>DD</sub> to GND	−0.3 V, +7 V
V <sub>A</sub> , V <sub>B</sub> , V <sub>W</sub> to GND	0 V, V <sub>DD</sub>
$\overline{PU}$ , $\overline{PD}$ , PRE Voltage to GND	0 V, V <sub>DD</sub>
Maximum Current	
I <sub>WB</sub> , I <sub>WA</sub> Pulsed	±20 mA
I <sub>WB</sub> Continuous (R <sub>WB</sub> ≤ 5 kΩ, A open) <sup>1</sup>	±1 mA
I <sub>WA</sub> Continuous (R <sub>WA</sub> ≤ 5 kΩ, B open) <sup>1</sup>	±1 mA
I <sub>AB</sub> Continuous (R <sub>AB</sub> = 10 kΩ/50 kΩ/100 kΩ) <sup>1</sup>	±500 μA/±100 μA/ ±50 μA
Operating Temperature Range	−40°C to +105°C
Maximum Junction Temperature (T <sub>Jmax</sub> )	150°C
Storage Temperature	−65°C to +150°C
Lead Temperature (Soldering, 10 s – 30 s)	245°C
Thermal Resistance <sup>2</sup> θ <sub>JA</sub>	230°C/W

<sup>1</sup> Maximum terminal current is bounded by the maximum applied voltage across any two of the A, B, and W terminals at a given resistance, the maximum current handling of the switches, and the maximum power dissipation of the package. V<sub>DD</sub> = 5 V.

<sup>2</sup> Package power dissipation = (T<sub>Jmax</sub> − T<sub>A</sub>) / θ<sub>JA</sub>.

Stresses at or above those listed under Absolute Maximum Ratings may cause permanent damage to the product. This is a stress rating only; functional operation of the product at these or any other conditions above those indicated in the operational section of this specification is not implied. Operation beyond the maximum operating conditions for extended periods may affect product reliability.

### ESD CAUTION



**ESD (electrostatic discharge) sensitive device.** Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

## PIN CONFIGURATION AND FUNCTION DESCRIPTIONS

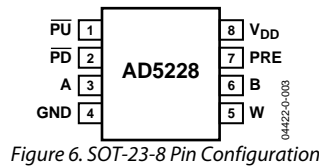


Figure 6. SOT-23-8 Pin Configuration

Table 4. Pin Function Descriptions

Pin No.	Mnemonic	Description
1	$\overline{\text{PU}}$	Push-Up Pin. Connect to the external pushbutton. Active low. A 100 k $\Omega$ pull-up resistor is connected to $V_{\text{DD}}$ .
2	$\overline{\text{PD}}$	Push-Down Pin. Connect to the external pushbutton. Active low. A 100 k $\Omega$ pull-up resistor is connected to $V_{\text{DD}}$ .
3	A	Resistor Terminal A. $\text{GND} \leq V_{\text{A}} \leq V_{\text{DD}}$ .
4	GND	Common Ground.
5	W	Wiper Terminal W. $\text{GND} \leq V_{\text{W}} \leq V_{\text{DD}}$ .
6	B	Resistor Terminal B. $\text{GND} \leq V_{\text{B}} \leq V_{\text{DD}}$ .
7	PRE	Power-On Preset. Output = midscale if PRE = GND; output = zero scale if PRE = $V_{\text{DD}}$ . Do not let the PRE pin float. No pull-up resistor is needed.
8	$V_{\text{DD}}$	Positive Power Supply, 2.7 V to 5.5 V.

### TYPICAL PERFORMANCE CHARACTERISTICS

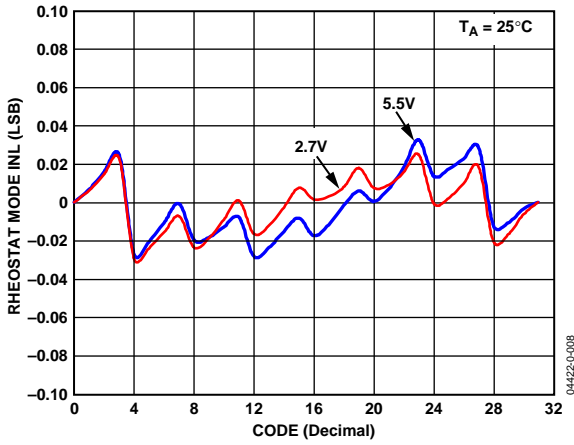


Figure 7. R-INL vs. Code vs. Supply Voltages

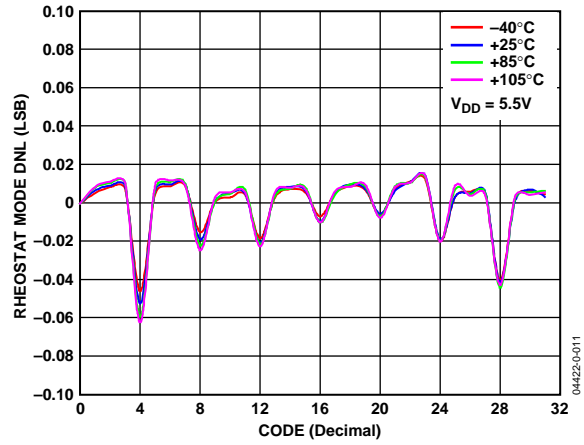


Figure 10. R-DNL vs. Code vs. Temperature,  $V_{DD} = 5V$

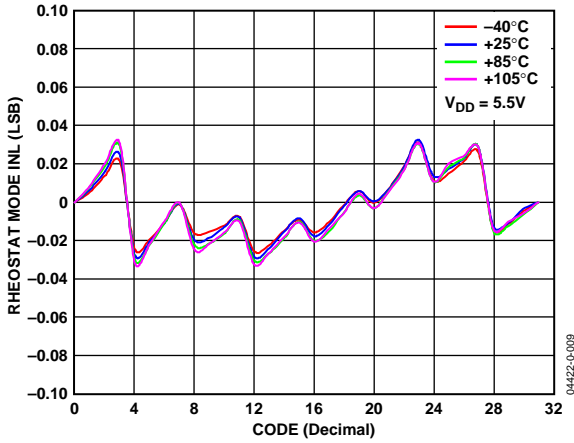


Figure 8. R-INL vs. Code vs. Temperature,  $V_{DD} = 5V$

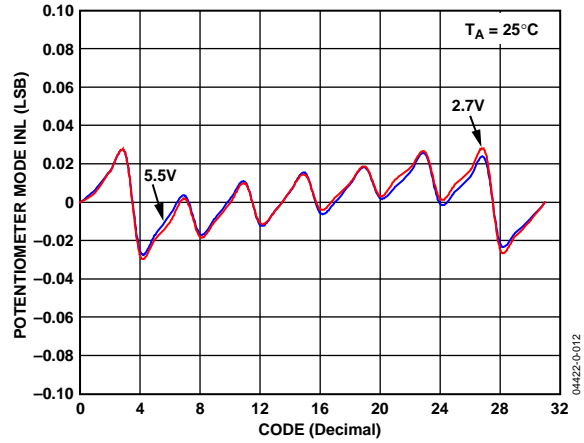


Figure 11. INL vs. Code vs. Supply Voltages

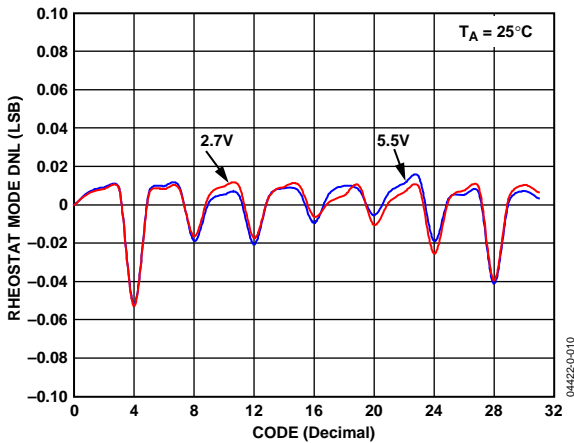


Figure 9. R-DNL vs. Code vs. Supply Voltages

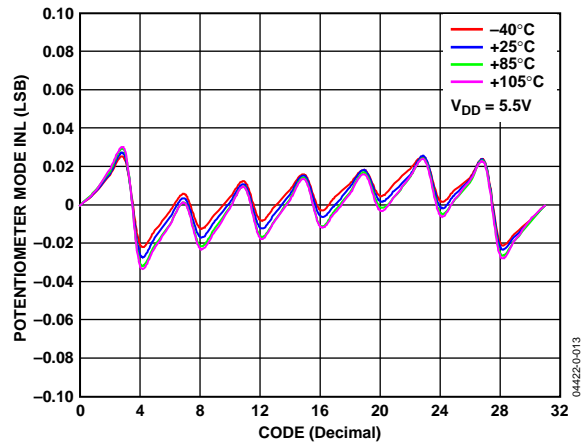


Figure 12. INL vs. Code,  $V_{DD} = 5V$

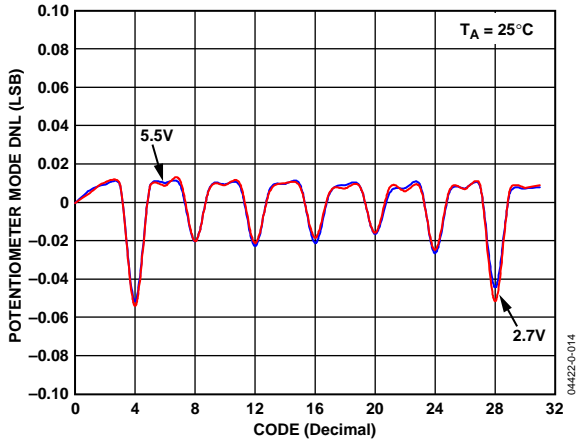


Figure 13. DNL vs. Code vs. Supply Voltages

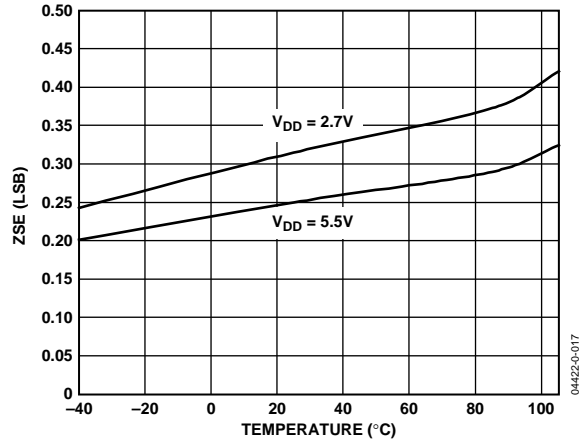


Figure 16. Zero-Scale Error vs. Temperature

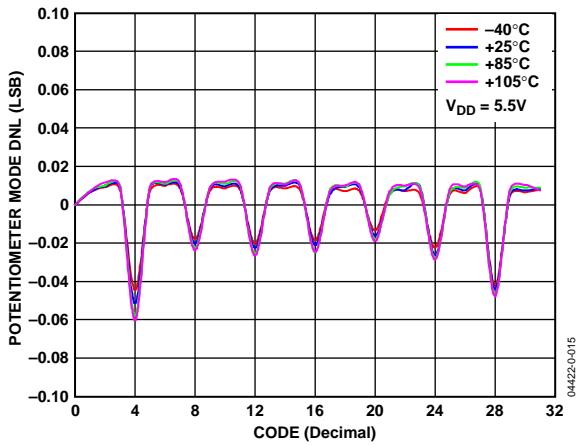


Figure 14. DNL vs. Code,  $V_{DD} = 5V$

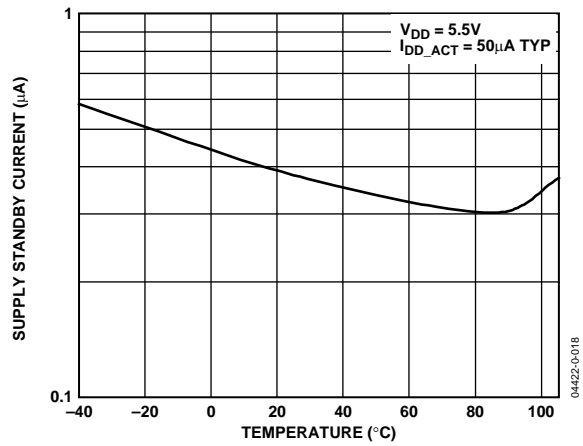


Figure 17. Supply Current vs. Temperature

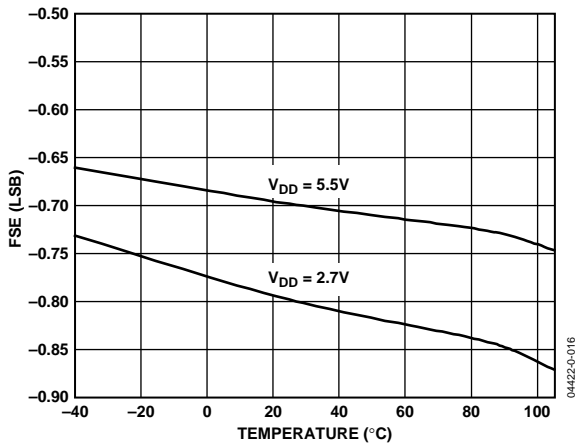


Figure 15. Full-Scale Error vs. Temperature

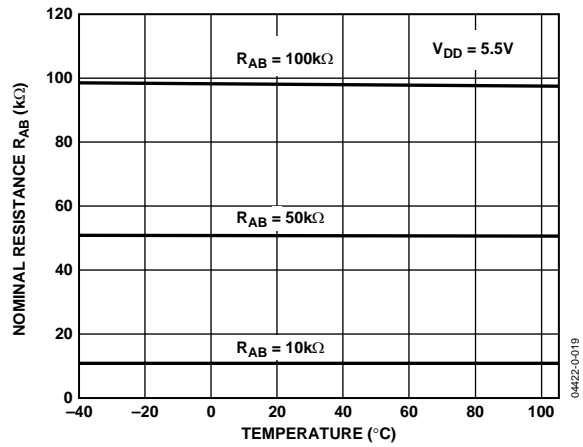


Figure 18. Nominal Resistance vs. Temperature

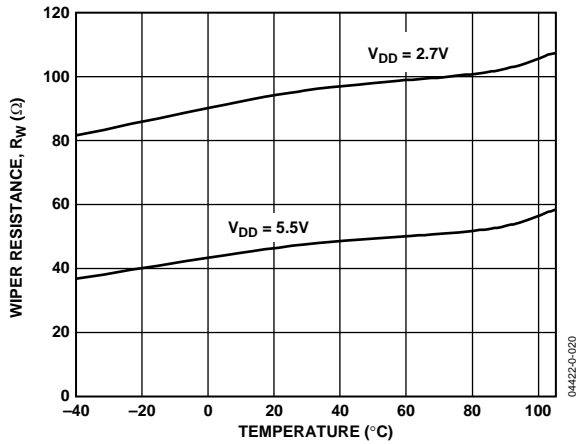


Figure 19. Wiper Resistance vs. Temperature

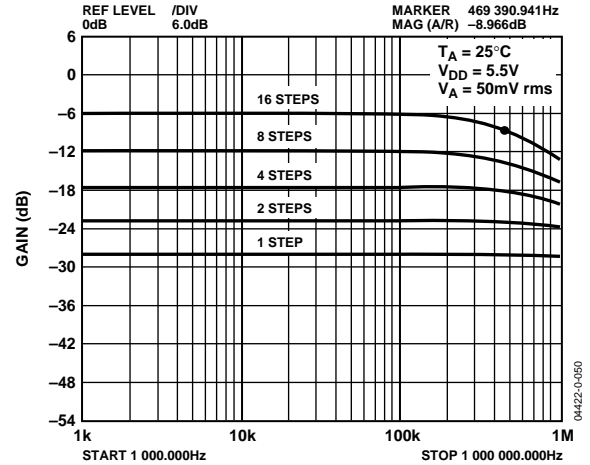


Figure 22. Gain vs. Frequency vs. Code,  $R_{AB} = 10\text{ k}\Omega$

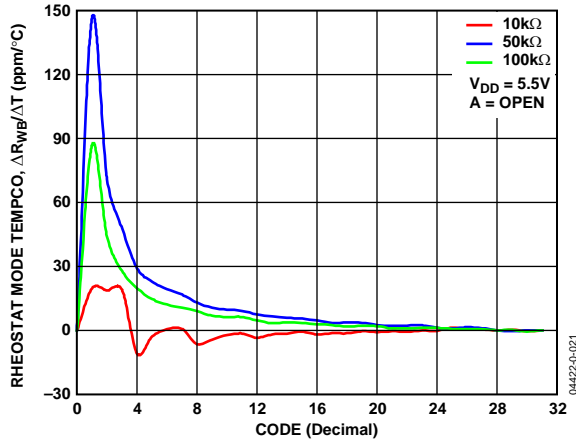


Figure 20. Rheostat Mode Tempco  $\Delta R_{WB}/\Delta T$  vs. Code

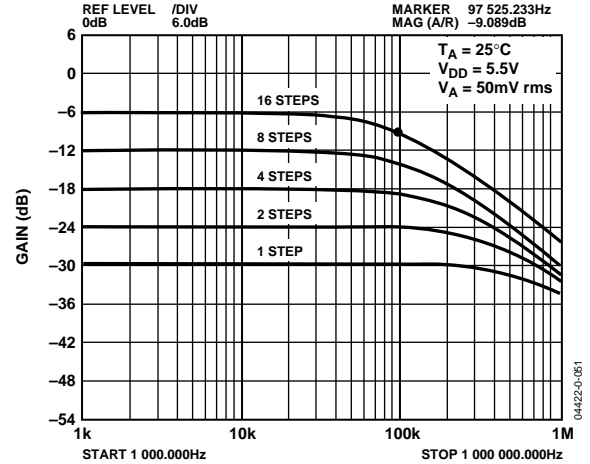


Figure 23. Gain vs. Frequency vs. Code,  $R_{AB} = 50\text{ k}\Omega$

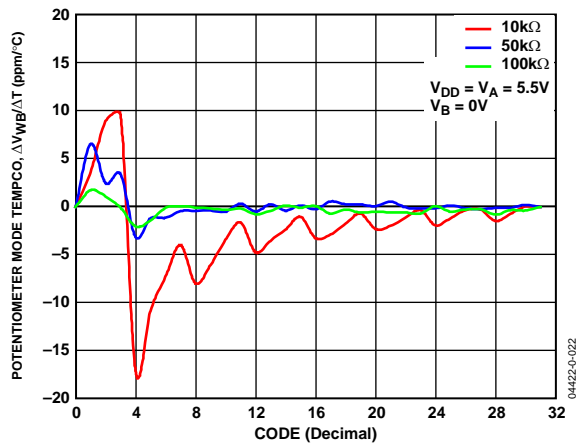


Figure 21. Potentiometer Mode Tempco  $\Delta V_{WB}/\Delta T$  vs. Code

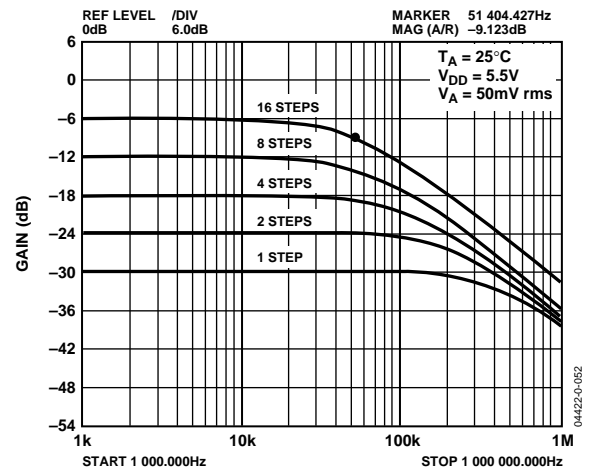


Figure 24. Gain vs. Frequency vs. Code,  $R_{AB} = 100\text{ k}\Omega$

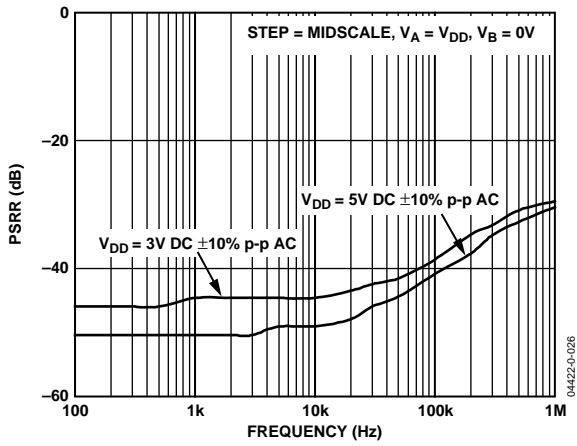


Figure 25. PSRR

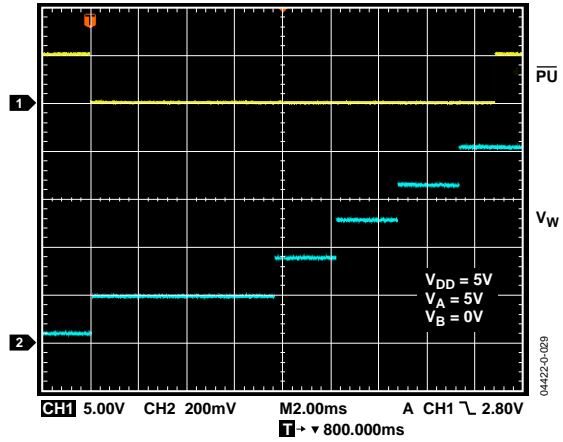


Figure 28. Autoscan Increment

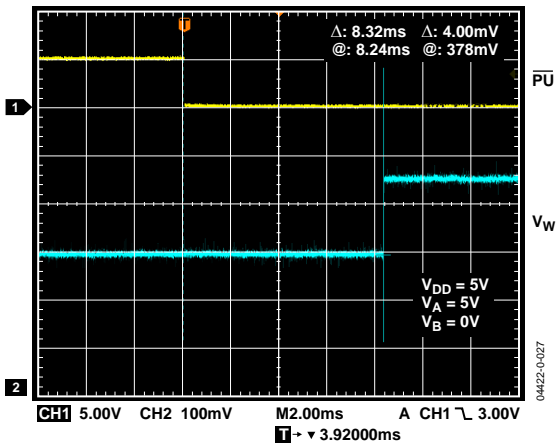


Figure 26. Basic Increment

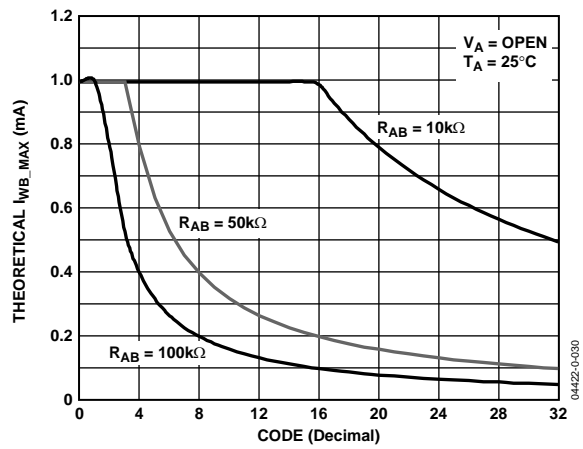


Figure 29. Maximum  $I_{WB}$  vs. Code

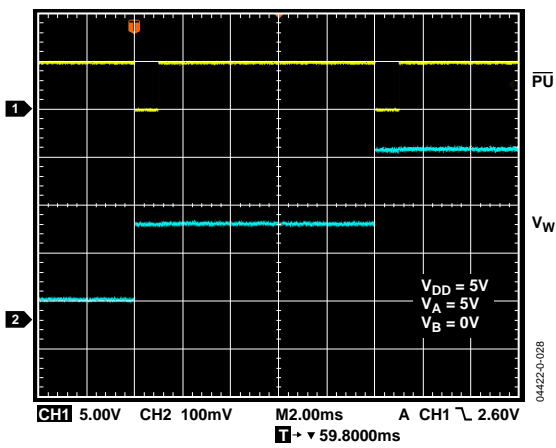


Figure 27. Repetitive Increment

## THEORY OF OPERATION

The AD5228 is a 32-position manual up/down digitally controlled potentiometer with selectable power-on preset. The AD5228 presets to midscale when the PRE pin is tied to ground and to zero-scale when PRE is tied to  $V_{DD}$ . Floating the PRE pin is not allowed. The step-up and step-down operations require the activation of the  $\overline{PU}$  (push-up) and  $\overline{PD}$  (push-down) pins. These pins have 100 k $\Omega$  internal pull-up resistors that the  $\overline{PU}$  and  $\overline{PD}$  activate at logic low. The common practice is to apply external pushbuttons (tactile switches) as shown in Figure 30.

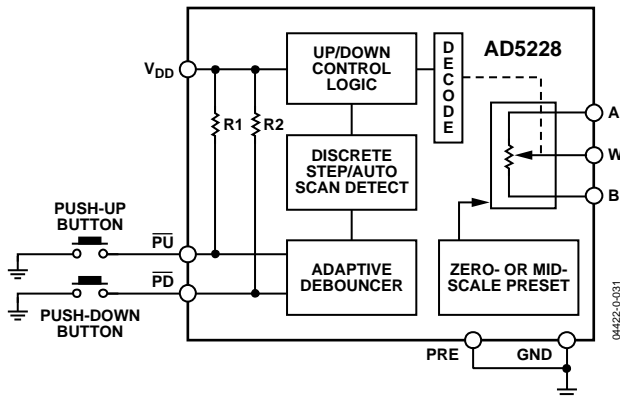


Figure 30. Typical Pushbutton Interface

Because of the bounce mechanism commonly found in the switches during contact closures, a single pushbutton press usually generates numerous bounces during contact closure. Note that the term *pushbutton* refers specifically to a pushbutton tactile switch or a similar switch that has 10 ms or less bounce time during contact closure. Figure 31 shows the characteristics of one such switch, the KRS-3550 tactile switch. Figure 32 and Figure 33 show close ups of the initial bounces and end bounces, respectively.

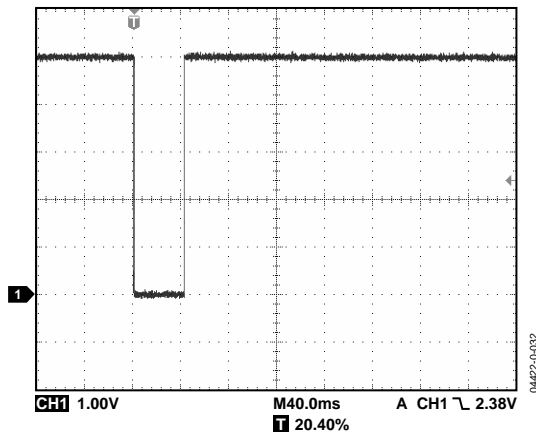


Figure 31. Typical Tactile Switch Characteristics

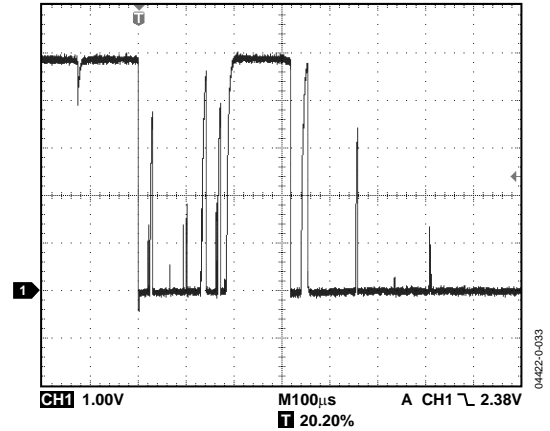


Figure 32. Close-Up of Initial Bounces

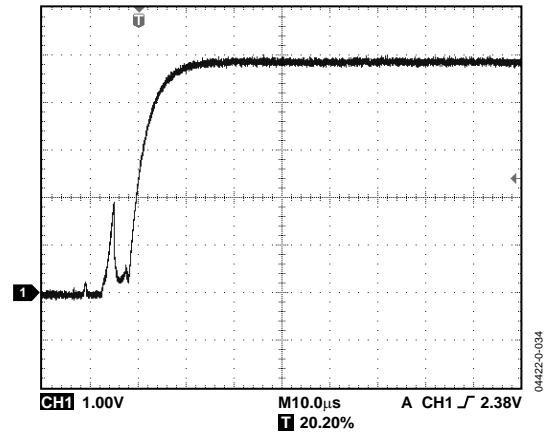


Figure 33. Close-Up of Final Bounces

The following paragraphs describes the  $\overline{PU}$  incrementing operation. Similar characteristics apply to the  $\overline{PD}$  decrementing operation.

The AD5228 features an adaptive debouncer that monitors the duration of the logic-low level of  $\overline{PU}$  signal between bounces. If the  $\overline{PU}$  logic-low level signal duration is shorter than 7 ms, the debouncer ignores it as an invalid incrementing command. Whenever the logic-low level of  $\overline{PU}$  signal lasts longer than 11 ms, the debouncer assumes that the last bounce is met and therefore increments  $R_{WB}$  by one step.

Repeatedly pressing the  $\overline{PU}$  button for fast adjustment without missing steps is allowed, provided that each press is not shorter than  $t_{PU}$ , which is 12 ms (see Figure 2). As a point of reference, an advanced video game player can press a pushbutton switch in 40 ms.

If the  $\overline{PU}$  button is held for longer than 1 second, continuously holding it activates autoscan mode such that the AD5228 increments by four  $R_{WB}$  steps per second (see Figure 3).

Whenever the maximum  $R_{WB}$  ( $= R_{AB}$ ) is reached,  $R_{WB}$  stops incrementing regardless of the state of the  $\overline{PU}$  pin. Any continuous holding of the  $\overline{PU}$  pin to logic-low simply elevates the supply current.

When both  $\overline{PU}$  and  $\overline{PD}$  buttons are pressed,  $R_{WB}$  decrements until it stops at zero scale.

All the preceding descriptions apply to  $\overline{PD}$  operation. Due to the tolerance of the internal RC oscillator, all the timing information given previously is based on the typical values, which can vary  $\pm 30\%$ .

The AD5228 debouncer is carefully designed to handle common pushbutton tactile switches. Other switches that have excessive bounces and duration are not suitable to use in conjunction with the AD5228.

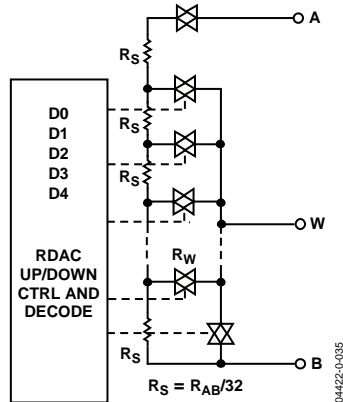


Figure 34. AD5228 Equivalent RDAC Circuit

**PROGRAMMING THE DIGITAL POTENTIOMETERS**

**Rheostat Operation**

If only the W-to-B or W-to-A terminals are used as variable resistors, the unused terminal can be opened or shorted with W. Such operation is called *rheostat mode* and is shown in Figure 35.

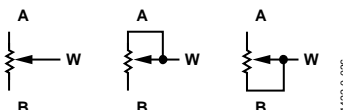


Figure 35. Rheostat Mode Configuration

The end-to-end resistance,  $R_{AB}$ , has 32 contact points accessed by the wiper terminal, plus the B terminal contact if  $R_{WB}$  is used. Pushing the  $\overline{PU}$  pin discretely increments  $R_{WB}$  by one step. The total resistance becomes  $R_S + R_W$  as shown in Figure 34. The change of  $R_{WB}$  can be determined by the number of discrete  $\overline{PU}$  executions provided that its maximum setting is not reached during operation.  $\Delta R_{WB}$  can, therefore, be approximated as

$$\Delta R_{WB} = + \left( \overline{PU} \frac{R_{AB}}{32} + R_W \right) \tag{1}$$

$$\Delta R_{WB} = - \left( \overline{PD} \frac{R_{AB}}{32} + R_W \right) \tag{2}$$

where:

$\overline{PU}$  is the number of push-up executions.

$\overline{PD}$  is the number of push-down executions.

$R_{AB}$  is the end-to-end resistance.

$R_W$  is the wiper resistance contributed by the on-resistance of the internal switch.

Similar to the mechanical potentiometer, the resistance of the RDAC between the Wiper W and Terminal A also produces a complementary resistance,  $R_{WA}$ . When these terminals are used, the B terminal can be opened or shorted to W.  $R_{WA}$  can also be approximated if its maximum and minimum settings are not reached.

$$\Delta R_{WA} = - \left( (32 - \overline{PU}) \frac{R_{AB}}{32} + R_W \right) \tag{3}$$

$$\Delta R_{WA} = + \left( (32 - \overline{PD}) \frac{R_{AB}}{32} + R_W \right) \tag{4}$$

Note that Equations 1 to 4 do not apply when  $\overline{PU}$  and  $\overline{PD} = 0$  execution.

Because in the lowest end of the resistor string, a finite wiper resistance is present, care should be taken to limit the current flow between W and B in this state to a maximum pulse current of no more than 20 mA. Otherwise, degradation or possible destruction of the internal switches can occur.

The typical distribution of the resistance tolerance from device to device is process lot dependent, and  $\pm 20\%$  tolerance is possible.

**Potentiometer Mode Operation**

If all three terminals are used, the operation is called *potentiometer mode*. The most common configuration is the voltage divider operation as shown in Figure 36.

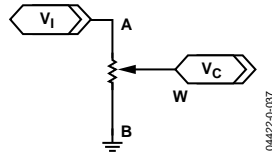


Figure 36. Potentiometer Mode Configuration

The change of  $V_{WB}$  is known provided that the AD5228 maximum or minimum scale has not been reached during operation. If the effect of wiper resistance is ignored, the transfer functions can be simplified as

$$\Delta V_{WB} = + \frac{\overline{PU}}{32} V_A \quad (5)$$

$$\Delta V_{WB} = + \frac{\overline{PD}}{32} V_A \quad (6)$$

Unlike in rheostat mode operation where the absolute tolerance is high, potentiometer mode operation yields an almost ratio-metric function of  $\overline{PU}/32$  or  $\overline{PD}/32$  with a relatively small error contributed by the  $R_W$  term. The tolerance effect is, therefore, almost canceled. Although the thin film step resistor  $R_S$  and CMOS switch resistance,  $R_W$ , have very different temperature coefficients, the ratiometric adjustment also reduces the overall temperature coefficient effect to 5 ppm/°C except at low value codes where  $R_W$  dominates.

Potentiometer mode operations include an op amp input and feedback resistors network and other voltage scaling applications. The A, W, and B terminals can be input or output terminals and have no polarity constraint provided that  $|V_{AB}|$ ,  $|V_{WA}|$ , and  $|V_{WB}|$  do not exceed  $V_{DD}$ -to-GND.

**CONTROLLING INPUTS**

All  $\overline{PU}$  and  $\overline{PD}$  inputs are protected with a Zener ESD structure as shown in Figure 37.

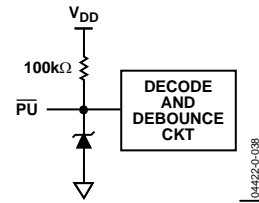


Figure 37. Equivalent ESD Protection in  $\overline{PU}$  and  $\overline{PD}$  Pins

$\overline{PU}$  and  $\overline{PD}$  pins are usually connected to pushbutton tactile switches for manual operation, but the AD5228 can also be controlled digitally. It is recommended to add external MOSFETs or transistors that simplify the logic controls.

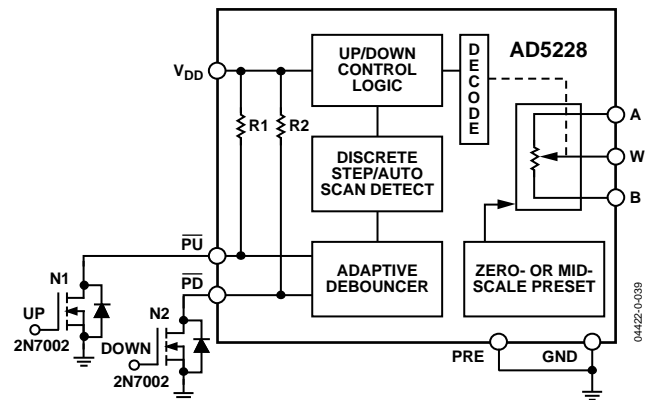


Figure 38. Digital Control with External MOSFETs

**TERMINAL VOLTAGE OPERATION RANGE**

The AD5228 is designed with internal ESD diodes for protection. These diodes also set the voltage boundary of the terminal operating voltages. Positive signals present on Terminal A, B, or W that exceed  $V_{DD}$  are clamped by the forward-biased diode. There is no polarity constraint between  $V_A$ ,  $V_W$ , and  $V_B$ , but they cannot be higher than  $V_{DD}$  or lower than GND.

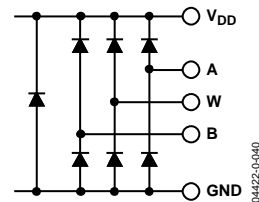


Figure 39. Maximum Terminal Voltages Set by  $V_{DD}$  and GND

### POWER-UP AND POWER-DOWN SEQUENCES

Because of the ESD protection diodes that limit the voltage compliance at Terminals A, B, and W (Figure 39), it is important to power on  $V_{DD}$  before applying any voltage to Terminals A, B, and W. Otherwise, the diodes are forward-biased such that  $V_{DD}$  is powered on unintentionally and can affect other parts of the circuit. Similarly,  $V_{DD}$  should be powered down last. The ideal power-on sequence is in the following order: GND,  $V_{DD}$ , and  $V_{A/B/W}$ . The order of powering  $V_A$ ,  $V_B$ , and  $V_W$  is not important as long as they are powered on after  $V_{DD}$ . The states of the  $\overline{PU}$  and  $\overline{PD}$  pins can be logic high or floating, but they should not be logic low during power-on.

### LAYOUT AND POWER SUPPLY BIASING

It is always a good practice to use compact, minimum lead length layout design. The leads to the input should be as direct as possible with a minimum conductor length. Ground paths should have low resistance and low inductance. It is also good practice to bypass the power supplies with quality capacitors. Low ESR (equivalent series resistance)  $1\ \mu\text{F}$  to  $10\ \mu\text{F}$  tantalum or electrolytic capacitors should be applied at the supplies to minimize any transient disturbance and to filter low frequency ripple. Figure 39 illustrates the basic supply bypassing configuration for the AD5228.

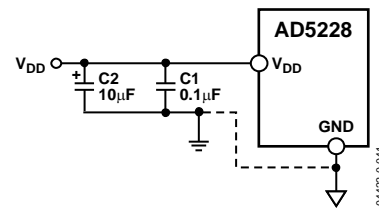


Figure 40. Power Supply Bypassing



**AUTOMATIC LCD PANEL BACKLIGHT CONTROL**

With the addition of a photocell sensor, an automatic brightness control can be achieved. As shown in Figure 44, the resistance of the photocell changes linearly but inversely with the light output. The brighter the light output, the lower the photocell resistance and vice versa. The AD5228 sets the voltage level that is gained up by U2 to drive N1 to a desirable brightness. With the photocell acting as the variable feedback resistor, the change in the light output changes the R2 resistance, therefore causing U2 to drive N1 accordingly to regulate the output. This simple low cost implementation of an LED controller can compensate for the temperature and aging effects typically found in high power LEDs. Similarly, for power efficiency, a PWM signal can be applied at the gate of N2 to switch the LED on and off without noticeable effect.

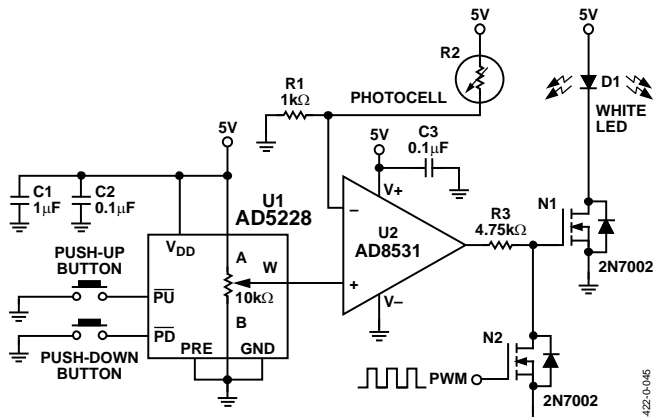


Figure 44. Automatic LCD Panel Backlight Control

04422-0-046

**AUDIO AMPLIFIER WITH VOLUME CONTROL**

The AD5228 and SSM2211 can form a 1.5 W audio amplifier with volume control that has adequate power and quality for portable devices such as PDAs and cell phones. The SSM2211 can drive a single speaker differentially between Pins 5 and 8 without any output capacitor. The high-pass cutoff frequency is  $f_{H1} = 1/(2 \times \pi \times R1 \times C1)$ . The SSM2211 can also drive two speakers as shown in Figure 45. However, the speakers must be configured in single-ended mode, and output coupling capacitors are needed to block the dc current. The output capacitor and the speaker load form an additional high-pass cutoff frequency as  $f_{H2} = 1/(2 \times \pi \times R5 \times C3)$ . As a result, C3 and C4 must be large to make the frequency as low as  $f_{H1}$ .

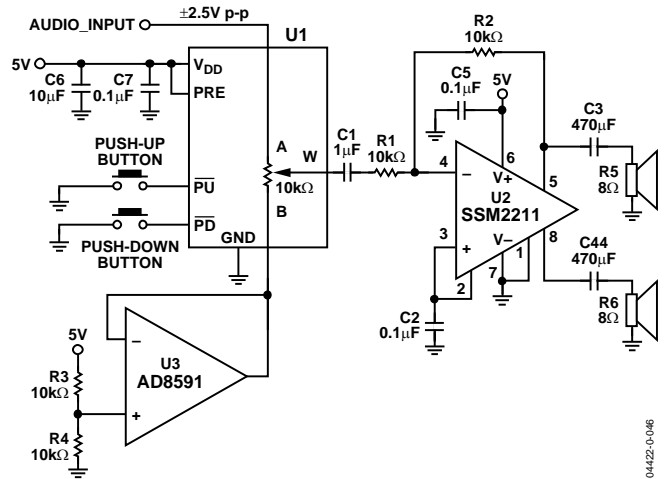


Figure 45. Audio Amplifier with Volume Control

04422-0-046

**CONSTANT BIAS WITH SUPPLY TO RETAIN RESISTANCE SETTING**

Users who consider EEMEM potentiometers but cannot justify the additional cost and programming for their designs can consider constantly biasing the AD5228 with the supply to retain the resistance setting as shown in Figure 46. The AD5228 is designed specifically with low power to allow power conservation even in battery-operated systems. As shown in Figure 47, a similar low power digital potentiometer is biased with a 3.4 V 450 mA/hour Li-Ion cell phone battery. The measurement shows that the device drains negligible power. Constantly biasing the potentiometer is a practical approach because most of the portable devices do not require detachable batteries for charging. Although the resistance setting of the AD5228 is lost when the battery needs to be replaced, this event occurs so infrequently that the inconvenience is minimal for most applications.

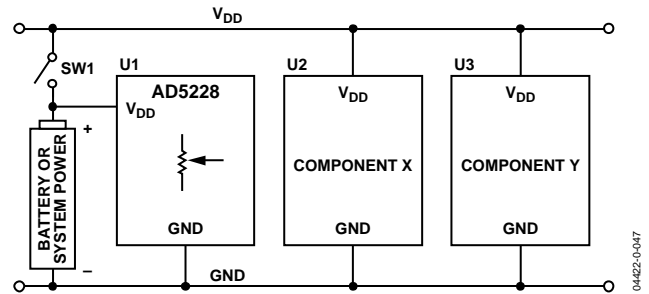


Figure 46. Constant Bias AD5228 for Resistance Retention

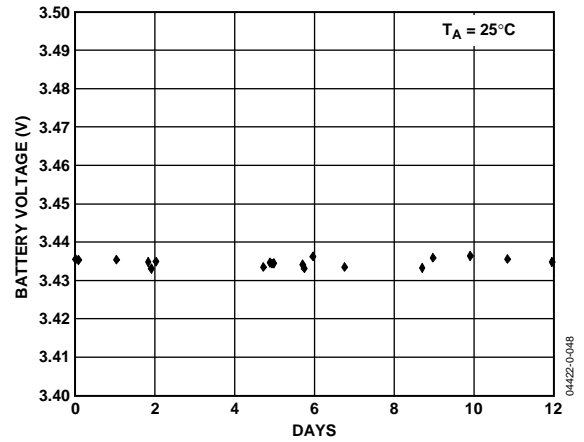
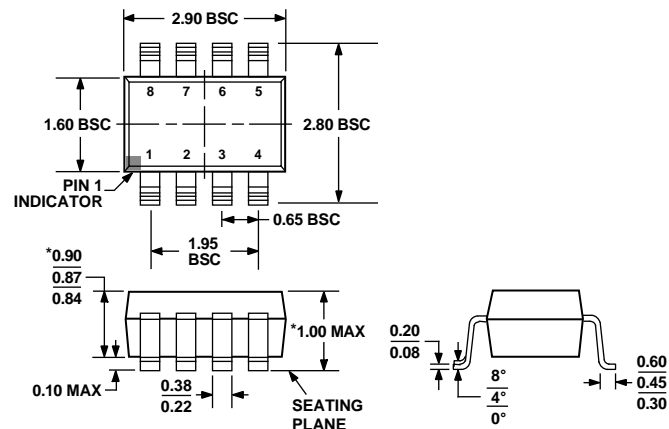


Figure 47. Battery Consumption Measurement

## OUTLINE DIMENSIONS



\*COMPLIANT TO JEDEC STANDARDS MO-193-BA WITH THE EXCEPTION OF PACKAGE HEIGHT AND THICKNESS.

Figure 48. 8-Lead Small Outline Transistor Package [TSOT] (UJ-8)

Dimensions shown in millimeters

## ORDERING GUIDE

Model <sup>1,2</sup>	R <sub>AB</sub> (kΩ)	Temperature Range	Package Description	Package Option	Ordering Quantity	Branding
AD5228BUJZ10-RL7	10	−40°C to +105°C	8-Lead TSOT	UJ-8	3000	D3K
AD5228BUJZ10-R2	10	−40°C to +105°C	8-Lead TSOT	UJ-8	250	D3K
AD5228BUJZ50-RL7	50	−40°C to +105°C	8-Lead TSOT	UJ-8	3000	D3L
AD5228BUJZ100-RL7	100	−40°C to +105°C	8-Lead TSOT	UJ-8	3000	D3M
AD5228BUJZ100-R2	100	−40°C to +105°C	8-Lead TSOT	UJ-8	250	D3M
EVAL-AD5228DBZ	10		Evaluation Board		1	

<sup>1</sup> The end-to-end resistance R<sub>AB</sub> is available in 10 kΩ, 50 kΩ, and 100 kΩ. The final three characters of the part number determine the nominal resistance value, for example, 10 kΩ = 10.

<sup>2</sup> Z = RoHS Compliant Part.

## Looking for pricing, stock, or lifecycle information?

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 [Analog Devices Inc. Information](#)

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