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September 2014

LM317M — 3-Terminal 0.5A Positive Adjustable Regulator

LM317M 3-Terminal 0.5A Positive Adjustable Regulator

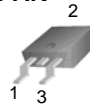
Features

- Output Current in Excess of 0.5 A
- Output Adjustable Between 1.2 V and 37 V
- Internal Thermal Overload Protection
- Internal Short-Circuit Current Limiting
- Output Transistor Safe Area Compensation
- Floating Operation for High Voltage Applications

Description

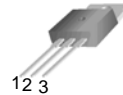
The LM317M is a 3-terminal adjustable positive voltage regulator capable of supplying in excess of 500 mA over an output voltage range of 1.2 V to 37 V. This voltage regulator is exceptionally easy to use and requires only two external resistors to set the output voltage.

D-PAK



1. Adj 2. Output 3. Input

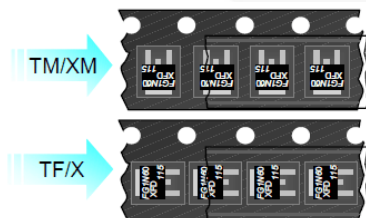
TO-220 (Single Gauge)



Ordering Information

Product Number	Marking	Package	Packing Method	Operating Temperature
LM317MDTX	LM317MDT	TO-252 3L (D-PAK)	Tape and Reel	0 to +125°C
LM317MDTXM	LM317MDT	TO-252 3L (D-PAK)	Tape and Reel	
LM317MT	LM317M	TO-220 3L (Single Gauge)	Rail	

* Refer to below unit orientation figure for TM / TF suffix packing.



Block Diagram

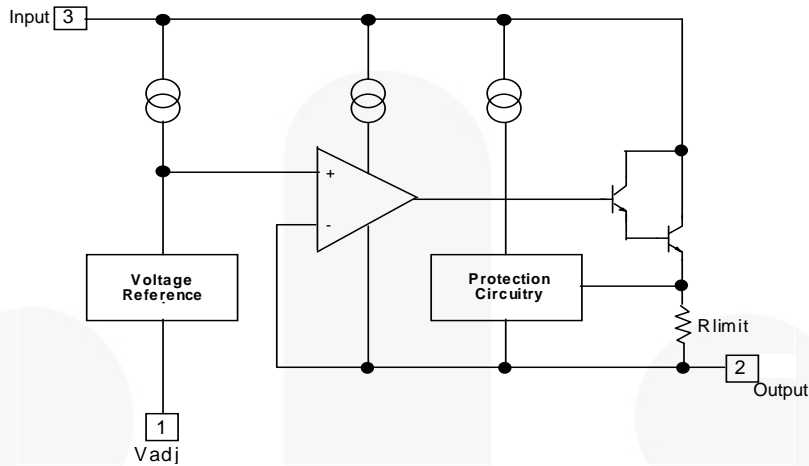


Figure 1. Block Diagram

Absolute Maximum Ratings

Stresses exceeding the absolute maximum ratings may damage the device. The device may not function or be operable above the recommended operating conditions and stressing the parts to these levels is not recommended. In addition, extended exposure to stresses above the recommended operating conditions may affect device reliability. The absolute maximum ratings are stress ratings only. Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value	Unit
$V_I - V_O$	Input-Output Voltage Differential	40	V
T_J	Operating Junction Temperature Range	0 to +125	$^\circ\text{C}$
T_{STG}	Storage Temperature Range	-65 to +125	$^\circ\text{C}$

Thermal Characteristics

Values are at $T_A = 25^\circ\text{C}$ unless otherwise noted.

Symbol	Parameter	Value		Unit
		LM317MT	LM317MDTX / LM317MDTXM ^{(1),(2)}	
P_D	Power Dissipation	Internally Limited		W
$R_{\theta\text{JC}}$	Thermal Resistance, Junction to Case	5	-	$^\circ\text{C}/\text{W}$
$R_{\theta\text{JA}}$	Thermal Resistance, Junction to Ambient	81	100	$^\circ\text{C}/\text{W}$

Notes:

- Thermal resistance test board - size: 76.2 mm x 114.3 mm x 1.6 mm (1S0P), JEDEC standard: JESD51-3, JESD51-7
- Assume no ambient airflow

Electrical Characteristics

$V_I - V_O = 5\text{ V}$, $I_O = 0.1\text{ A}$, $0^\circ\text{C} \leq T_J \leq +125^\circ\text{C}$, $P_{D\text{MAX}} = 7.5\text{ W}$, unless otherwise specified.

Symbol	Parameter	Conditions	Min.	Typ.	Max.	Unit
Rline	Line Regulation ⁽³⁾	$T_A = +25^\circ\text{C}$, $3\text{ V} \leq V_I - V_O \leq 40\text{ V}$		0.01	0.04	% / V
		$3\text{ V} \leq V_I - V_O \leq 40\text{ V}$		0.02	0.07	
Rload	Load Regulation ⁽³⁾	$T_A = +25^\circ\text{C}$, $10\text{ mA} \leq I_O \leq 0.5\text{ A}$, $V_O \leq 5\text{ V}$		5	25	mV
		$T_A = +25^\circ\text{C}$, $10\text{ mA} \leq I_O \leq 0.5\text{ A}$, $V_O \geq 5\text{ V}$		0.1	0.5	% / V_O
		$10\text{ mA} \leq I_O \leq 0.5\text{ A}$, $V_O \leq 5\text{ V}$		20	70	mV
		$10\text{ mA} \leq I_O \leq 0.5\text{ A}$, $V_O \geq 5\text{ V}$		0.3	1.5	% / V_O
I_{ADJ}	Adjustment Pin Current	-		50	100	μA
ΔI_{ADJ}	Adjustment Pin Current Change	$3\text{ V} \leq V_I - V_O \leq 40\text{ V}$, $10\text{ mA} \leq I_O \leq 0.5\text{ A}$, $P_D < P_{D\text{MAX}}$		0.2	5.0	μA
V_{REF}	Reference Voltage	$3\text{ V} < V_I - V_O < 40\text{ V}$, $10\text{ mA} \leq I_O \leq 0.5\text{ A}$, $P_D < P_{D\text{MAX}}$	1.20	1.25	1.30	V
ST_T	Temperature Stability	$T_J = 0^\circ\text{C}$ to $+125^\circ\text{C}$		0.7		% / V_O
$I_{L(\text{MIN})}$	Minimum Load Current to Maintain Regulation	$V_I - V_O = 40\text{ V}$		3.5	10.0	mA
$I_{O(\text{MAX})}$	Maximum Output Current	$V_I - V_O \leq 15\text{ V}$, $P_D < P_{D\text{MAX}}$	0.5	0.9		A
		$V_I - V_O = 40\text{ V}$, $P_D < P_{D\text{MAX}}$, $T_A = +25^\circ\text{C}$	0.15	0.25		
e_N	RMS Noise, % of V_{OUT}	$T_A = +25^\circ\text{C}$, $10\text{ Hz} < f < 10\text{ kHz}$		0.003		% / V_O
RR	Ripple Rejection	$V_O = 10\text{ V}$, $f = 120\text{ Hz}$, without C_{ADJ}	66	65		dB
		$V_O = 10\text{ V}$, $f = 120\text{ Hz}$, $C_{\text{ADJ}} = 10\text{ }\mu\text{F}^{(4)}$		80		
ST	Long-Term Stability	$T_J = +125^\circ\text{C}$, 1000 Hours		0.3	1	% / 1000Hrs

Notes:

- Load and Line regulation are specified at constant junction temperature. Change in V_O due to heating effects must be taken into account separately. Pulse testing with low duty cycle is used.
- C_{ADJ} , when used, is connected between the adjustment pin and ground.

Typical Performance Characteristics

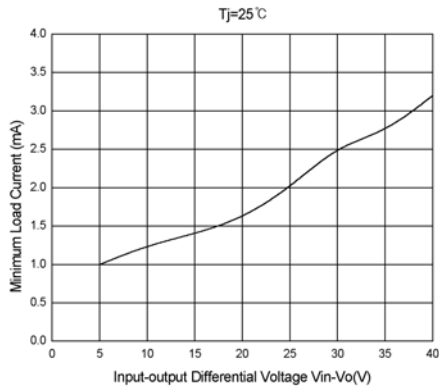


Figure 2. Minimum Load Current

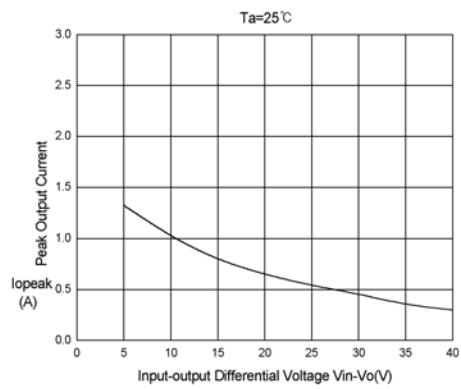


Figure 3. Peak Output Current vs. Input-Output Differential Voltage

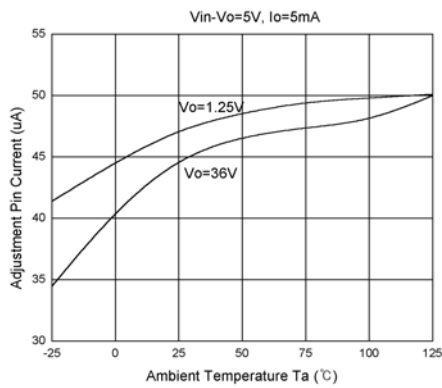


Figure 4. Adjustment Pin Current vs. Temperature

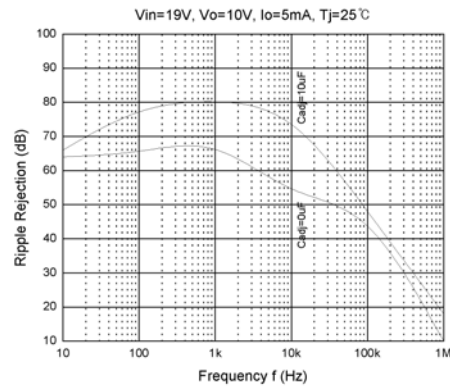


Figure 5. Ripple Rejection vs. Frequency

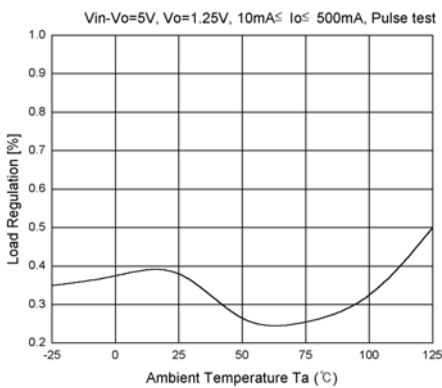


Figure 6. Load Regulation vs. Temperature

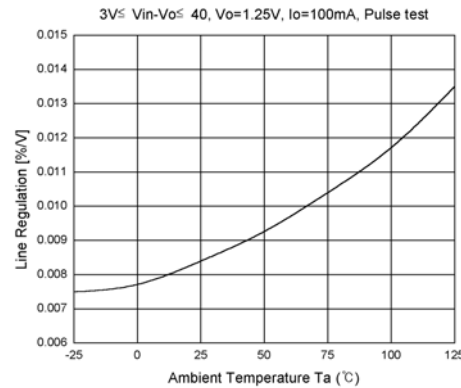


Figure 7. Line Regulation vs. Temperature

Typical Performance Characteristics (Continued)

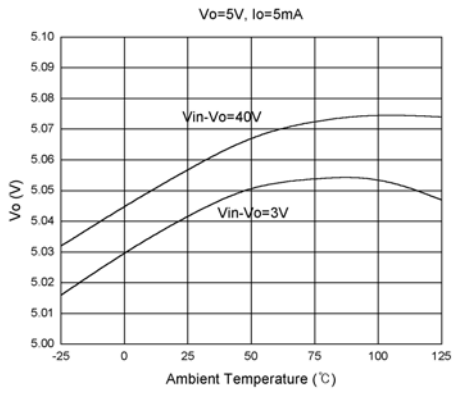


Figure 8. Output Voltage vs. Temperature

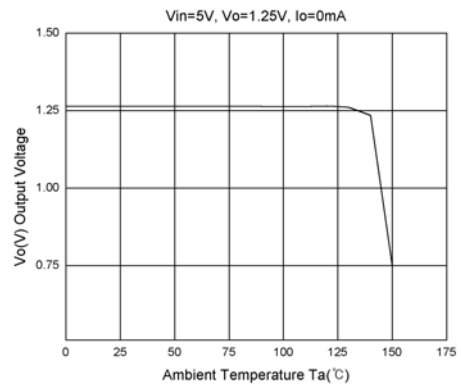


Figure 9. Thermal Shutdown



Typical Application

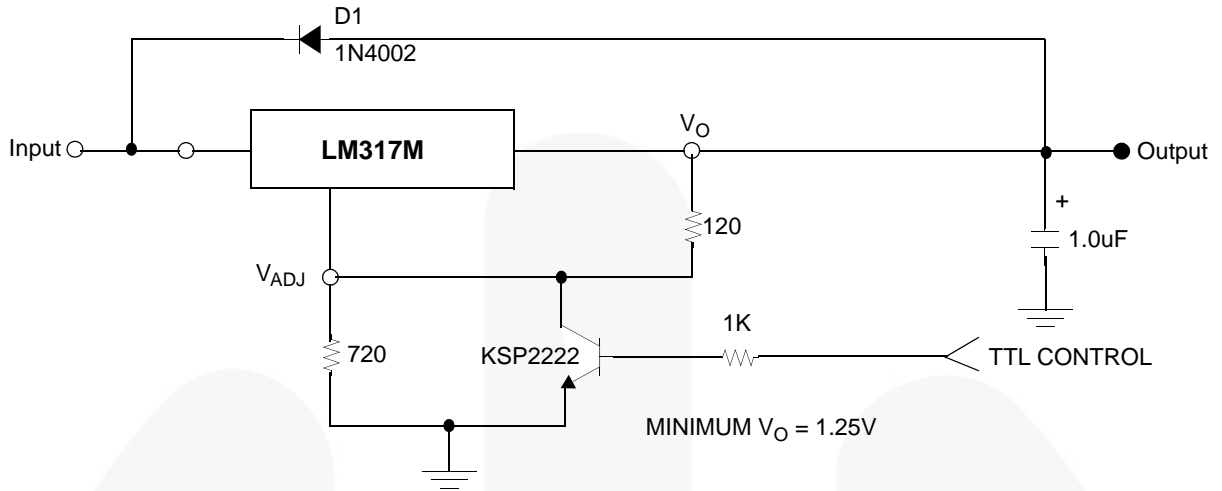


Figure 10. 15V Electronic Shutdown Regulator⁽⁵⁾

Note:

5. D1 protects the device during an input short circuit.

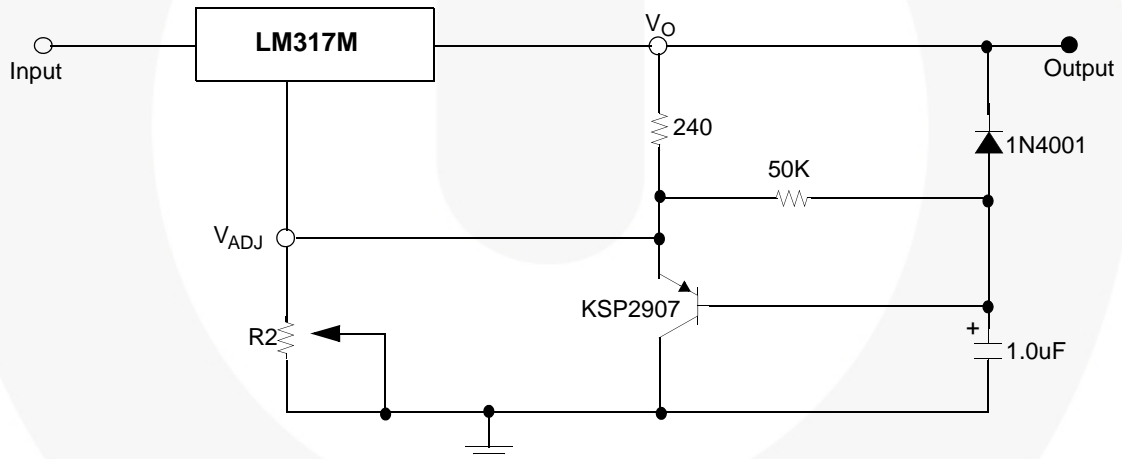
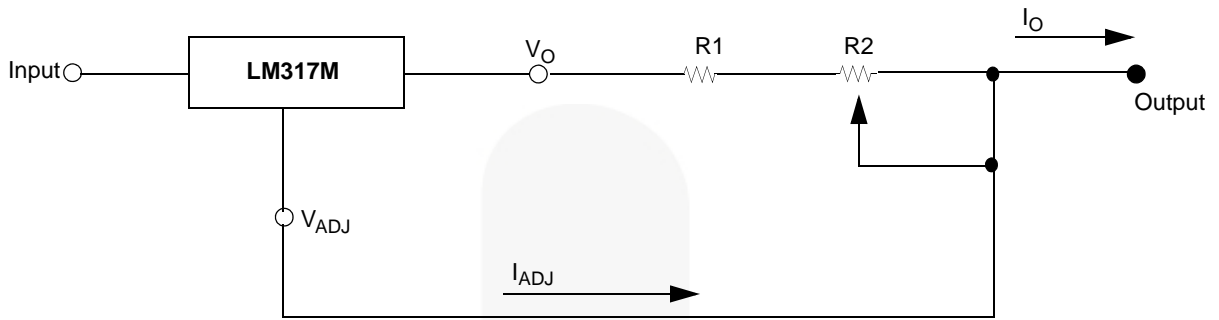


Figure 11. Slow Turn-On Regulator

Typical Application (Continued)



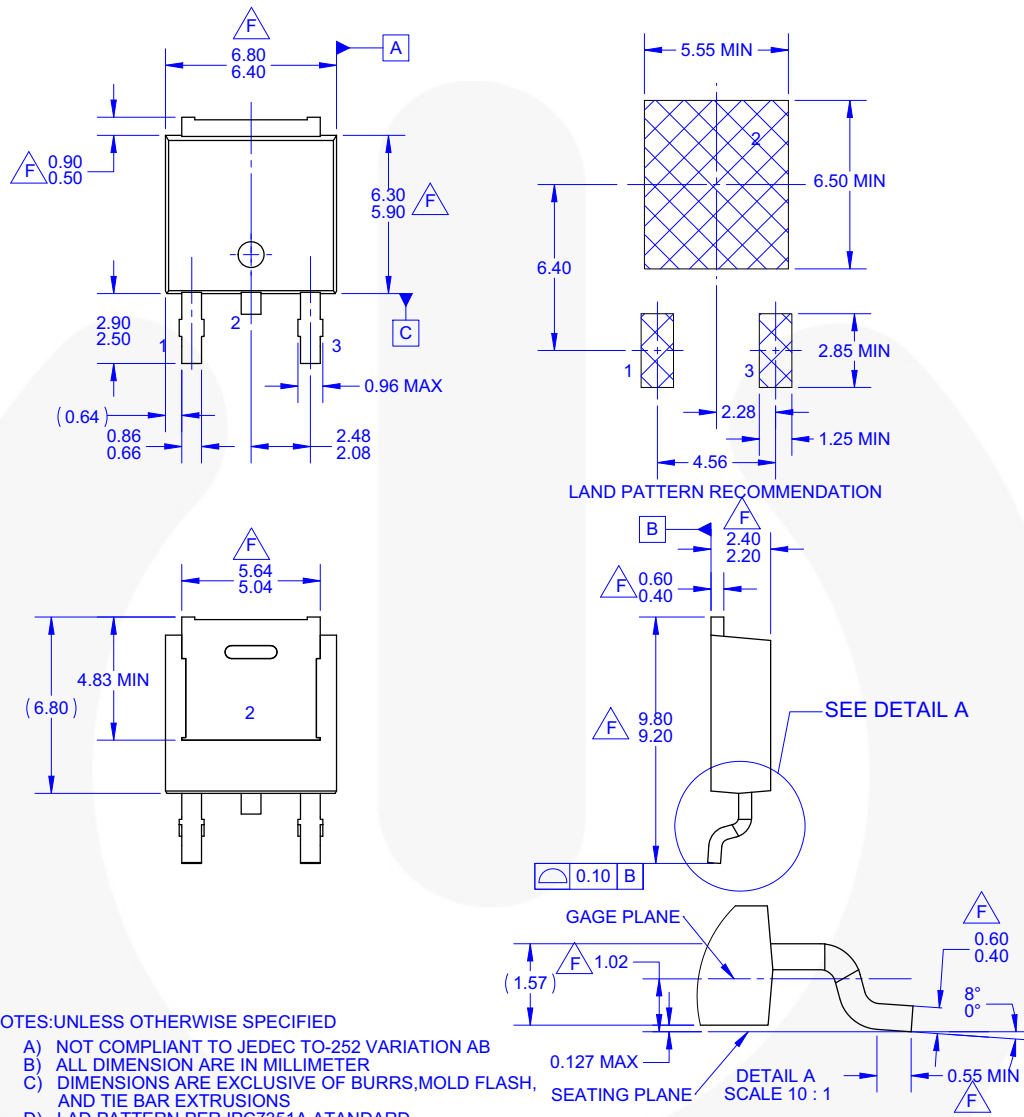
$$I_{O\text{MAX}} = \left(\frac{V_{\text{REF}}}{R_1} \right) + I_{\text{ADJ}} \cong \frac{1.25\text{V}}{R_1}$$

$$I_{O\text{MAX}} = \left(\frac{V_{\text{REF}}}{R_1 + R_2} \right) + I_{\text{ADJ}} \cong \frac{1.25\text{V}}{R_1 + R_2}$$

5mA < I_O < 500mA

Figure 12. Current Regulator

Physical Dimensions



- NOTES: UNLESS OTHERWISE SPECIFIED
- A) NOT COMPLIANT TO JEDEC TO-252 VARIATION AB
 - B) ALL DIMENSION ARE IN MILLIMETER
 - C) DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS
 - D) LAD PATTERN PER IPC7351A ATANDARD TO228P991X239-3N
 - E) DRAWING FILE NAME: MKT-TO252D03REV3.
 - F) DOES NOT COMPLY JEDEC STANDARD VALUE.
 - G) FAIRCHILD SEMICONDUCTOR.

Figure 13. 3LEAD, TO-252, JEDEC TO-252 VAR. AB, SURFACE MOUNT (DPAK)

Physical Dimensions (Continued)

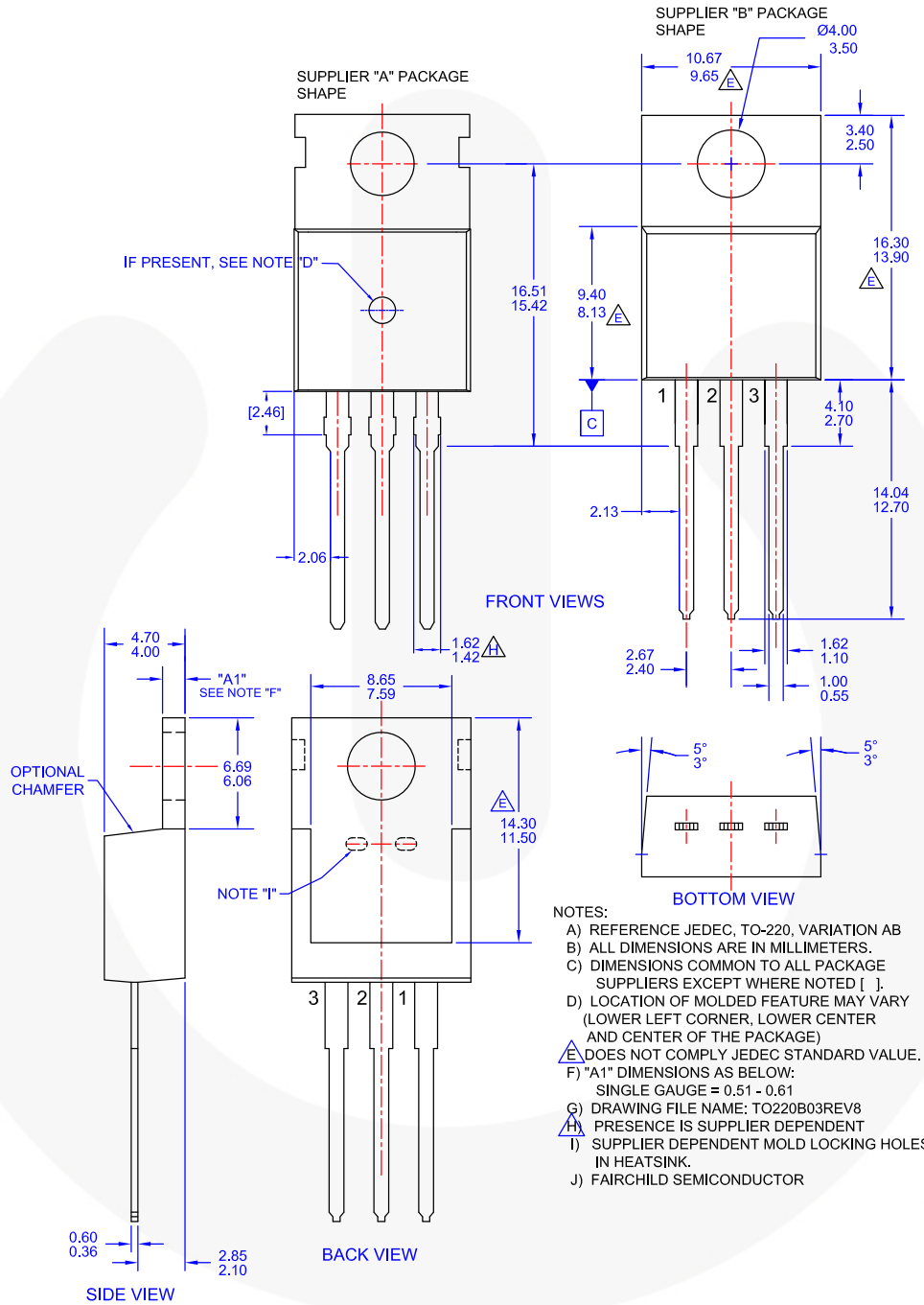


Figure 14. TO-220, MOLDED, 3LEAD, JEDEC VARIATION AB



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