WINSOURCE
ELECTRONICS

THE DATASHEET OF

IRFR3706

PD - 93933B

International
IOR Rectifier

SMPS MOSFET

IRFR3706
IRFU3706

HEXFET® Power MOSFET

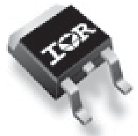
V_{DSS}	$R_{DS(on)}$ max	I_D
20V	**9.0mΩ**	**75A**④

Applications

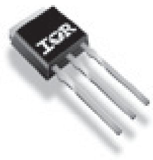
- High Frequency Isolated DC-DC Converters with Synchronous Rectification for Telecom and Industrial Use
- High Frequency Buck Converters for Computer Processor Power

Benefits

- Ultra-Low Gate Impedance
- Very Low RDS(on) at 4.5V V_{GS}
- Fully Characterized Avalanche Voltage and Current



D-Pak
IRFR3706



I-Pak
IRFU3706

Absolute Maximum Ratings

Symbol	Parameter	Max.	Units
V_{DS}	Drain-Source Voltage	20	V
V_{GS}	Gate-to-Source Voltage	± 12	V
I_D @ T_C = 25°C	Continuous Drain Current, V_{GS} @ 10V	75 ④	A
I_D @ T_C = 100°C	Continuous Drain Current, V_{GS} @ 10V	53 ④	
I_{DM}	Pulsed Drain Current①	280	
P_D @T_C = 25°C	Maximum Power Dissipation③	88	W
P_D @T_C = 100°C	Maximum Power Dissipation③	44	W
	Linear Derating Factor	0.59	mW/°C
T_J , T_{STG}	Junction and Storage Temperature Range	-55 to + 175	°C

Thermal Resistance

	Parameter	Typ.	Max.	Units
$R_{\theta JC}$	Junction-to-Case⑤	–––	1.7	°C/W
$R_{\theta JA}$	Junction-to-Ambient (PCB mount)*⑤	–––	50	
$R_{\theta JA}$	Junction-to-Ambient⑤	–––	110	

* When mounted on 1" square PCB (FR-4 or G-10 Material) .
For recommended footprint and soldering techniques refer to application note #AN-994

Notes ① through ⑤ are on page 10

Static @ T_J = 25°C (unless otherwise specified)

	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	20	——	——	V	V_{GS} = 0V, I_D = 250μA
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient	——	0.021	——	V/°C	Reference to 25°C, I_D = 1mA
$R_{DS(on)}$	Static Drain-to-Source On-Resistance	——	6.9	9.0	mΩ	V_{GS} = 10V, I_D = 15A ③
		——	8.1	11		V_{GS} = 4.5V, I_D = 12A ③
		——	11.5	23		V_{GS} = 2.8V, I_D = 7.5A ③
$V_{GS(th)}$	Gate Threshold Voltage	0.6	——	2.0	V	V_{DS} = V_{GS}, I_D = 250μA
I_{DSS}	Drain-to-Source Leakage Current	——	——	20	μA	V_{DS} = 16V, V_{GS} = 0V
		——	——	100		V_{DS} = 16V, V_{GS} = 0V, T_J = 125°C
I_{GSS}	Gate-to-Source Forward Leakage	——	——	200	nA	V_{GS} = 12V
	Gate-to-Source Reverse Leakage	——	——	-200		V_{GS} = -12V

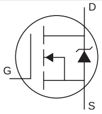
Dynamic @ T_J = 25°C (unless otherwise specified)

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
g_{fs}	Forward Transconductance	53	——	——	S	V_{DS} = 16V, I_D = 57A
Q_g	Total Gate Charge	——	23	35	nC	I_D = 28A
Q_{gs}	Gate-to-Source Charge	——	8.0	12		V_{DS} = 10V
Q_{gd}	Gate-to-Drain ("Miller") Charge	——	5.5	8.3		V_{GS} = 4.5V ③
Q_{oss}	Output Gate Charge	——	16	24		V_{GS} = 0V, V_{DS} = 10V
Rg	Gate Resistance	——	1.8	——	Ω	
$t_{d(on)}$	Turn-On Delay Time	——	6.8	——	ns	V_{DD} = 10V
t_r	Rise Time	——	87	——		I_D = 28A
$t_{d(off)}$	Turn-Off Delay Time	——	17	——		R_G = 1.8Ω
t_f	Fall Time	——	4.8	——		V_{GS} = 4.5V ③
C_{iss}	Input Capacitance	——	2410	——	pF	V_{GS} = 0V
C_{oss}	Output Capacitance	——	1070	——		V_{DS} = 10V
C_{rss}	Reverse Transfer Capacitance	——	140	——		ƒ = 1.0MHz

Avalanche Characteristics

Symbol	Parameter	Typ.	Max.	Units
E_{AS}	Single Pulse Avalanche Energy②	——	220	mJ
I_{AR}	Avalanche Current①	——	28	A

Diode Characteristics

Symbol	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)	——	——	75④	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①	——	——	280		
V_{SD}	Diode Forward Voltage	——	0.88	1.3	V	T_J = 25°C, I_S = 36A, V_{GS} = 0V ③
		——	0.82	——		T_J = 125°C, I_S = 36A, V_{GS} = 0V ③
t_{rr}	Reverse Recovery Time	——	45	68	ns	T_J = 25°C, I_F = 36A, V_R=20V
Q_{rr}	Reverse Recovery Charge	——	65	98	nC	di/dt = 100A/μs ③
t_{rr}	Reverse Recovery Time	——	49	74	ns	T_J = 125°C, I_F = 36A, V_R=20V
Q_{rr}	Reverse Recovery Charge	——	78	120	nC	di/dt = 100A/μs ③

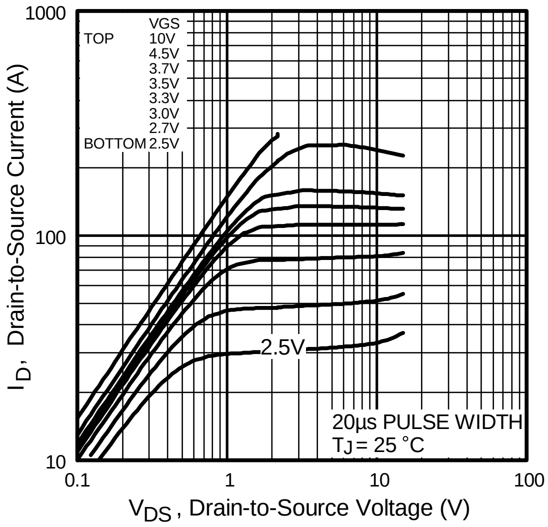


Fig 1. Typical Output Characteristics

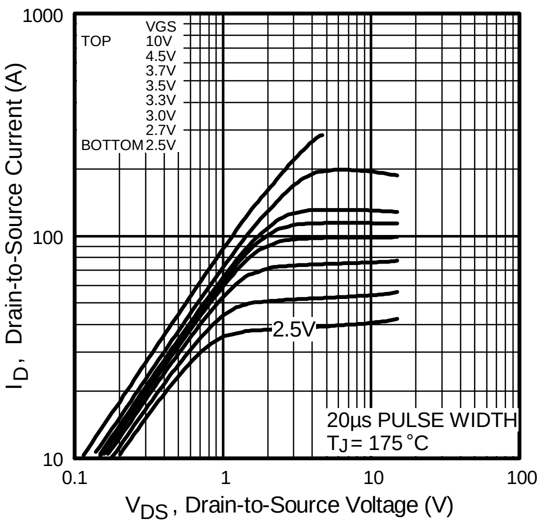


Fig 2. Typical Output Characteristics

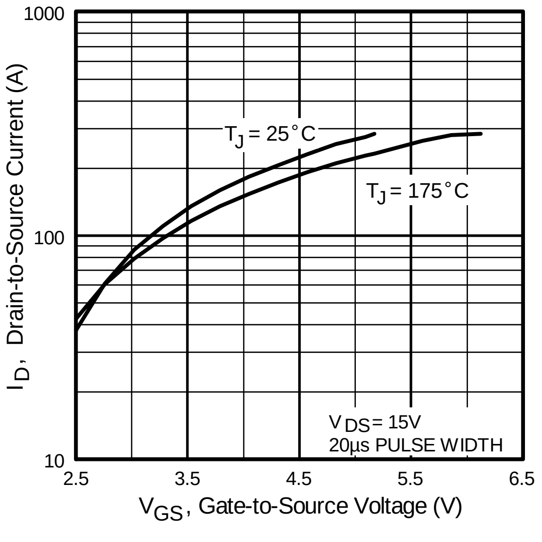


Fig 3. Typical Transfer Characteristics

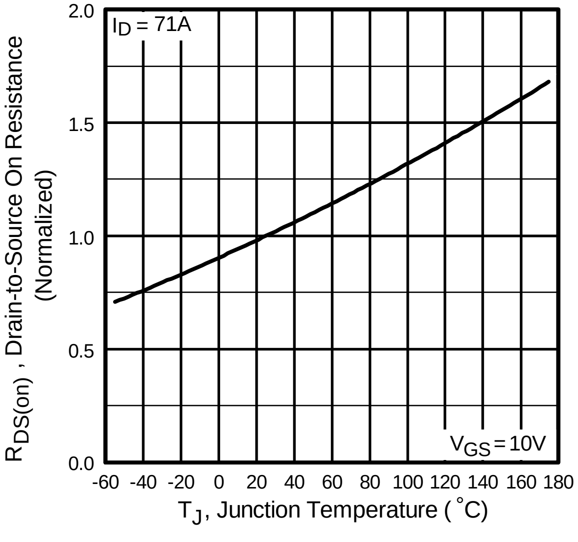


Fig 4. Normalized On-Resistance
Vs. Temperature

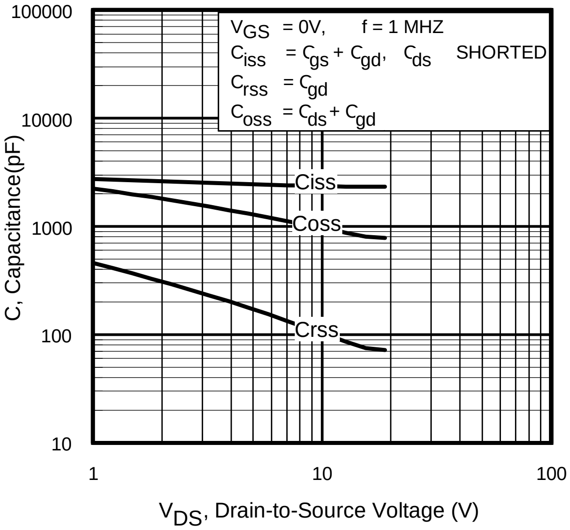


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

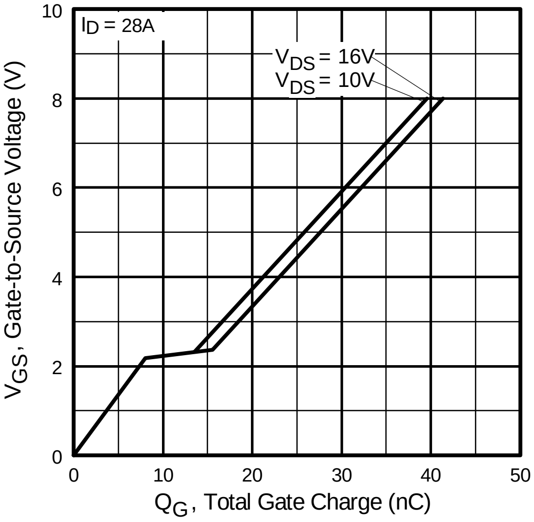


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

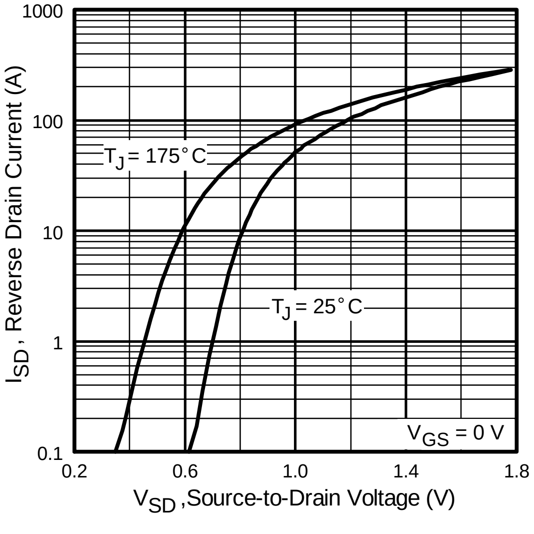


Fig 7. Typical Source-Drain Diode Forward Voltage

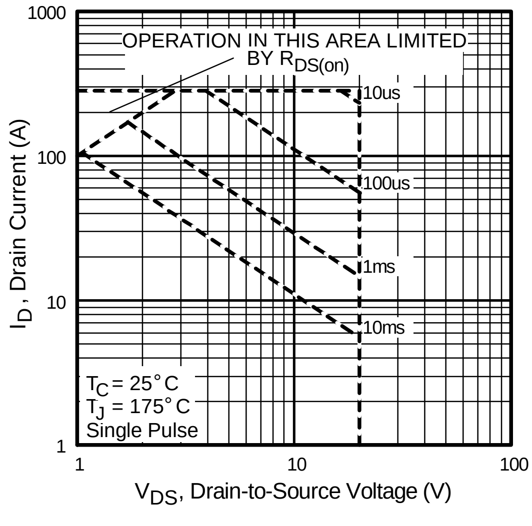


Fig 8. Maximum Safe Operating Area

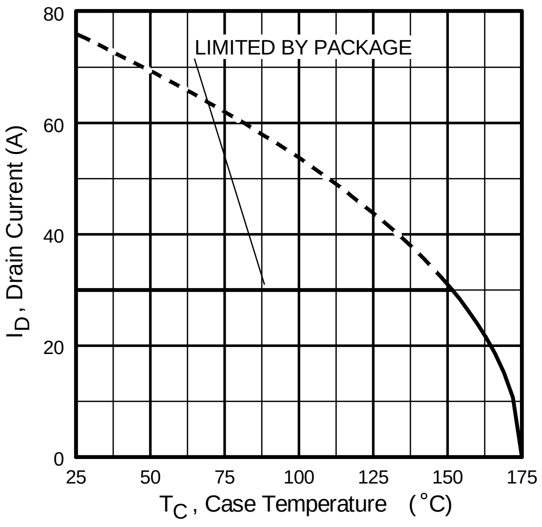


Fig 9. Maximum Drain Current Vs. Case Temperature

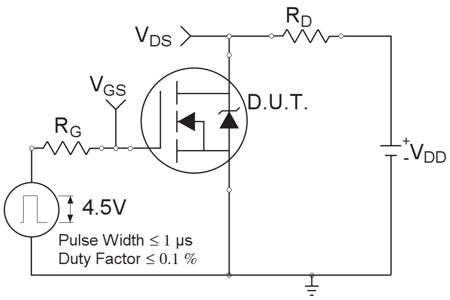


Fig 10a. Switching Time Test Circuit

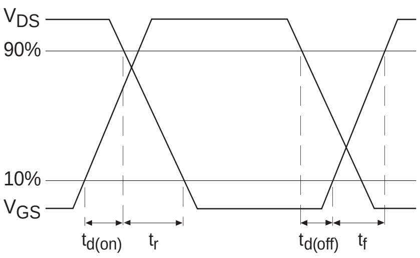


Fig 10b. Switching Time Waveforms

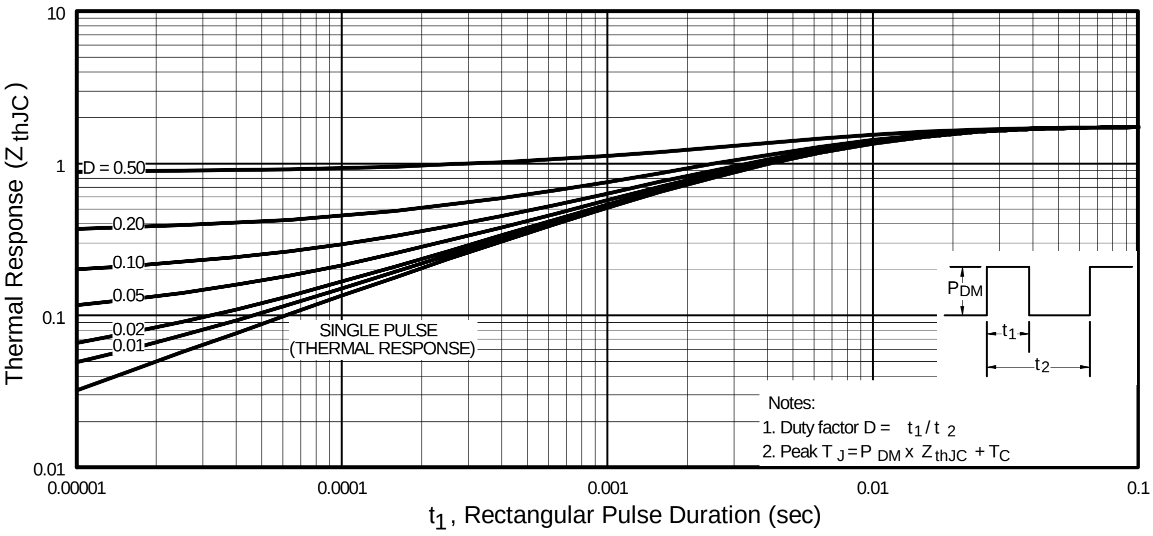


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Case

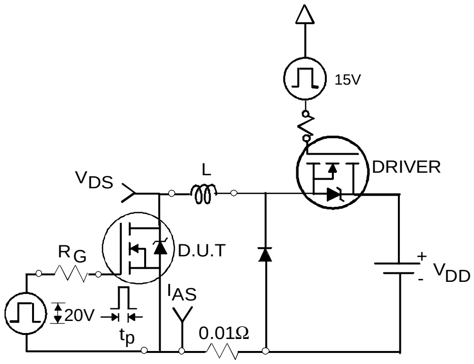


Fig 12a. Unclamped Inductive Test Circuit

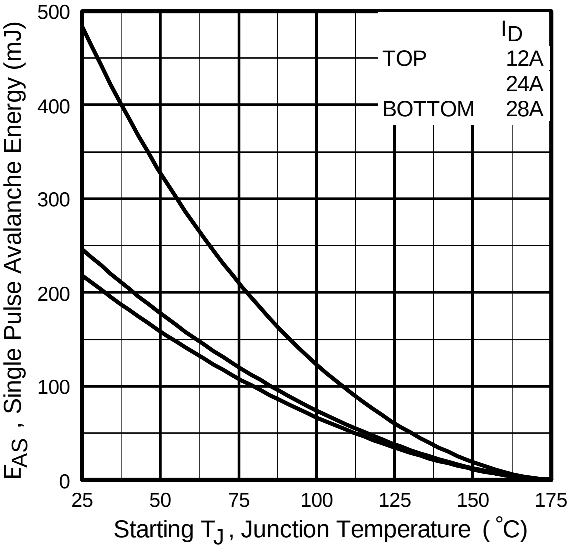


Fig 12c. Maximum Avalanche Energy Vs. Drain Current

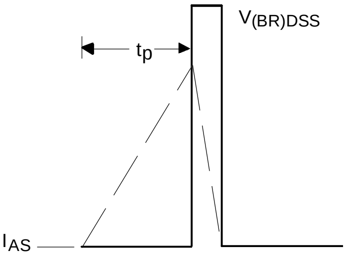


Fig 12b. Unclamped Inductive Waveforms

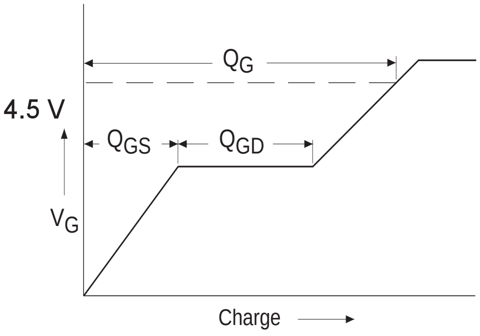


Fig 13a. Basic Gate Charge Waveform

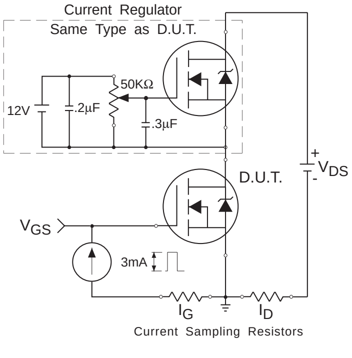
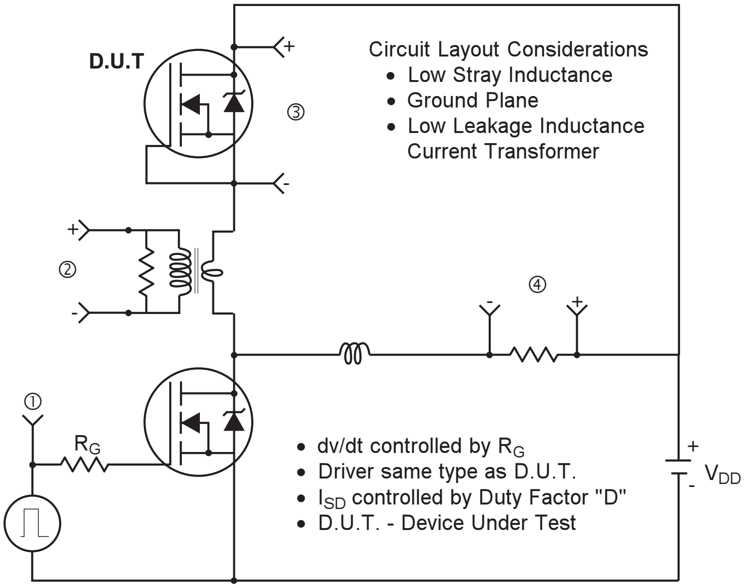


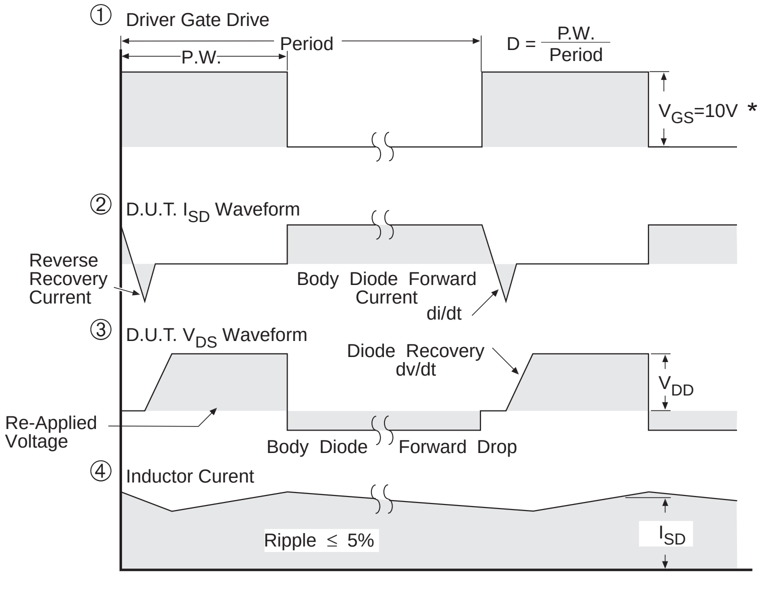
Fig 13b. Gate Charge Test Circuit

Peak Diode Recovery dv/dt Test Circuit



Circuit Layout Considerations
- Low Stray Inductance
- Ground Plane
- Low Leakage Inductance Current Transformer

- dv/dt controlled by R_G
- Driver same type as D.U.T.
- I_{SD} controlled by Duty Factor "D"
- D.U.T. - Device Under Test

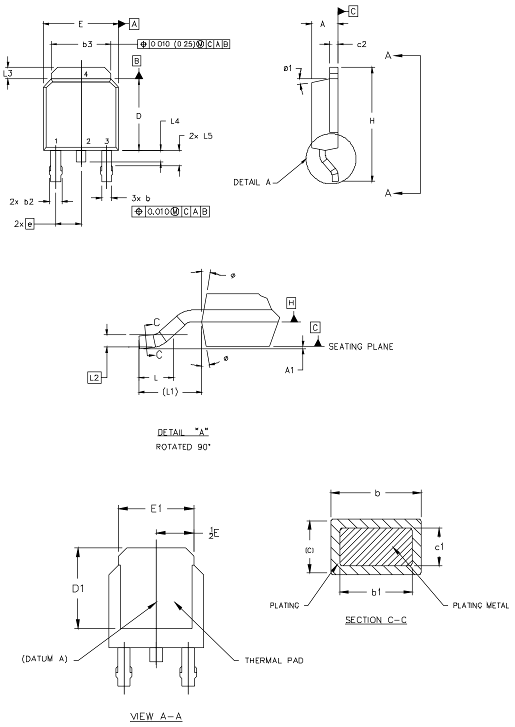


* V_{GS} = 5V for Logic Level Devices

Fig 14. For N-Channel HEXFET® Power MOSFETs

D-Pak (TO-252AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1.0 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M– 1994.
2.0 DIMENSIONS ARE SHOWN IN INCHES [MILLIMETERS].
3.0 LEAD DIMENSION UNCONTROLLED IN L5
4.0 DIMENSION D1 AND E1 ESTABLISH A MINIMUM MOUNTING SURFACE FOR THERMAL PAD.
5.0 SECTION C–C DIMENSIONS APPLY TO THE FLAT SECTION OF THE LEAD BETWEEN .005 [0.127] AND .010 [0.2540 FROM THE LEAD TIP.
6.0 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED .005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
7.0 OUTLINE CONFORMS TO JEDEC OUTLINE TO–252AA.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	.086	.094	
A1		0.13		.005	
b	0.64	0.89	.025	.035	5
b1	0.64	0.79	.025	0.031	5
b2	0.76	1.14	.030	.045	
b3	4.95	5.46	.195	.215	
c	0.46	0.61	.018	.024	5
c1	0.41	0.56	.016	.022	5
c2	.046	0.89	.018	.035	5
D	5 97	6 22	.235	.245	6
D1	5.21	–	.205	–	4
E	6 35	6 73	.250	.265	6
E1	4 32	–	.170		4
e	2.29		.090 BSC		
H	9.40	10.41	.370	.410	
L	1.40	1.78	.055	.070	
L1	2.74 REF.		.108 REF.		
L2	0.051 BSC		.020 BSC		
L3	0.89	1.27	.035	.050	
L4		1.02		.040	
L5	1.14	1.52	.045	.060	3
ø	0°	10°	0°	10°	
ø1	0°	15°	0°	15°	

LEAD ASSIGNMENTS

HEXFET

1.– GATE
2.– DRAIN
3.– SOURCE
4.– DRAIN

IGBTs, CoPACK

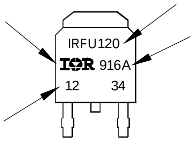
1.– GATE
2.– COLLECTOR
3.– EMITTER
4.– COLLECTOR

D-Pak (TO-252AA) Part Marking Information

EXAMPLE: THIS IS AN IRFR120
WITH ASSEMBLY
LOT CODE 1234
ASSEMBLED ON WW 16, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position
indicates "Lead-Free"

INTERNATIONAL
RECTIFIER
LOGO



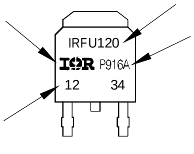
PART NUMBER

DATE CODE
YEAR 9 = 1999
WEEK 16
LINE A

ASSEMBLY
LOT CODE

OR

INTERNATIONAL
RECTIFIER
LOGO



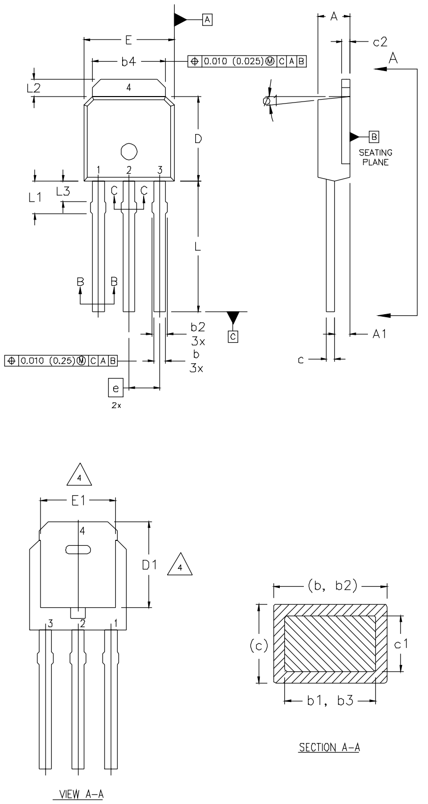
PART NUMBER

DATE CODE
P = DESIGNATES LEAD-FREE
PRODUCT (OPTIONAL)
YEAR 9 = 1999
WEEK 16
A = ASSEMBLY SITE CODE

ASSEMBLY
LOT CODE

I-Pak (TO-251AA) Package Outline

Dimensions are shown in millimeters (inches)



NOTES:

1 DIMENSIONING AND TOLERANCING PER ASME Y14.5 M- 1994.
2 DIMENSIONS ARE SHOWN IN MILLIMETERS [INCHES].
3 DIMENSION D & E DO NOT INCLUDE MOLD FLASH. MOLD FLASH SHALL NOT EXCEED 0.005" (0.127) PER SIDE. THESE DIMENSIONS ARE MEASURED AT THE OUTERMOST EXTREMES OF THE PLASTIC BODY.
4 THERMAL PAD CONTOUR OPTION WITHIN DIMENSION b4, L2, E1 & D1.
5 LEAD DIMENSION UNCONTROLLED IN L3.
6 DIMENSION b1, b3 APPLY TO BASE METAL ONLY.
7 OUTLINE CONFORMS TO JEDEC OUTLINE TO-251AA.
8 CONTROLLING DIMENSION : INCHES.

SYMBOL	DIMENSIONS				NOTES
	MILLIMETERS		INCHES		
	MIN.	MAX.	MIN.	MAX.	
A	2.18	2.39	0.086	.094	
A1	0.89	1.14	0.035	0.045	
b	0.64	0.89	0.025	0.035	
b1	0.64	0.79	0.025	0.031	4
b2	0.76	1.14	0.030	0.045	
b3	0.76	1.04	0.030	0.041	
b4	5.00	5.46	0.195	0.215	4
c	0.46	0.61	0.018	0.024	
c1	0.41	0.56	0.016	0.022	
c2	.046	0.86	0.018	0.035	
D	5.97	6.22	0.235	0.245	3, 4
D1	5.21	–	0.205	–	4
E	6.35	6.73	0.250	0.265	3, 4
E1	4.32	–	0.170	–	4
e	2.29		0.090 BSC		
L	8.89	9.60	0.350	0.380	
L1	1.91	2.29	0.075	0.090	
L2	0.89	1.27	0.035	0.050	4
L3	1.14	1.52	0.045	0.060	5
ø1	0°	15°	0°	15°	

LEAD ASSIGNMENTS

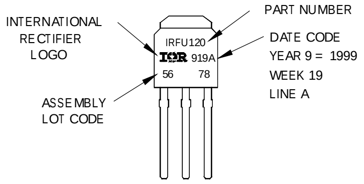
HEXFET

1.- GATE
2.- DRAIN
3.- SOURCE
4.- DRAIN

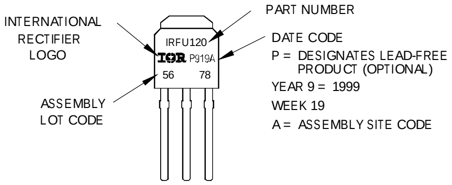
I-Pak (TO-251AA) Part Marking Information

EXAMPLE: THIS IS AN IRFU120
WITH ASSEMBLY
LOT CODE 5678
ASSEMBLED ON WW 19, 1999
IN THE ASSEMBLY LINE "A"

Note: "P" in assembly line position indicates "Lead-Free"

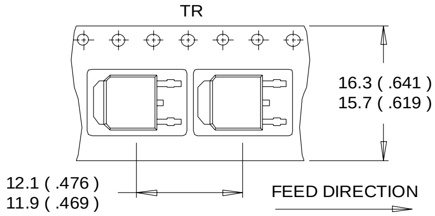


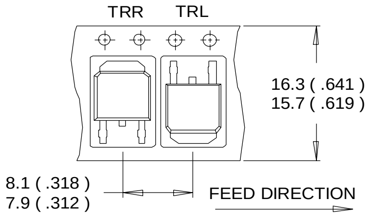
OR



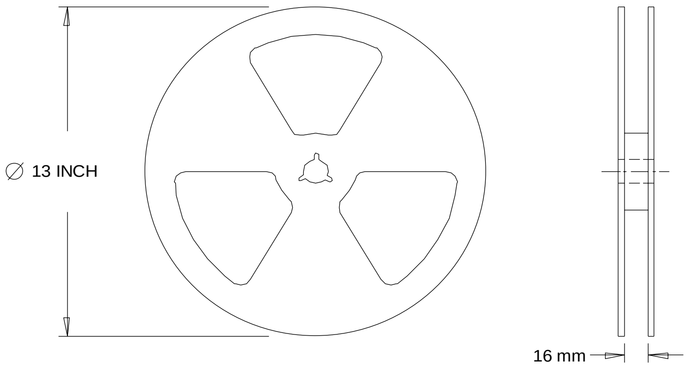
D-Pak (TO-252AA) Tape & Reel Information

Dimensions are shown in millimeters (inches)





NOTES :
1. CONTROLLING DIMENSION : MILLIMETER.
2. ALL DIMENSIONS ARE SHOWN IN MILLIMETERS (INCHES).
3. OUTLINE CONFORMS TO EIA-481 & EIA-541.



NOTES :
1. OUTLINE CONFORMS TO EIA-481.

Notes:

① Repetitive rating; pulse width limited by max. junction temperature.

② Starting $T_J = 25°C$, L = 0.54mH $R_G = 25\Omega$, $I_{AS} = 28A$.

③ Pulse width ≤ 400µs; duty cycle ≤ 2%.

④ Calculated continuous current based on maximum allowable junction temperature. Package limitation current is 30A.

⑤ R_θ is measured at T_J approximately 90°C

Data and specifications subject to change without notice.
This product has been designed and qualified for the Industrial market.
Qualification Standards can be found on IR's Web site.

International
IOR Rectifier

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TAC Fax: (310) 252-7903
Visit us at www.irf.com for sales contact information. 12/04

Note: For the most current drawings please refer to the IR website at:
http://www.irf.com/package/