



**THE DATASHEET OF
IPP80N08S2L07AKSA1**



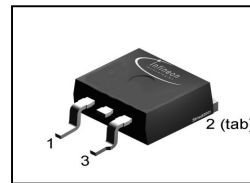
OptiMOS™ Power-Transistor
Features

- N-channel Logic Level - Enhancement mode
- Automotive AEC Q101 qualified
- MSL1 up to 260°C peak reflow
- 175°C operating temperature
- **Green package (lead free)**
- Ultra low Rds(on)
- 100% Avalanche tested

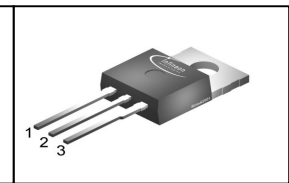
Product Summary

V_{DS}	75	V
$R_{DS(on),max}$ (SMD version)	6.8	mΩ
I_D	80	A

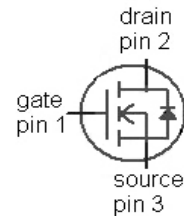
PG-TO263-3-2



PG-TO220-3-1



Type	Package	Ordering Code	Marking
IPB80N08S2L-07	PG-TO263-3-2	SP0002-19051	2N08L07
IPP80N08S2L-07	PG-TO220-3-1	SP0002-19050	2N08L07


Maximum ratings, at $T_j=25\text{ °C}$, unless otherwise specified

Parameter	Symbol	Conditions	Value	Unit
Continuous drain current ¹⁾	I_D	$T_C=25\text{ °C}$, $V_{GS}=10\text{ V}^{1)}$	80	A
		$T_C=100\text{ °C}$, $V_{GS}=10\text{ V}^{2)}$	80	
Pulsed drain current ²⁾	$I_{D,pulse}$	$T_C=25\text{ °C}$	320	
Avalanche energy, single pulse ²⁾	E_{AS}	$I_D=80\text{ A}$	810	mJ
Gate source voltage	V_{GS}		±20	V
Power dissipation	P_{tot}	$T_C=25\text{ °C}$	300	W
Operating and storage temperature	T_j , T_{stg}		-55 ... +175	°C
IEC climatic category; DIN IEC 68-1			55/175/56	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	
Thermal characteristics²⁾						
Thermal resistance, junction - case	R_{thJC}		-	-	0.5	K/W
Thermal resistance, junction - ambient, leaded	R_{thJA}		-	-	62	
SMD version, device on PCB	R_{thJA}	minimal footprint	-	-	62	
		6 cm ² cooling area ³⁾	-	-	40	

Electrical characteristics, at $T_j=25\text{ °C}$, unless otherwise specified

Static characteristics

Drain-source breakdown voltage	$V_{(BR)DSS}$	$V_{GS}=0\text{ V}, I_D=1\text{ mA}$	75	-	-	V
Gate threshold voltage	$V_{GS(th)}$	$V_{DS}=V_{GS}, I_D=250\text{ }\mu\text{A}$	1.2	1.6	2.0	
Zero gate voltage drain current	I_{DSS}	$V_{DS}=75\text{ V}, V_{GS}=0\text{ V}, T_j=25\text{ °C}$	-	0.01	1	μA
		$V_{DS}=75\text{ V}, V_{GS}=0\text{ V}, T_j=125\text{ °C}^{2)}$	-	1	100	
Gate-source leakage current	I_{GSS}	$V_{GS}=20\text{ V}, V_{DS}=0\text{ V}$	-	1	100	nA
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=4.5\text{ V}, I_D=80\text{ A}$	-	6.6	9	m Ω
		$V_{GS}=4.5\text{ V}, I_D=80\text{ A},$ SMD version	-	6.3	8.7	
Drain-source on-state resistance	$R_{DS(on)}$	$V_{GS}=10\text{ V}, I_D=80\text{ A}$	-	5.1	7.1	m Ω
		$V_{GS}=10\text{ V}, I_D=80\text{ A},$ SMD version	-	4.8	6.8	

Parameter	Symbol	Conditions	Values			Unit
			min.	typ.	max.	

Dynamic characteristics²⁾

Input capacitance	C_{iss}	$V_{GS}=0\text{ V}, V_{DS}=25\text{ V},$ $f=1\text{ MHz}$	-	5400	-	pF
Output capacitance	C_{oss}		-	1300	-	
Reverse transfer capacitance	C_{rss}		-	590	-	
Turn-on delay time	$t_{d(on)}$	$V_{DD}=40\text{ V}, V_{GS}=10\text{ V},$ $I_D=80\text{ A}, R_G=1.1\ \Omega$	-	19	-	ns
Rise time	t_r		-	55	-	
Turn-off delay time	$t_{d(off)}$		-	85	-	
Fall time	t_f		-	22	-	

Gate Charge Characteristics²⁾

Gate to source charge	Q_{gs}	$V_{DD}=60\text{ V}, I_D=80\text{ A},$ $V_{GS}=0\text{ to }10\text{ V}$	-	18	23	nC
Gate to drain charge	Q_{gd}		-	69	83	
Gate charge total	Q_g		-	183	233	
Gate plateau voltage	$V_{plateau}$		-	3.4	-	V

Reverse Diode

Diode continuous forward current ²⁾	I_S	$T_C=25\text{ }^\circ\text{C}$	-	-	80	A
Diode pulse current ²⁾	$I_{S,pulse}$		-	-	320	
Diode forward voltage	V_{SD}	$V_{GS}=0\text{ V}, I_F=80\text{ A},$ $T_J=25\text{ }^\circ\text{C}$	-	0.9	1.3	V
Reverse recovery time ²⁾	t_{rr}	$V_R=40\text{ V}, I_F=I_S,$ $di_F/dt=100\text{ A}/\mu\text{s}$	-	95	120	ns
Reverse recovery charge ²⁾	Q_{rr}		-	240	300	nC

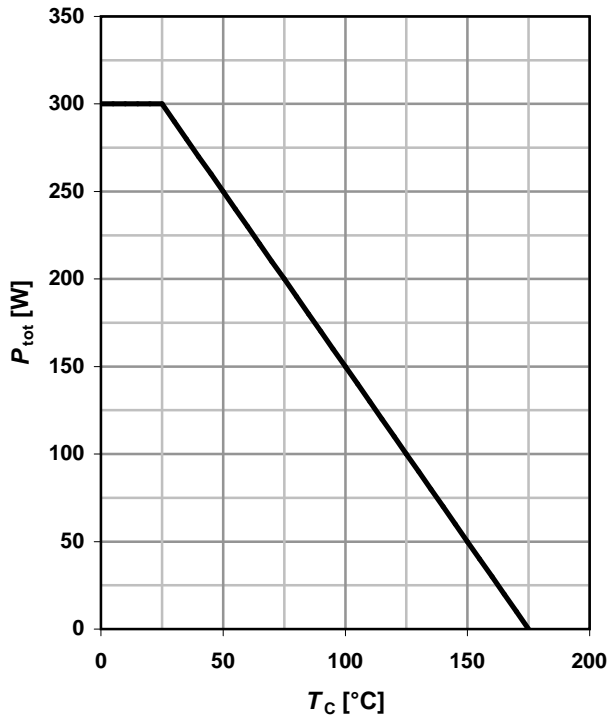
¹⁾ Current is limited by bondwire; with an $R_{thJC} = 0.5\text{K/W}$ the chip is able to carry 135A at 25°C.

²⁾ Defined by design. Not subject to production test.

³⁾ Device on 40 mm x 40 mm x 1.5 mm epoxy PCB FR4 with 6 cm² (one layer, 70 μm thick) copper area for drain connection. PCB is vertical in still air.

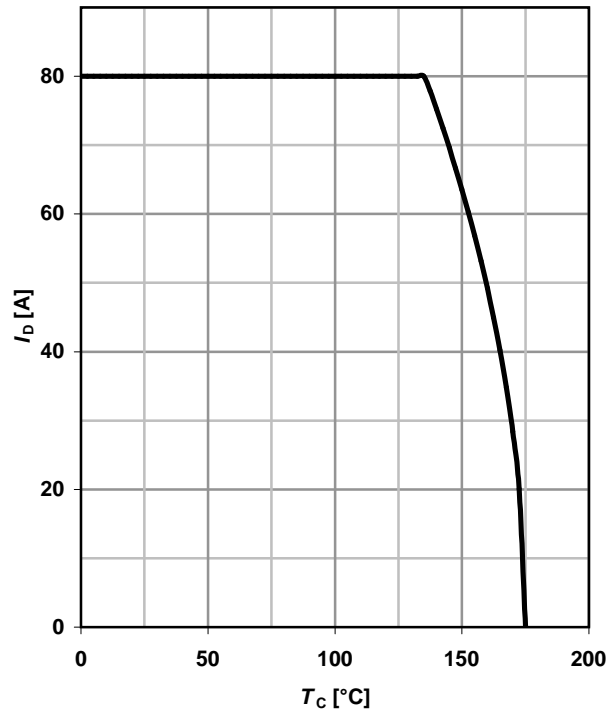
1 Power dissipation

$P_{tot} = f(T_C); V_{GS} \geq 4 \text{ V}$



2 Drain current

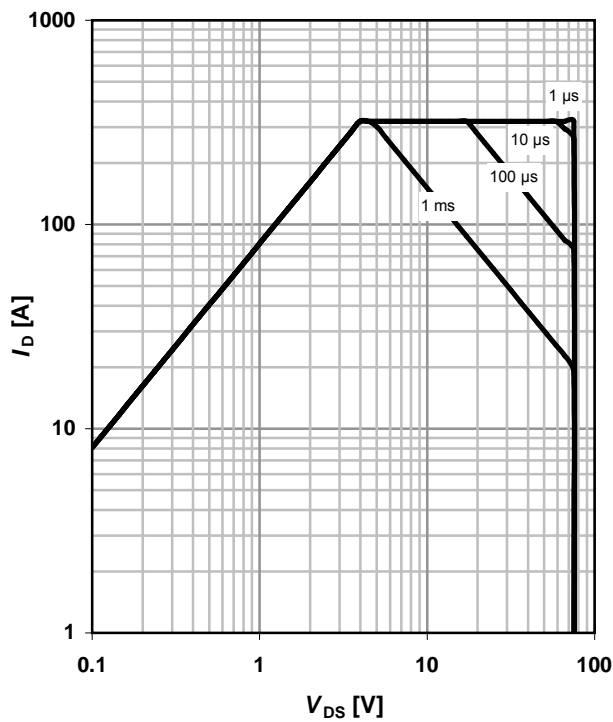
$I_D = f(T_C); V_{GS} \geq 10 \text{ V}$



3 Safe operating area

$I_D = f(V_{DS}); T_C = 25 \text{ °C}; D = 0$

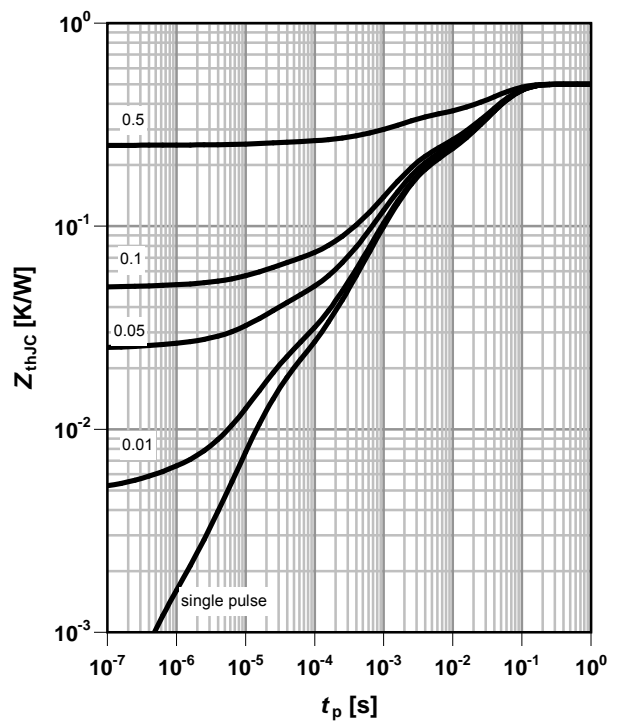
parameter: t_p



4 Max. transient thermal impedance

$Z_{thJC} = f(t_p)$

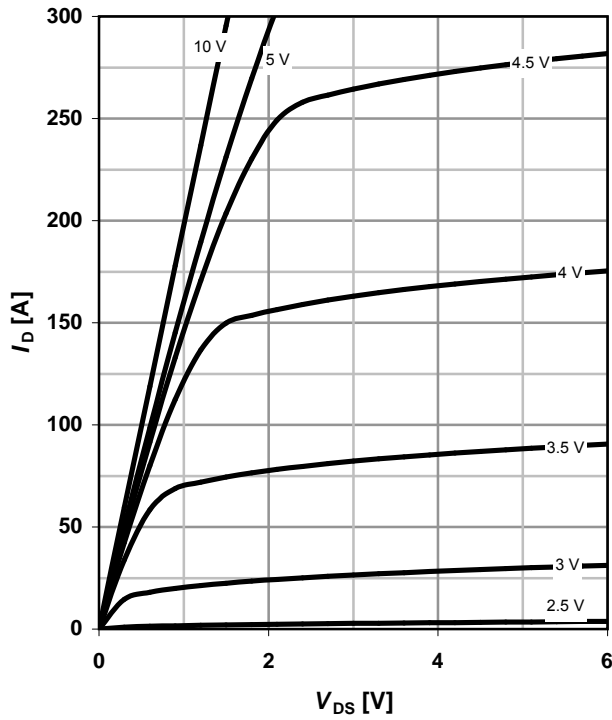
parameter: $D = t_p/T$



5 Typ. output characteristics

$I_D = f(V_{DS}); T_j = 25\text{ }^\circ\text{C}$

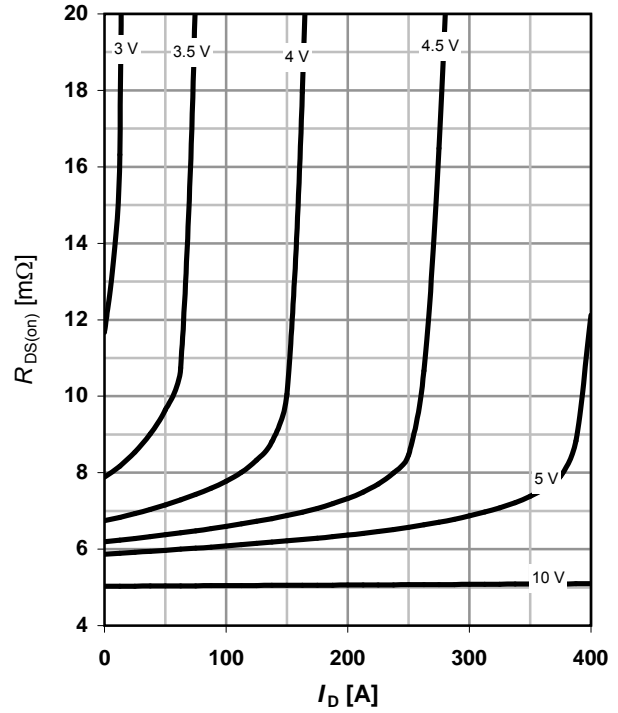
parameter: V_{GS}



6 Typ. drain-source on-state resistance

$R_{DS(on)} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

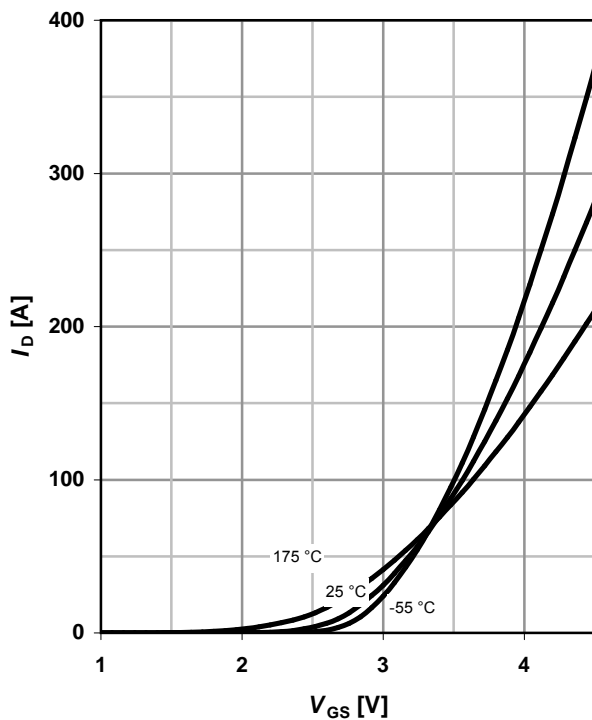
parameter: V_{GS}



7 Typ. transfer characteristics

$I_D = f(V_{GS}); V_{DS} = 6\text{V}$

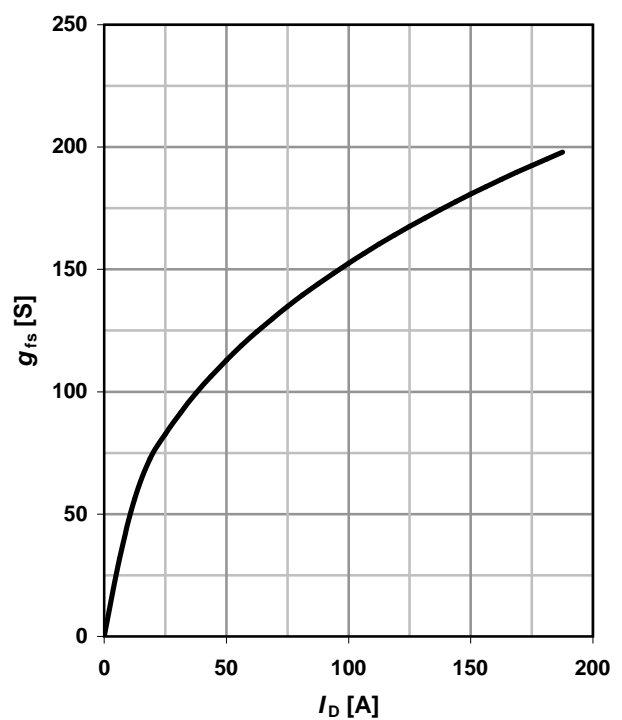
parameter: T_j



8 Typ. Forward transconductance

$g_{fs} = f(I_D); T_j = 25\text{ }^\circ\text{C}$

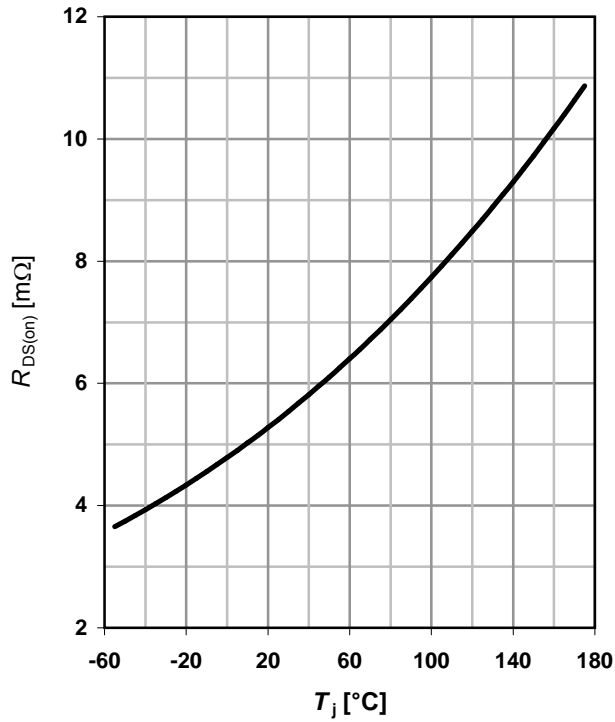
parameter: g_{fs}



9 Typ. Drain-source on-state resistance

$$R_{DS(ON)} = f(T_j)$$

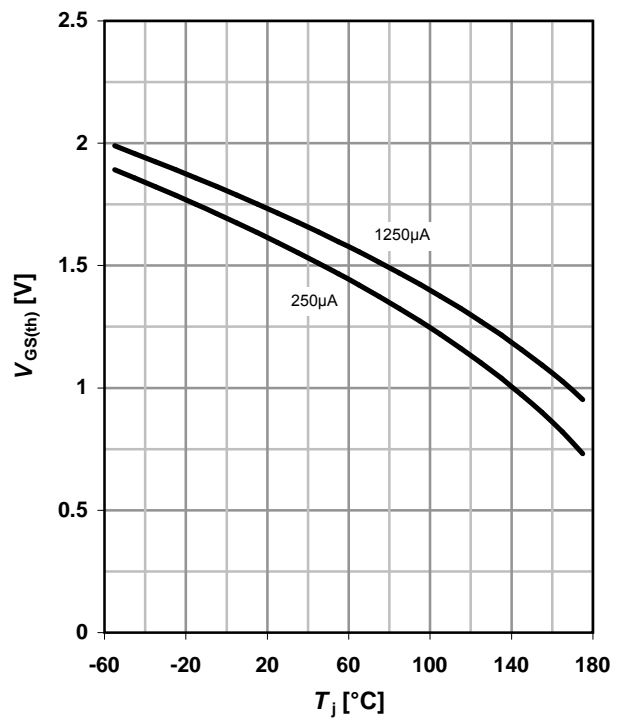
parameter: $I_D = 80\text{ A}$; $V_{GS} = 10\text{ V}$



10 Typ. gate threshold voltage

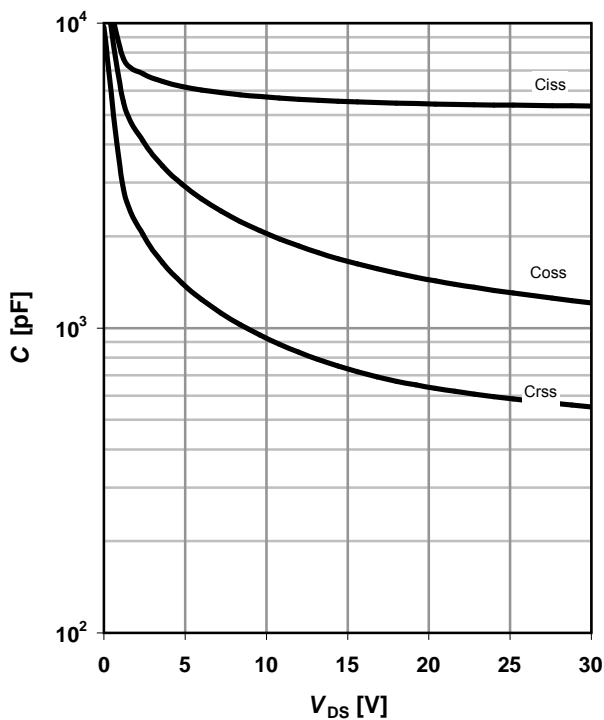
$$V_{GS(th)} = f(T_j); V_{GS} = V_{DS}$$

parameter: I_D



11 Typ. capacitances

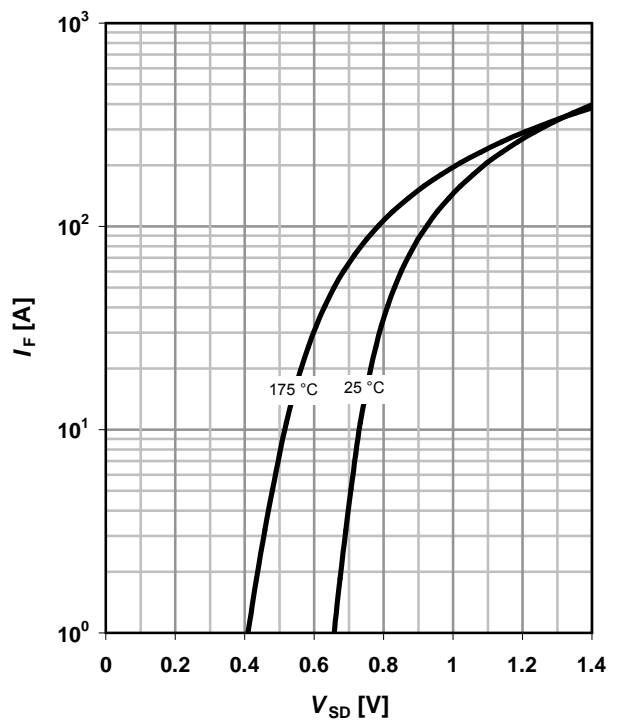
$$C = f(V_{DS}); V_{GS} = 0\text{ V}; f = 1\text{ MHz}$$



12 Typical forward diode characteristics

$$I_F = f(V_{SD})$$

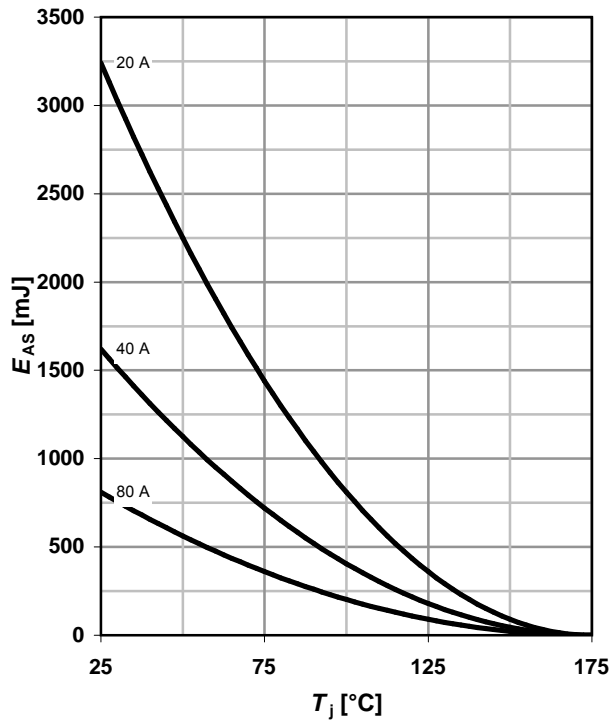
parameter: T_j



13 Typical avalanche energy

$E_{AS} = f(T_j)$

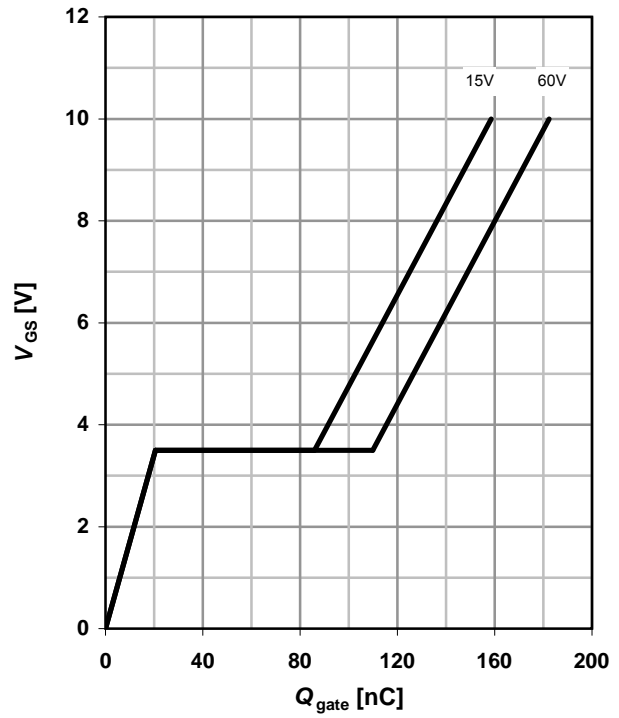
parameter: I_D



14 Typ. gate charge

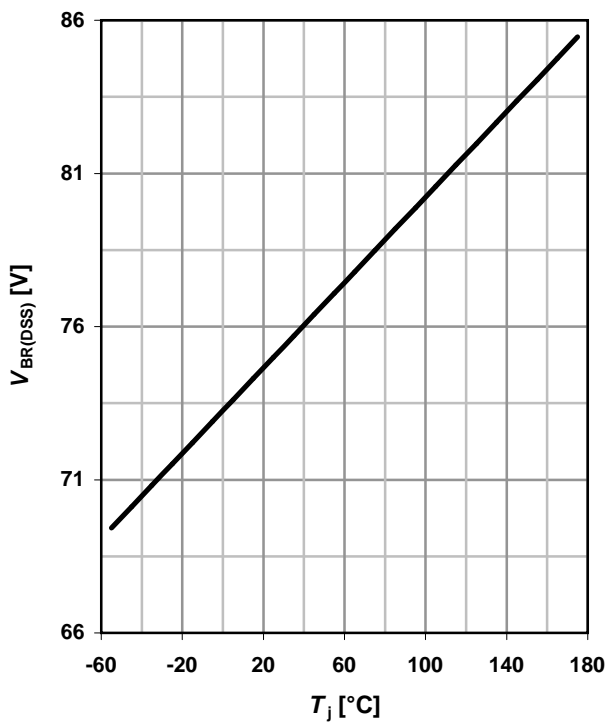
$V_{GS} = f(Q_{gate}); I_D = 80 \text{ A pulsed}$

parameter: V_{DD}

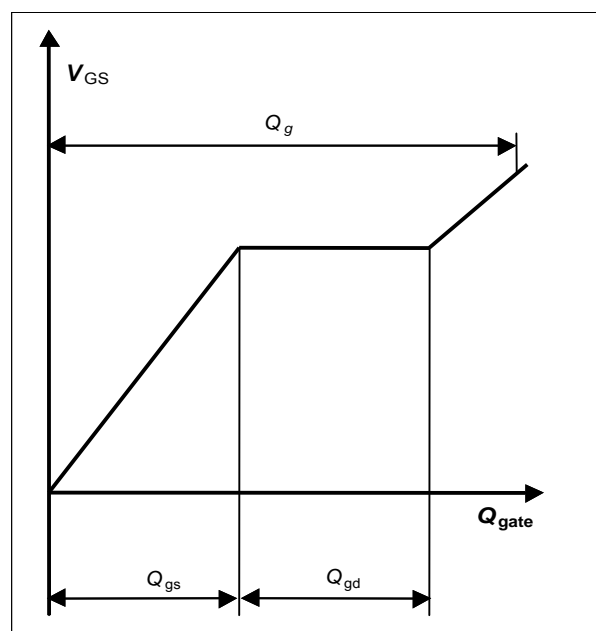


15 Typ. drain-source breakdown voltage

$V_{BR(DSS)} = f(T_j); I_D = 1 \text{ mA}$



16 Gate charge waveforms



Published by
Infineon Technologies AG
Am Campeon 1-12
D-85579 Neubiberg
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Revision History

Version	Date	Changes
Revision 1.0	03.03.2006	Final Data Sheet
Revision 1.1	07.03.2014	SOA extended

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